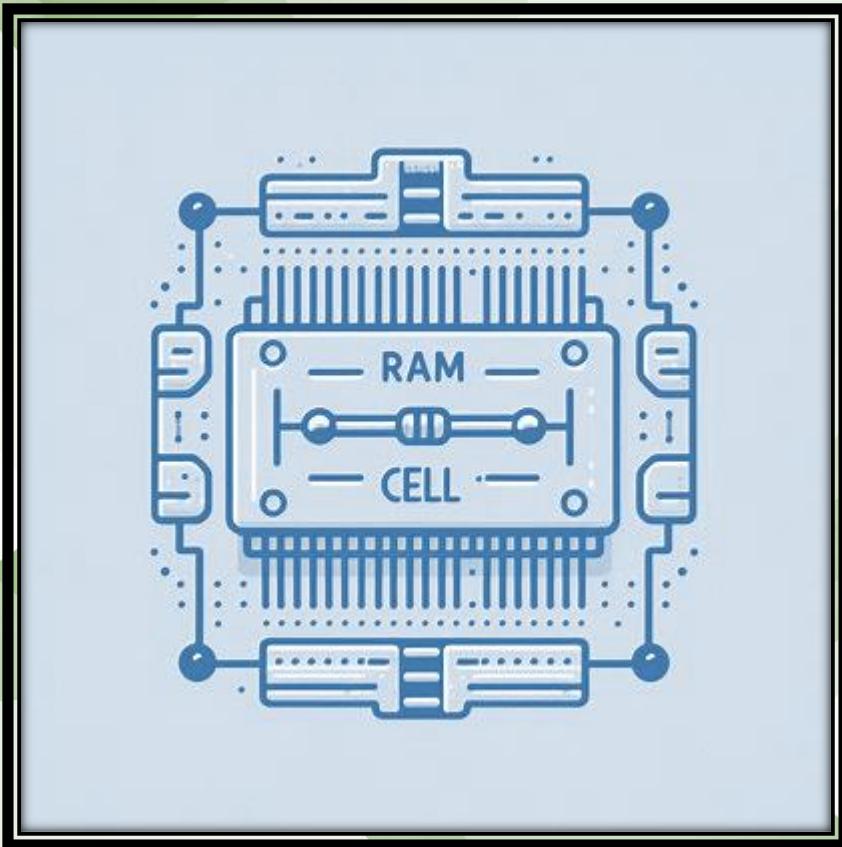


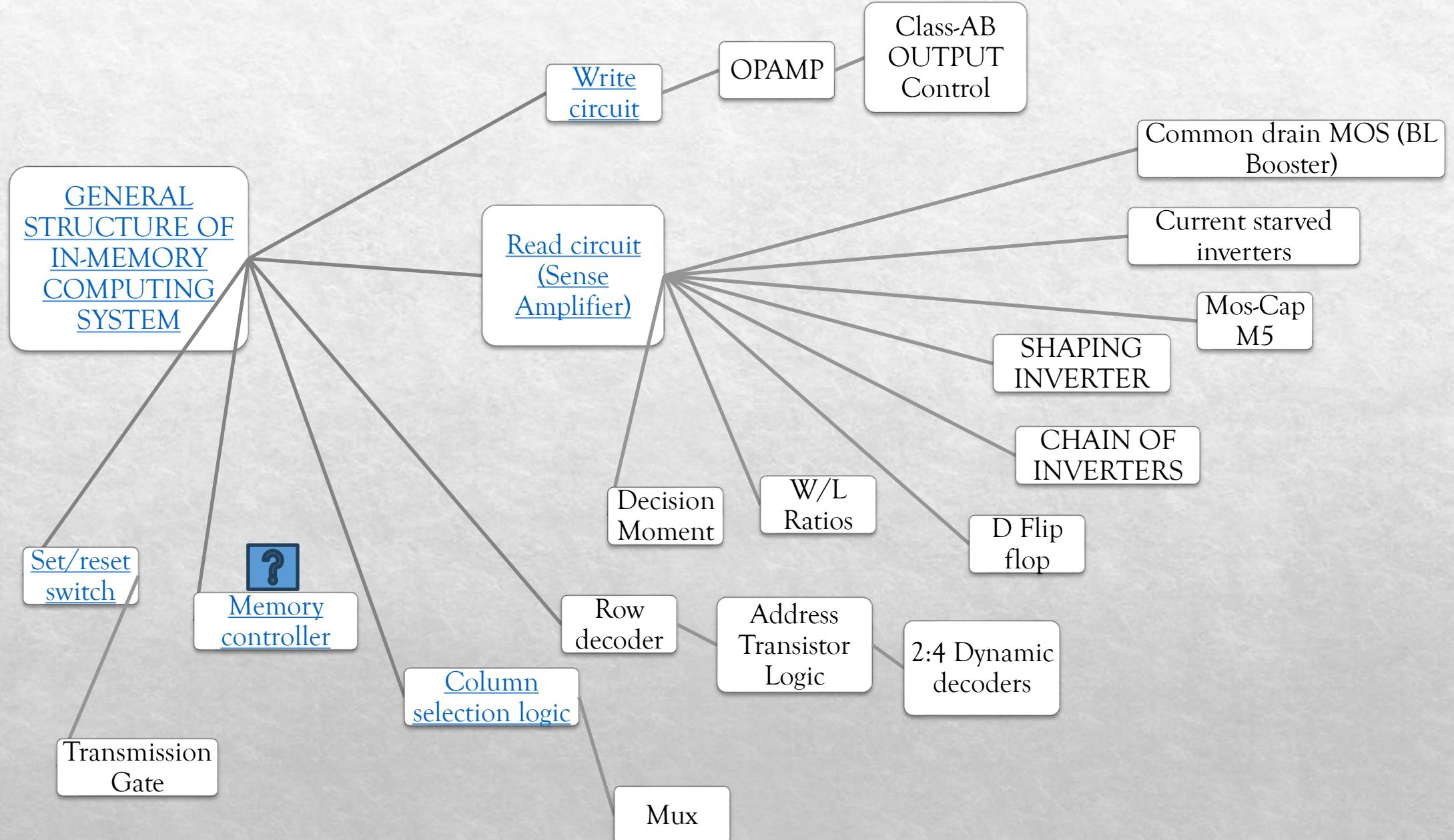
ReRAM
(Memristor)

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Why In-Memory Computing

Von Neumann Architecture Limitations:

1. Widely adopted since 1945, separating CPU and storage device.
2. Requires data transfer between memory and CPU via transmission interface.
3. Increasing data volume leads to high latency and energy consumption, known as the "von Neumann bottleneck."

Data Processing Bottleneck:

1. High latency and energy consumption during data transmission.
2. Bottleneck becomes more pronounced as data volume increases.

Attempts to Enhance Performance:

1. Integration of multiple processing cores.
2. Design of dedicated accelerators.
3. These solutions improve data processing speed but worsen the computation and data transportation gap.

In-Memory Computing Advantages:

1. Integrates data storage and computation functions.
2. Reduces the need for data transfer between memory and CPU.
3. Addresses the von Neumann bottleneck by minimizing latency and energy consumption.
4. Supports efficient vector-matrix multiplication and neural network applications with RRAM technology.

Figure. Schemes of von Neumann architecture versus in-memory computing.

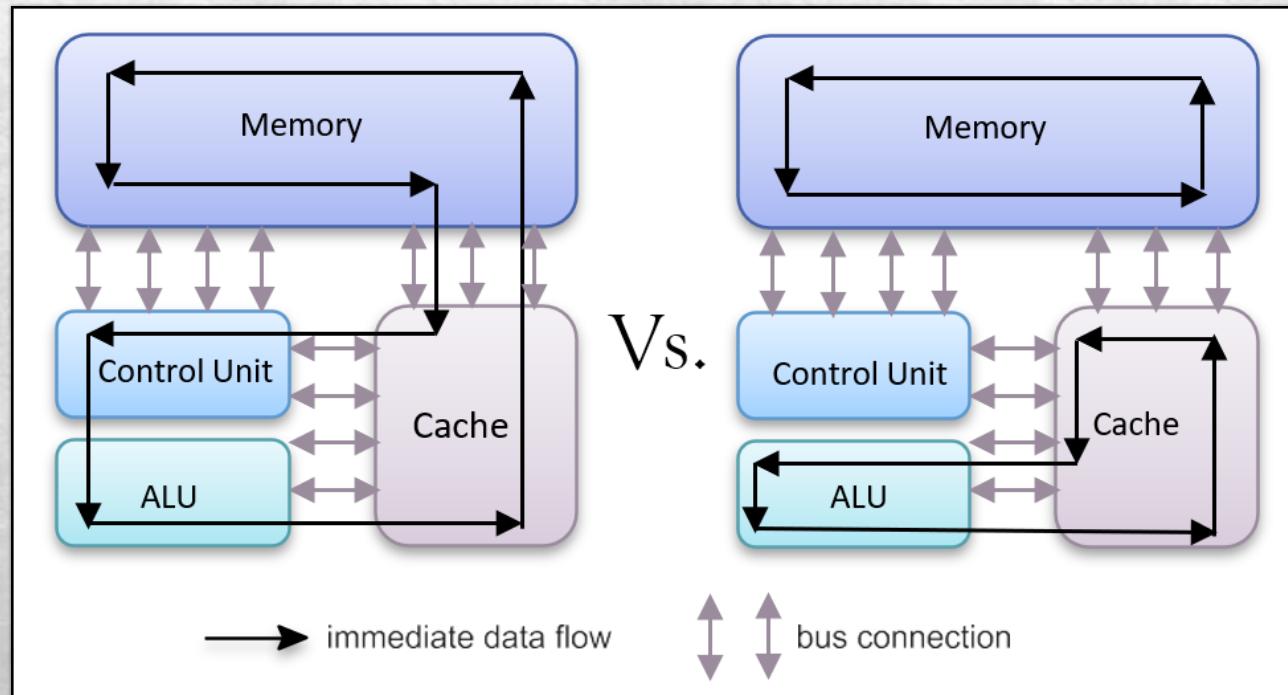


Diagram of von Neumann bottleneck.

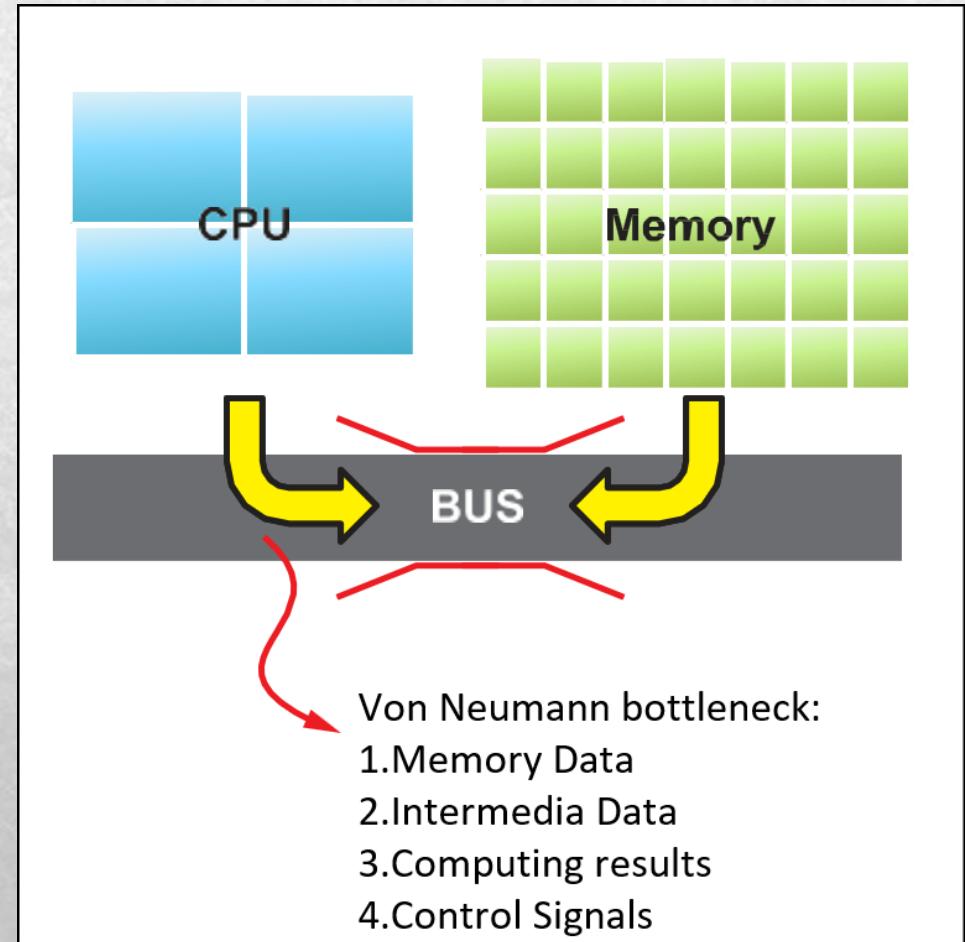
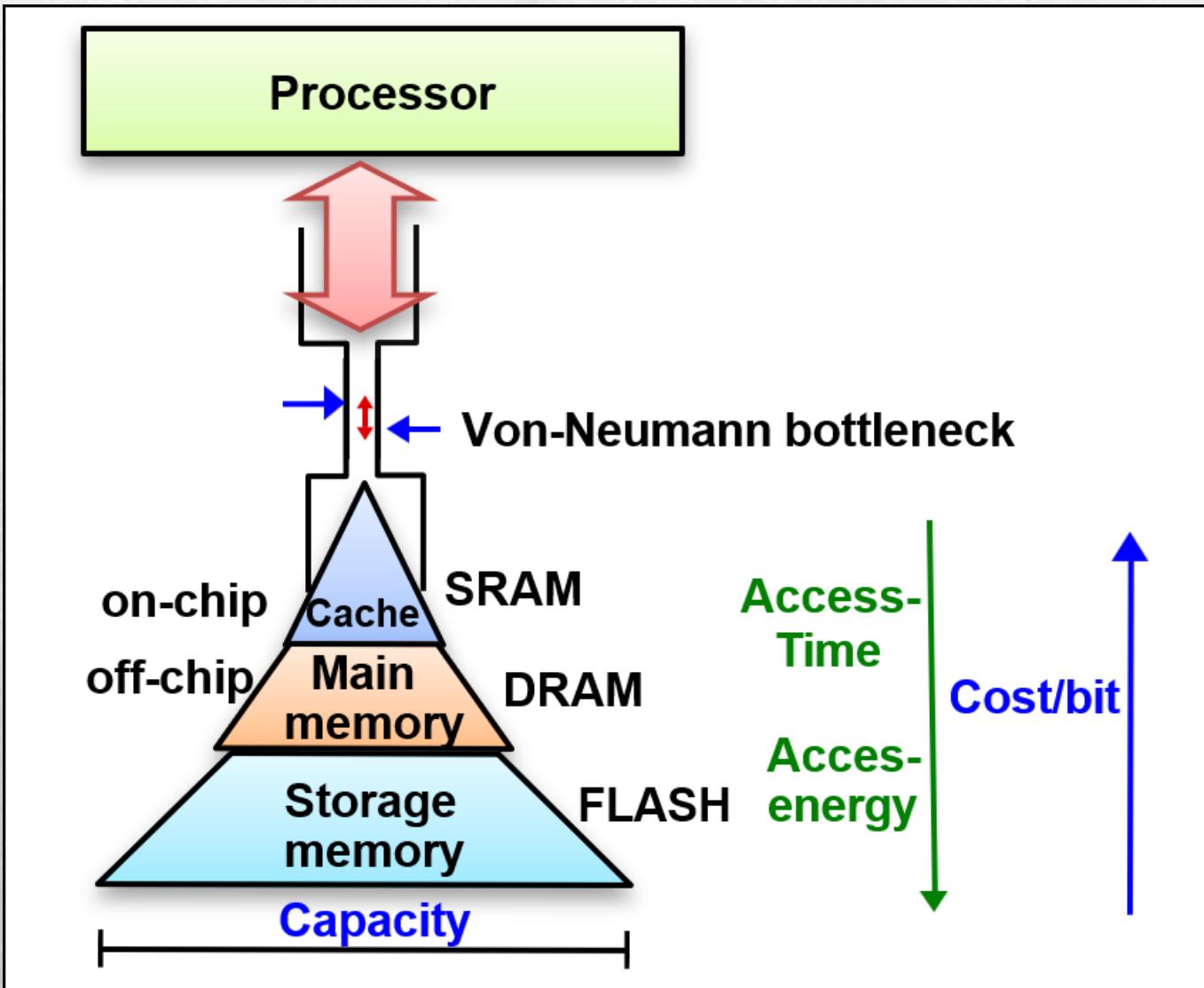


Figure : The von-Neumann bottleneck. Possible ways in which emerging non-volatile memories (NVMs) (eNVM) can be integrated into the memory hierarchy.



Applications of In-Memory Computing

Integrated Data Storage and Computation:

1. Combines data storage and arithmetic computation functions in one scheme.
2. Utilizes RRAM arrays with innovative peripheral circuitry.

Enhanced Computational Capabilities:

1. Enables efficient vector-matrix multiplication beyond basic Boolean logic.
2. Provides a hardware solution for matrix-multiplication-dependent neural networks and related applications.

3D-Stackable RRAM and On-Chip Training:

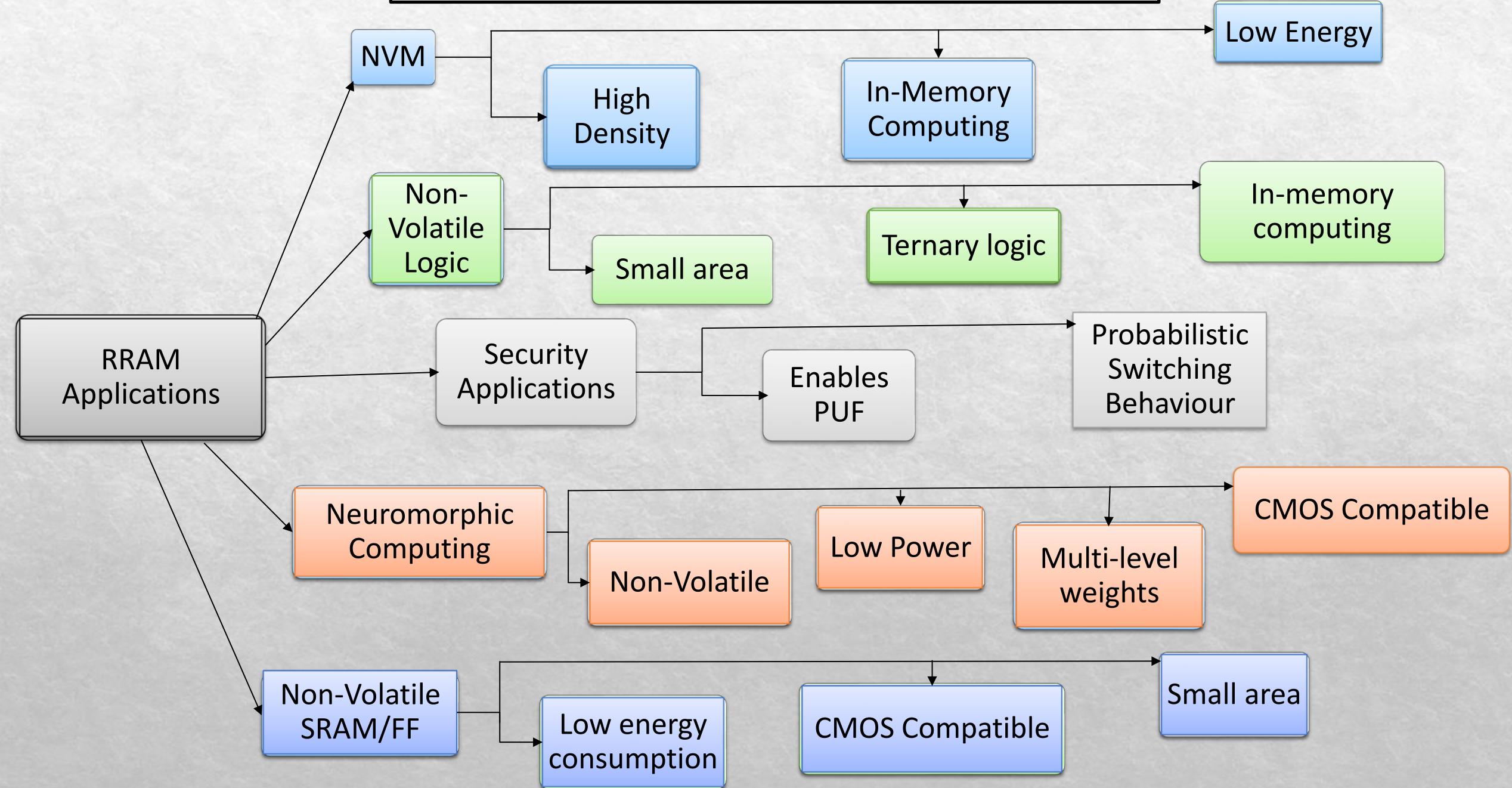
1. Introduced for large-scale integration.
2. Enhances scalability and versatility of RRAM-based systems.

Overcoming the von Neumann Bottleneck:

1. Circuit design and system organization of RRAM-based in-memory computing are crucial.
2. Facilitates large-scale implementation of ultra-low-power and dense neural network accelerators.

In-memory computing, also called as computing-in-memory (CIM) or process-in-memory (PIM), fuses memory modules and data processing units to reduce and even eliminate the frequent data transportation between memory and data processing units in modern computers

Resistive Random Access Memory (RRAM) applications.



Types of Memory

- ❑ Key:

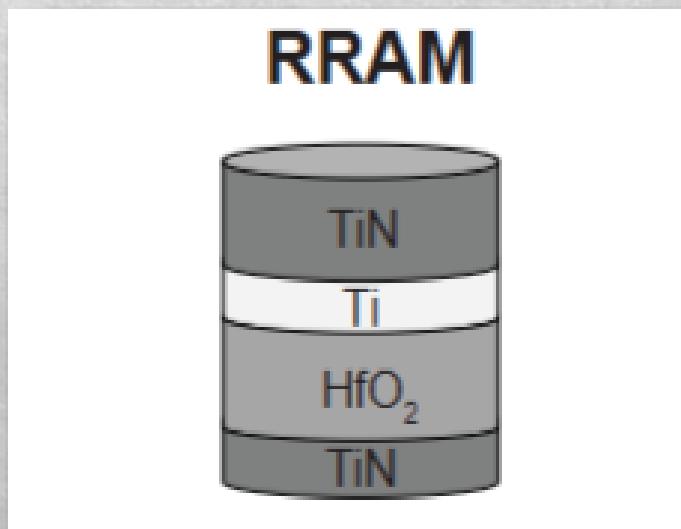
- **Volatility:** Whether the memory retains data when power is off.
- **Speed:** Read/write speed.
- **Density:** Amount of data stored per unit area.
- **Programming:** How data is written to the memory.
- **Use Cases:** Typical applications for the memory type.

Memory Type	Volatility	Speed	Density	Programming	Use Cases
SRAM	Volatile	Very high	Moderate	Deterministic	CPU caches
Flash Memory	Non-volatile	Moderate	High	Sequential	SSDs, USB drives
MRAM	Non-volatile	High	Moderate	Stochastic	High-speed, nonvolatile applications
Racetrack Memory	Non-volatile	Moderate	Extremely high	Sequential	High-density storage
PCM	Non-volatile	Moderate	Moderate	Linear	Optical discs, emerging memory
RRAM	Non-volatile	Moderate	High	Stochastic	High-density, low-power applications
Memristors	Non-volatile	Moderate	Moderate	Stochastic	Neural networks, neuromorphic computing
Analog Memory Devices	Volatile/Non-volatile	High	Moderate	Analog	Deep learning accelerators
Nonvolatile Memory Materials	Non-volatile	Varies	Varies	Varies	Machine learning hardware

Memory Type	Volatility	Key Characteristics	Use Cases
Static Random Access Memory (SRAM)	Volatile	Fastest read/write speed (sub-nanosecond); Mature fabrication process	Cache memory; High-speed applications
Flash Memory (NAND Flash)	Nonvolatile	Supports sequential data accesses; Complex techniques for robustness and reliability	USB drives; SSDs
Magnetic Random Access Memory (MRAM)	Nonvolatile	Fast write speeds (comparable to SRAM); Stochastic programming	Embedded systems; Memory caches
Racetrack Memory	Nonvolatile	Extremely high density (20 nm-wide nanowire); Supports sequential access along tracks	High-density storage applications; Space-efficient data storage
Phase Change Memory (PCM)	Nonvolatile	Linear conductance update characteristic	Neuromorphic computing; Specialized computing architectures
Resistive Random Access Memory (RRAM)	Nonvolatile	High resistivity ($M\Omega$ order); Supports 3D integration; Stochastic programming; Multilevel cell capability (up to 6 bits per cell)	AI acceleration; Neuromorphic computing; Advanced computing paradigms
Memristors	Nonvolatile	Can retain resistance state without power; Mimics synaptic weights	Neuromorphic computing; Energy-efficient computing hardware
Analog Memory Devices	Typically Nonvolatile	Stores data in continuous states; Includes resistive, capacitive, and photonic devices	Deep learning accelerators; Precision-required computing
Nonvolatile Memory Materials	Nonvolatile	Used to construct memory devices that don't require power to maintain data; Persistent storage of weights and states	Machine learning hardware; Reducing power consumption

Features:

- Resistive RAM is used here.
- Resistive Values will switch between high and low.

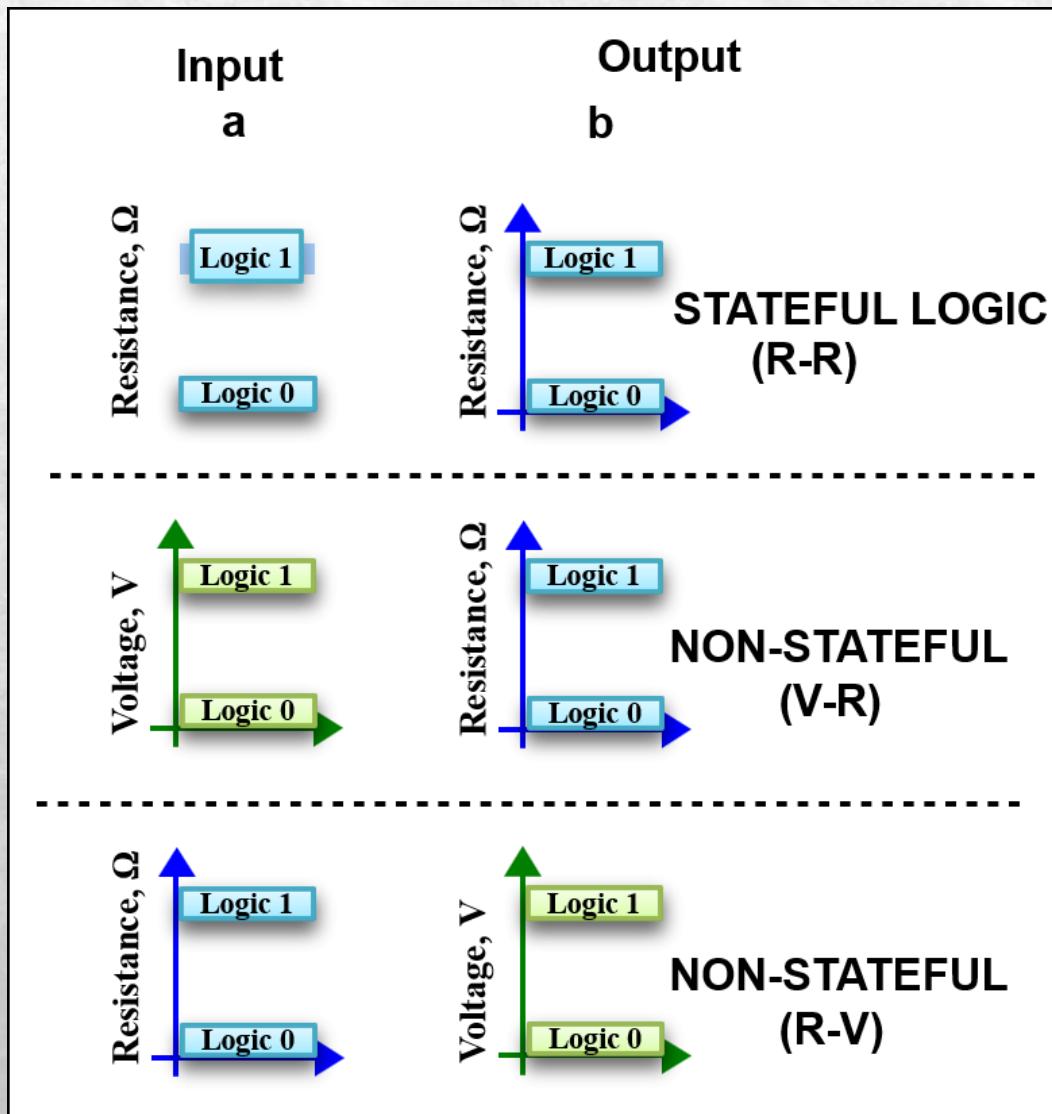


What is ReRAM?

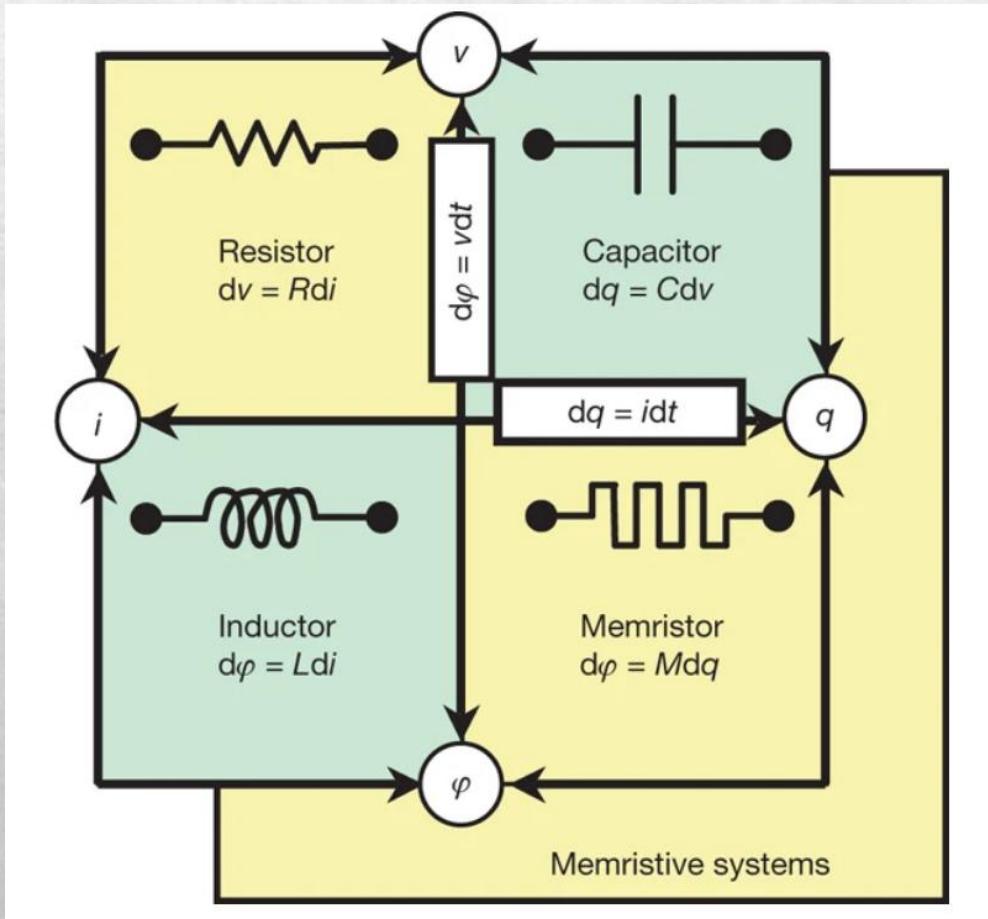
A resistive memory (RRAM, a.k.a. memristor) device generally represents any two-terminal electronic device whose resistance value can be programmed by applying external voltage/current with an appropriate configuration.

A single RRAM device contains a resistive layer sandwiched by two electrodes. The resistive layer is typically transition metal oxides, such as HfO_x, NbO_x, TiO_x, and TaO_x.

Stateful vs Non-stateful



If resistance is the only state variable, a memristive logic is said to be stateful.
If voltage is also used in addition to resistance, it is said to be non-stateful.



A **memristor** is a two-terminal passive electronic device whose resistance changes based on the **history of current** that has passed through it. It essentially "remembers" the amount of charge (or flux) that has previously flowed through it, making it a **non-volatile** memory element.

In the context of circuit theory, a memristor is described by the relationship between **flux (ϕ)** and **charge (q)**:

$$d\varphi = M \cdot dq$$

- ϕ (flux linkage) is the time integral of voltage ($v=d\phi/dt$)
- q (charge) is the time integral of current ($i=dq/dt$)
- M is the memristance, which is a function of charge or time, not a constant as in a regular resistor.

1T1R Cell

The 1T1R (One Transistor One Resistor) cell is a fundamental building block for memory technologies like Resistive Random-Access Memory (RRAM).

It consists of a single transistor connected in series with a resistor element that can change its resistance state (high or low) based on applied voltage.

- Components:
 - ✓ Transistor:
 1. Acts as a switch controlling the access to the resistor element.
 2. Isolates the selected cell from unselected cells, preventing current leakage and ensuring accurate reading and writing operations.
 - ✓ Resistor (Memristor):
 1. Stores the data as a high or low resistance state.
 2. Can be switched between these states by applying an appropriate voltage.

Components:

1. Top Electrode:

1. This is the terminal at the top of the RRAM structure, where the voltage is applied to control the switching of the device between different resistance states (high resistance and low resistance).

2. Gate:

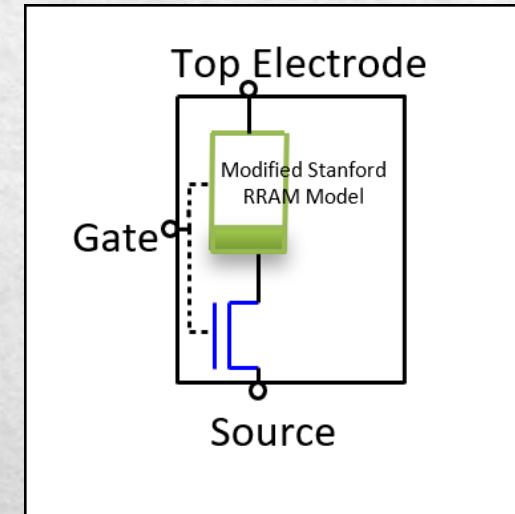
1. The gate likely refers to a control terminal that influences the state of the RRAM. In some advanced RRAM designs, a transistor or similar component may be used to modulate the operation of the memory cell, enhancing its functionality or stability.
2. The dotted line suggests a connection or influence between the gate and the resistive switching material (or model) inside the memory cell.

3. Source:

1. The source is the terminal at the bottom of the RRAM device, usually connected to ground or a specific reference voltage. It is part of the circuitry that forms the complete path for current flow through the device during operation.

4. Modified Stanford RRAM Model:

1. This label indicates that the RRAM device is modeled using a specific version or modification of the Stanford RRAM Model. The Stanford RRAM Model is a well-known computational model used to simulate the behavior of RRAM devices, helping in the understanding and design of such memory systems.
2. The modification could involve changes to the original model to better match the characteristics of the specific RRAM device in use, such as adjusting parameters for the material properties or the switching mechanism.



Composite 1T-1R model

Functionality:

•RRAM Operation:

- RRAM works by changing the resistance across a dielectric material sandwiched between two electrodes (Top Electrode and Source in this case). By applying a voltage, the device can switch between a low resistance state (LRS) and a high resistance state (HRS), representing binary data (0 or 1).

•Role of the Gate:

- In some designs, a gate can be used to control the switching process more precisely, potentially adding a third terminal to the RRAM structure, similar to a transistor. This can improve the memory device's performance, reliability, or allow for new functionalities like multi-level cell (MLC) storage.

Application:

•In-Memory Computing:

- Devices like the one depicted in the image are essential in developing in-memory computing systems, where memory and computation are closely integrated. This reduces the data transfer time and energy consumption compared to traditional computing architectures where memory and processing units are separate.

Resistive Random-Access Memory (RRAM), also known as a memristor, is a type of two-terminal electronic device that can have its resistance value adjusted by applying an external voltage or current.

1. Structure of RRAM Devices:

• **Basic Configuration:** An RRAM device is composed of a resistive layer positioned between two metal electrodes. The resistance of this layer can be changed through external electrical stimuli, enabling the device to store information.

• **Resistive Layer:** This is the core functional part of the RRAM device. It is typically made of transition metal oxides, which are materials known for their variable resistance properties. Common examples include:

- **HfO_x (Hafnium Oxide)**
- **NbO_x (Niobium Oxide)**
- **TiO_x (Titanium Oxide)**
- **TaO_x (Tantalum Oxide)**

• **Other Materials:** Besides the common transition metal oxides, other materials have also been found to exhibit resistive switching properties:

- **SrTiO₃ (Strontium Titanate)**
- **PrCaMnO₃ (Praseodymium Calcium Manganese Oxide)**
- **Ag**
- **(Silver-doped Amorphous Silicon)**

2. Resistive Switching Mechanisms:

(Formation vs Redistribution)

RRAM devices operate based on mechanisms that change the resistance of the resistive layer, allowing the device to switch between different states (e.g., high resistance or low resistance), which corresponds to binary data (0s and 1s). These mechanisms are generally categorized into two main types:

•Filamentary RRAM:

- **Mechanism:** In filamentary RRAM, the change in resistance is primarily due to the formation and dissolution of conductive filaments within the resistive layer. These filaments are typically made of metal ions or are created by the movement of oxygen vacancies (missing oxygen atoms) in the insulating material.
- **Formation and Dissolution:**
 - **Formation:** When a sufficient voltage is applied across the electrodes, metal ions or oxygen vacancies migrate and form a conductive path or filament, reducing the resistance (this is known as the **SET** operation).
 - **Dissolution:** Applying an opposite or higher voltage can break this filament, increasing the resistance (known as the **RESET** operation).
- **Applications:** Filamentary RRAM is known for its high scalability and fast switching speeds, making it suitable for high-density memory applications.

•Interfacial RRAM:

- **Mechanism:** Unlike filamentary RRAM, interfacial RRAM does not rely on the formation of conductive filaments. Instead, it changes resistance by redistributing oxygen vacancies at the interface between different materials in the device.
- **Interface Dynamics:** The resistive switching occurs due to the modulation of the barrier height at the interface, which alters the flow of current. The concentration and distribution of oxygen vacancies at the interface can be controlled by applying different voltages, leading to changes in resistance.
- **SET and RESET Operations:** Similar to filamentary RRAM, interfacial RRAM also utilizes SET (decreasing resistance) and RESET (increasing resistance) operations, but the mechanism is based on the interface modulation rather than filament formation.

3. Programming Operations:

•SET Operation:

- The SET operation is used to switch the RRAM device from a high-resistance state (HRS) to a low-resistance state (LRS). This is typically achieved by applying a positive voltage across the device, causing the formation of conductive filaments or modifying the interface to reduce resistance.
- **In Filamentary RRAM:** The SET operation causes metal ions or oxygen vacancies to form a continuous conductive filament, bridging the gap between the electrodes, and thereby increasing conductance (reducing resistance).
- **In Interfacial RRAM:** The SET operation increases the concentration of oxygen vacancies at the interface, reducing the barrier for current flow and lowering resistance.

•RESET Operation:

- The RESET operation reverses the SET process, switching the device back from a low-resistance state to a high-resistance state. This is usually done by applying a negative voltage or a higher voltage in the opposite direction.
- **In Filamentary RRAM:** The RESET operation breaks the conductive filament, either by electromigration of the metal ions or by the movement of oxygen vacancies away from the filament, thereby decreasing conductance (increasing resistance).
- **In Interfacial RRAM:** The RESET operation redistributes the oxygen vacancies away from the interface, increasing the barrier for current flow and thereby increasing resistance.

4. Applications and Advantages:

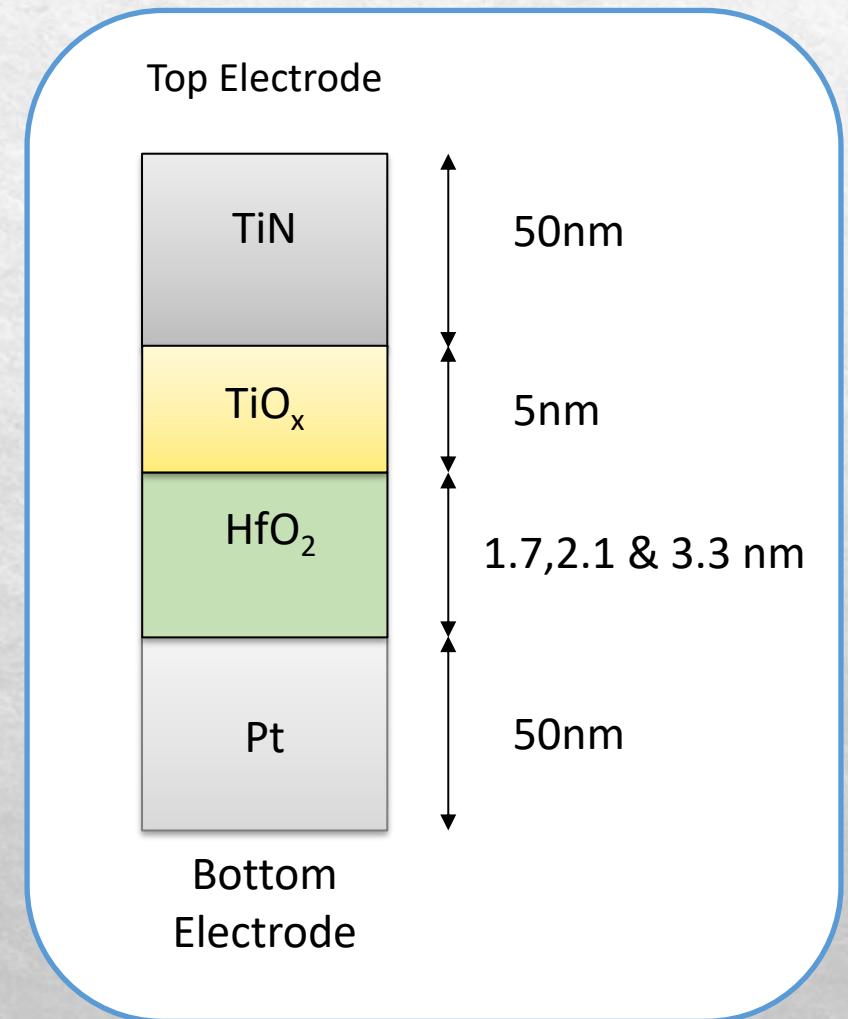
- **Non-Volatile Memory:** RRAM devices are non-volatile, meaning they retain their data even when power is turned off, similar to flash memory.
- **High Speed:** RRAM offers faster read and write speeds compared to traditional memory technologies like flash or DRAM.
- **Scalability:** RRAM can be scaled down to very small sizes, making it a good candidate for high-density memory applications.
- **Low Power Consumption:** The power required to perform SET and RESET operations is relatively low, which is beneficial for energy-efficient memory solutions.

In conclusion, RRAM devices represent a versatile and powerful memory technology, capable of achieving high speeds, low power consumption, and excellent scalability. The technology operates by modifying the resistance of a specialized layer between two electrodes through either filament formation or interfacial changes, making it suitable for a wide range of applications in modern electronics.

Stanford-PKU(Peking University) RRAM Model

We used a Stanford PKU model of RRAM.

- The Stanford-PKU RRAM Model is a SPICE-compatible compact model which describes switching performance for bipolar metal oxide RRAM.
- In principle, this model has no limitations on the size of the RRAM cell.
- The complex process of ion and vacancy migration was simplified into the growth of a single dominant filament that preserved the essential switching physics.
- The size of the tunneling gap (g), which is the distance between the tip of the filament and the opposite electrode, is the primary variable determining device resistance.



Not to Scale

The ReRAM cell in the image shows a **layered structure** consisting of different materials:

- **Top Electrode (TE):**
 - Material: **Titanium Nitride (TiN)**
 - Thickness: **50 nm**
- **Resistive Switching Layers:**
 - **TiO_x Layer:** This is the top resistive switching layer.
 - Thickness: **5 nm**
 - **HfO₂ Layer:** This is the crucial switching medium where the conductive filaments form and dissolve, allowing for the resistive switching between high resistance and low resistance states.
 - Thickness: **1.7, 2.1, and 3.3 nm** (varied depending on the model)
- **Bottom Electrode (BE):**
 - Material: **Platinum (Pt)**
 - Thickness: **50 nm**

- **Electrode Materials**

- TiN: High conductivity, compatibility with CMOS processes, and resistance to oxidation.
- Pt: Excellent conductivity, inert nature, and good adhesion to the switching layer.

- **HfO₂ Layer**

- Thinner layers: Faster switching, lower power, but may have reduced endurance.
- Thicker layers: Improved endurance, but slower switching and higher power consumption.
- **Thickness of the HfO₂ layer be optimized for specific ReRAM applications**
 - ✓ For high-speed applications: Thinner layers.
 - ✓ For high-endurance applications: Thicker layers.
 - ✓ For energy-efficient applications: Carefully balance switching speed and power consumption.

- **TiO_x Layer**

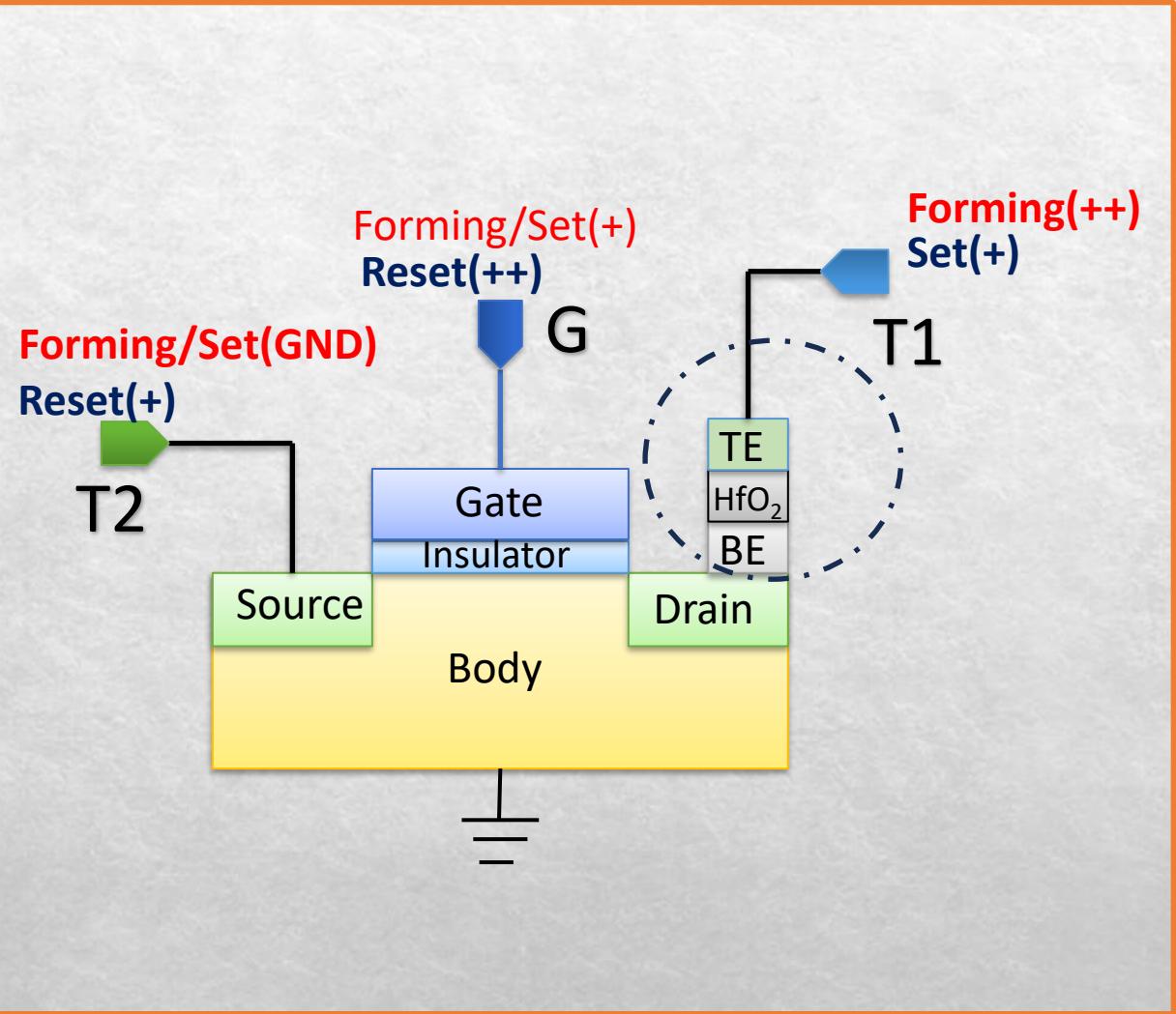
- Acts as a buffer layer, improving filament formation and stability.
- Can influence the SET/RESET voltage and current requirements.
- Can enhance the endurance and reliability of the device.

- **Platinum (Pt)**

- Its excellent conductivity ensures efficient current flow.
- Its inert nature prevents unwanted reactions with the switching layer.
- Its stability under various conditions contributes to device reliability.

- **What are the challenges in selecting suitable electrode materials for ReRAM?**

- Compatibility with the switching layer
- Resistance to diffusion and intermixing
- Long-term stability under electrical stress



Forming(++)
Set(+)

Forming/Set(GND)
Reset(+)

Forming/Set(+)
Reset(++)

G

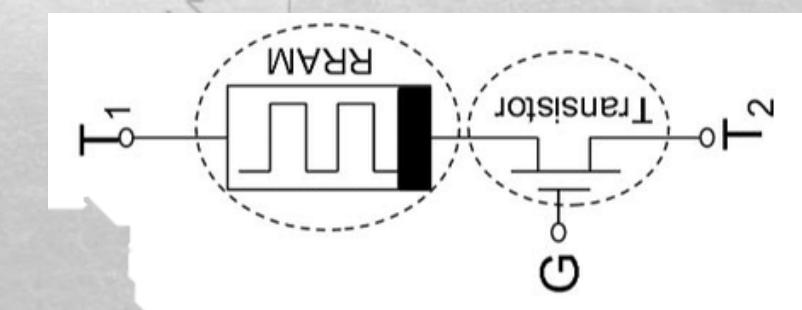
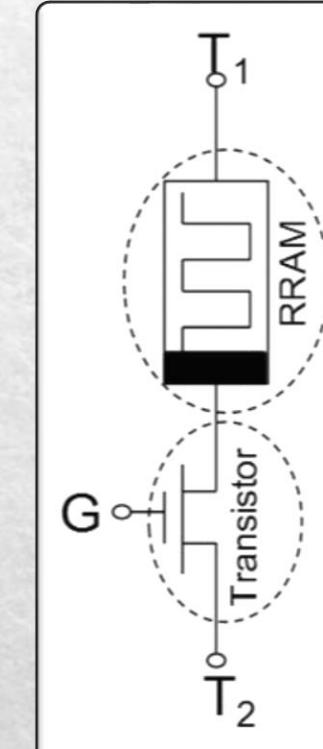
T2

Source

Body

—

Drain



Schematic representation of the 1T1R configuration

Components:

- **Top Electrode (TE):** The upper terminal where voltage is applied.
- **Gate (G):** A control terminal that can influence the RRAM's behavior.
- **Insulator:** A layer that separates the conductive layers.
- **HfO₂:** A common material used as the resistive switching layer.
- **Bottom Electrode (BE):** The lower terminal where voltage is applied.
- **Source and Drain:** Terminals for connecting the RRAM to external circuitry.
- **Body:** The substrate on which the device is fabricated.

Reset to Set Operation

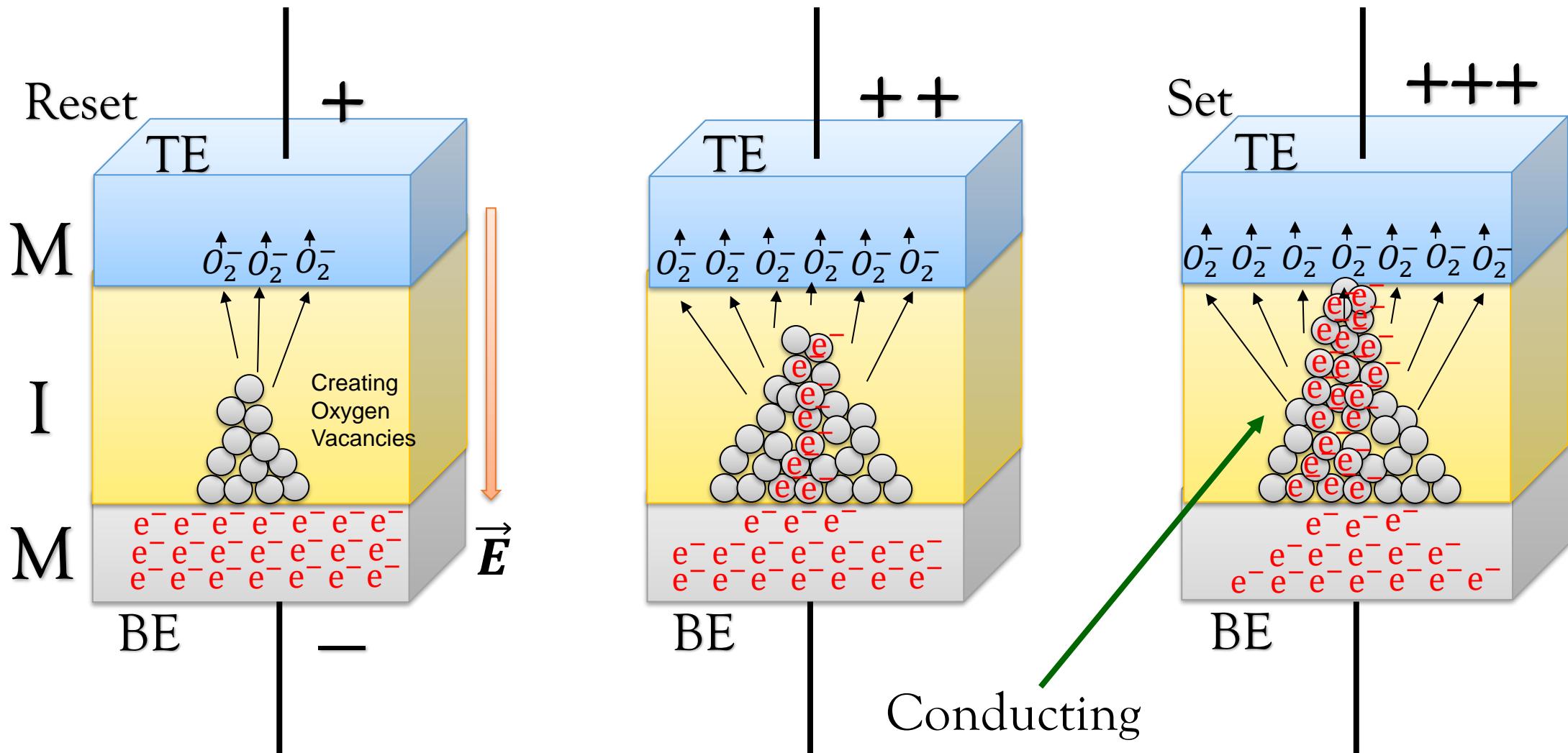
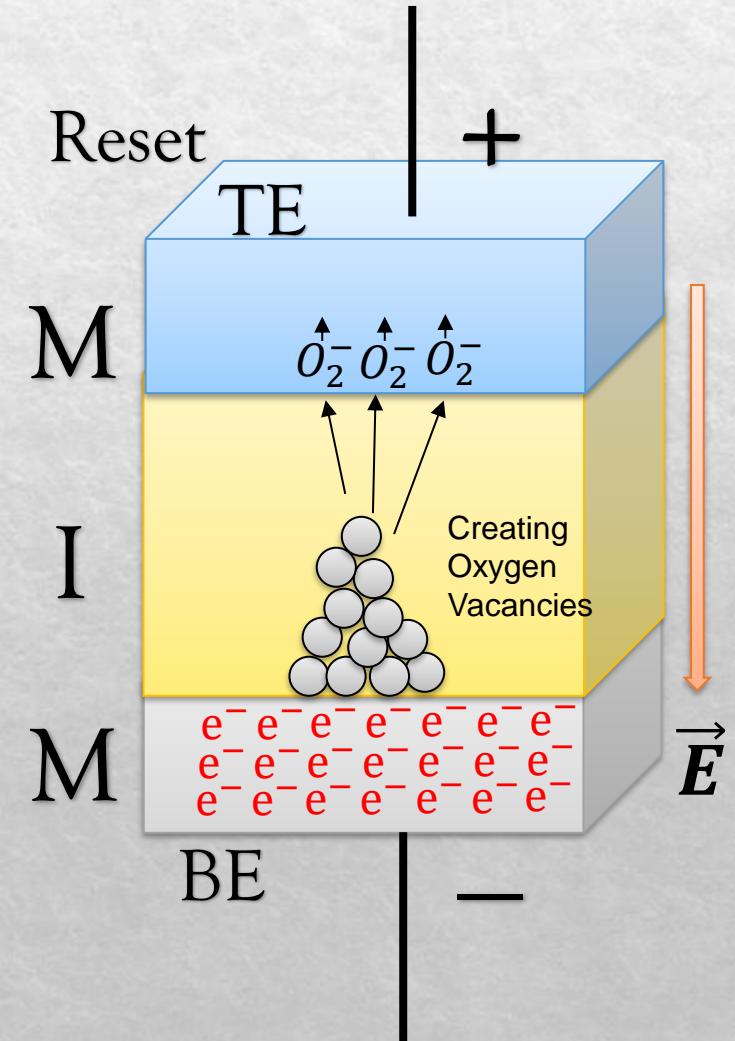


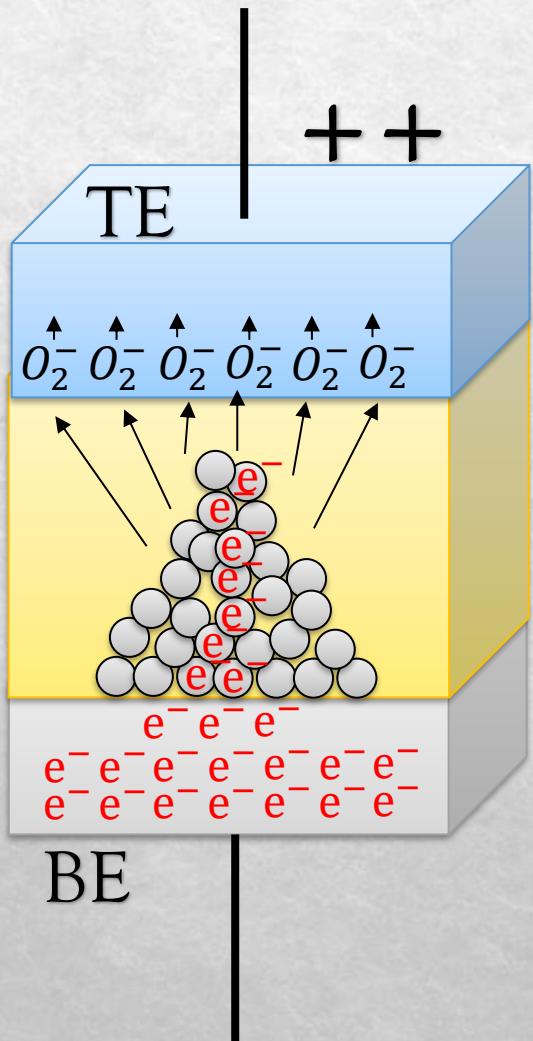
Fig. It shows how the conductive filament forms within the **metal-insulator-metal (MIM)** structure.

The three main steps are **RESET**, **transition (Reset to Set)**, and **SET**, demonstrating the **formation** of conductive filaments due to the movement of **oxygen vacancies** and **electrons**.

1. RESET Operation in ReRAM

- **High Resistance State (HRS):** The ReRAM device is in a non-conductive state.
- **Voltage Application:** A positive voltage is applied to the top electrode (TE) and a negative voltage to the bottom electrode (BE).
- **Oxygen Ion Migration:** Oxygen ions (O_2^-) migrate towards the top electrode (TE).
- **Oxygen Vacancy Formation:** This migration creates oxygen vacancies (V_o) in the insulating layer.
- **Electron Depletion:** Since the filament is broken, the number of free electrons is minimal, causing high resistance. The device remains in HRS after the reset.



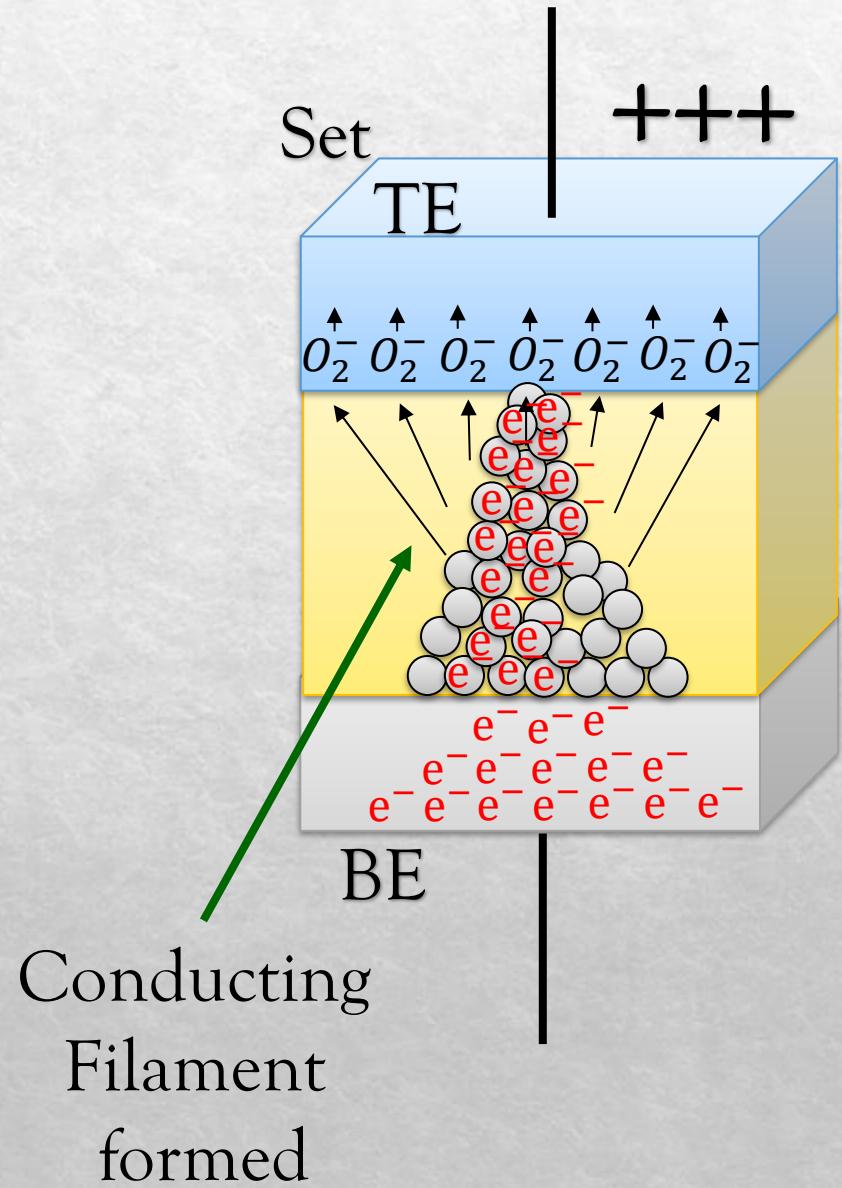


2. Transition from RESET to SET in ReRAM

- **Increased Voltage:** A higher positive voltage is applied to the top electrode (TE) and bottom electrode (BE).
- **Electric Field:** The increased electric field pushes electrons from the bottom electrode (BE) towards the top electrode (TE).
- **Oxygen Vacancy Migration:** Oxygen vacancies (V_o) start migrating downward.
- **Filament Reconstruction:** Oxygen vacancies and electrons begin to **recombine** in the region between the BE and TE, and the filament starts to form again.

3. SET Operation (Low Resistance State - LRS):

- **Complete Filament Formation:** A further increase in voltage creates enough energy to fully form a **conductive filament** between the top electrode (TE) and bottom electrode (BE). This filament is composed of **oxygen vacancies** and **free electrons**, providing a **low resistance path** through the device.
- **Conducting Filament:** The conductive filament allows for efficient current flow, switching the device into a **low resistance state (LRS)**.
- **Oxygen Vacancies and Electrons:** The oxygen vacancies now align and bond with the available electrons to complete the conductive path.
- This is what effectively "programs" the ReRAM cell to LRS.



Set to Reset Operation

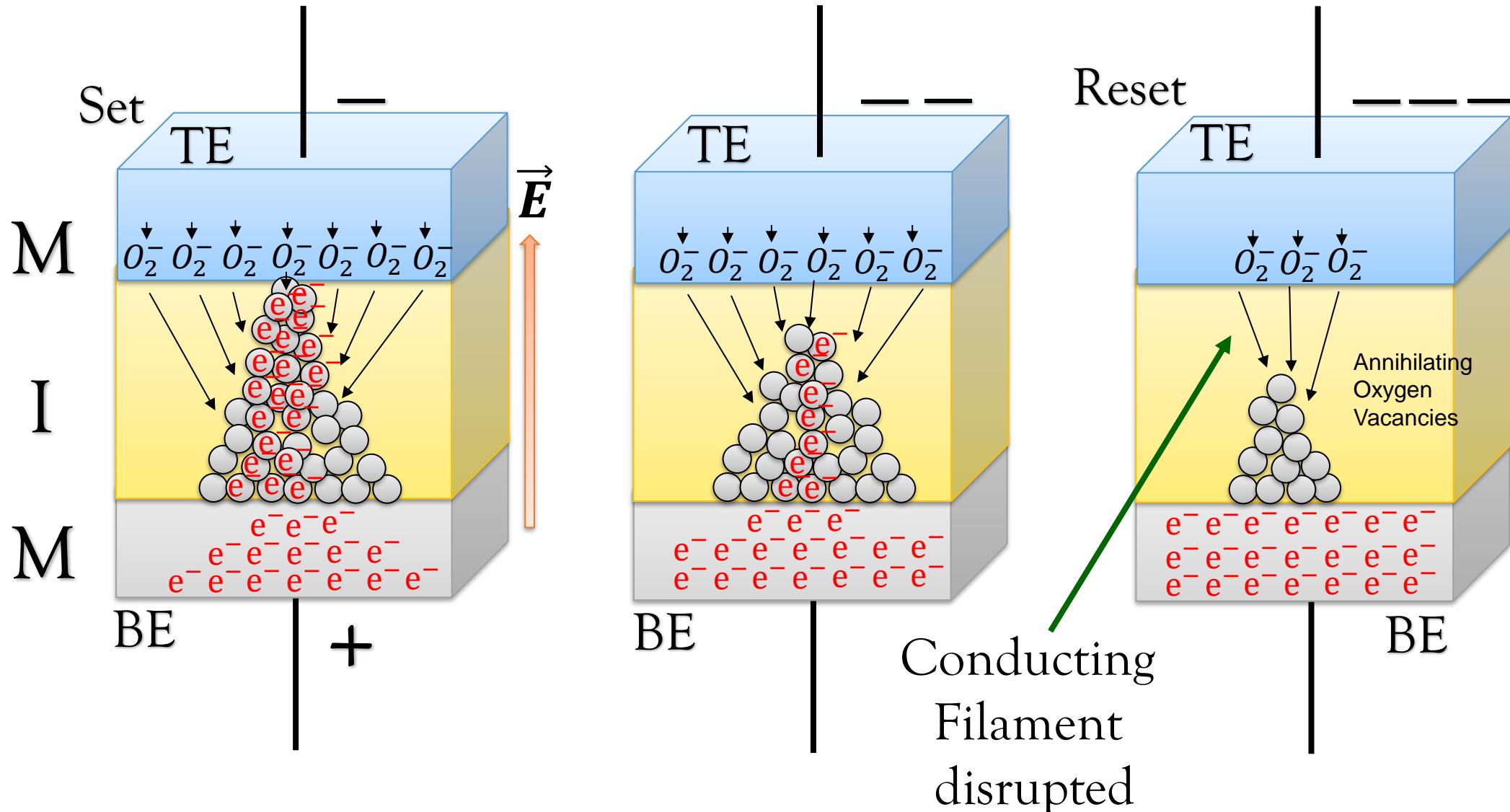
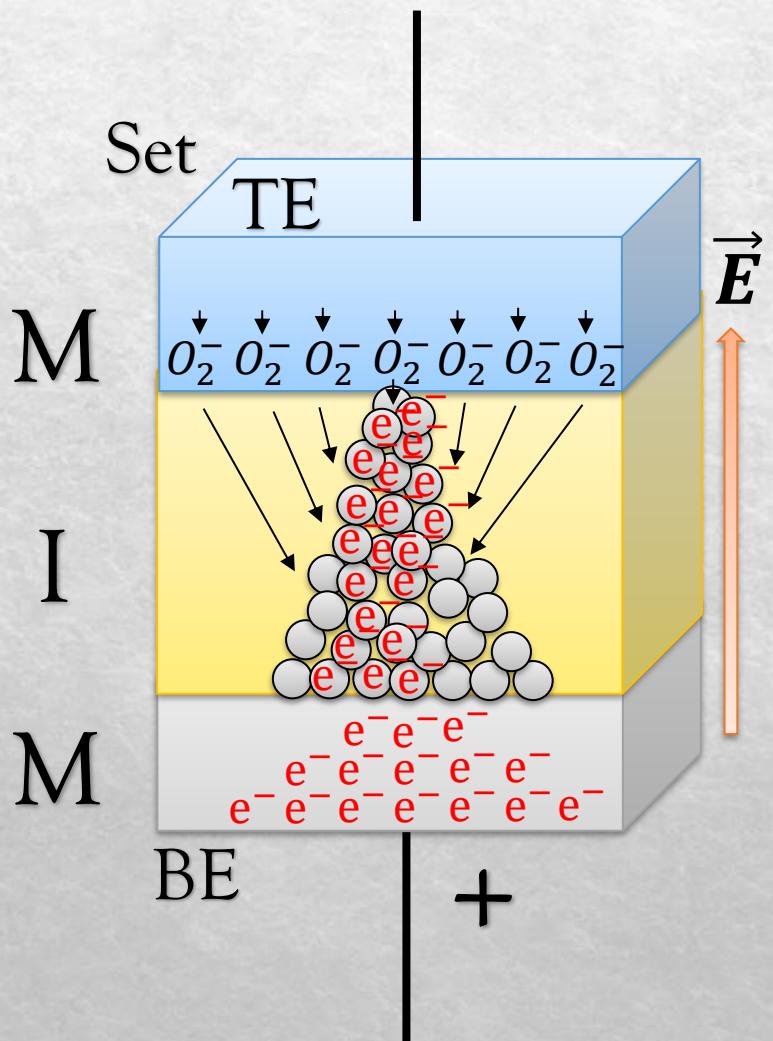


Fig. It shows how the conductive filament disrupted within the **metal-insulator-metal (MIM)** structure.



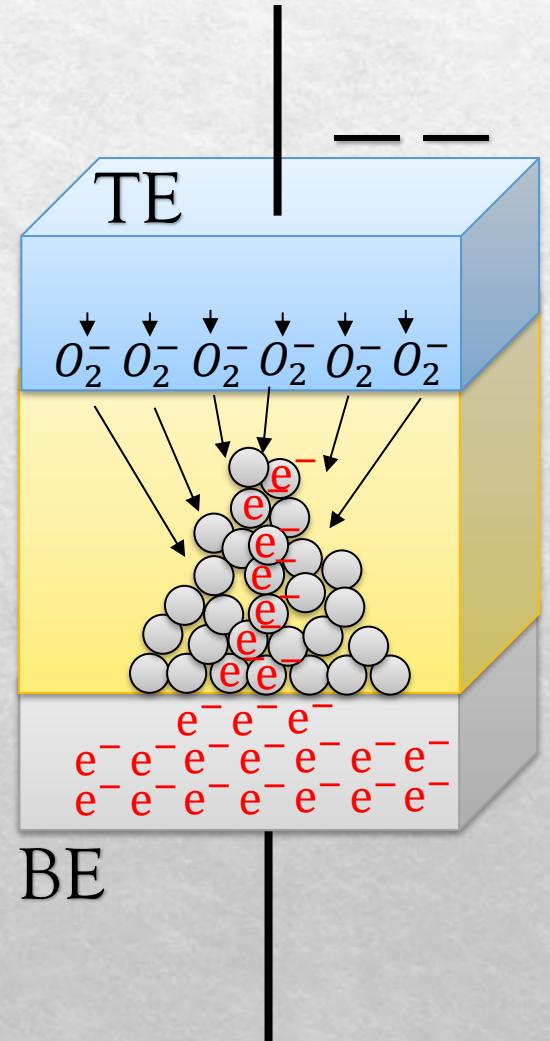
The three main steps: **SET (Low Resistance State)**, **transition (Set to Reset)**, and **RESET (High Resistance State)**. This explains the disruption of the conductive filament due to the movement of **oxygen ions (O^{2-})** and **electrons**.

1. SET Operation in ReRAM

- **Low Resistance State (LRS):** The ReRAM cell is in a conductive state.
- **Conductive Filament:** A filament composed of oxygen vacancies (Vo) and free electrons is formed between the top electrode (TE) and the bottom electrode (BE).
- **Voltage Application:** A negative voltage is applied to the top electrode (TE), and a positive voltage to the bottom electrode (BE).
- **Data Storage:** The LRS represents the programmed state, where the memory cell stores the binary data "1."

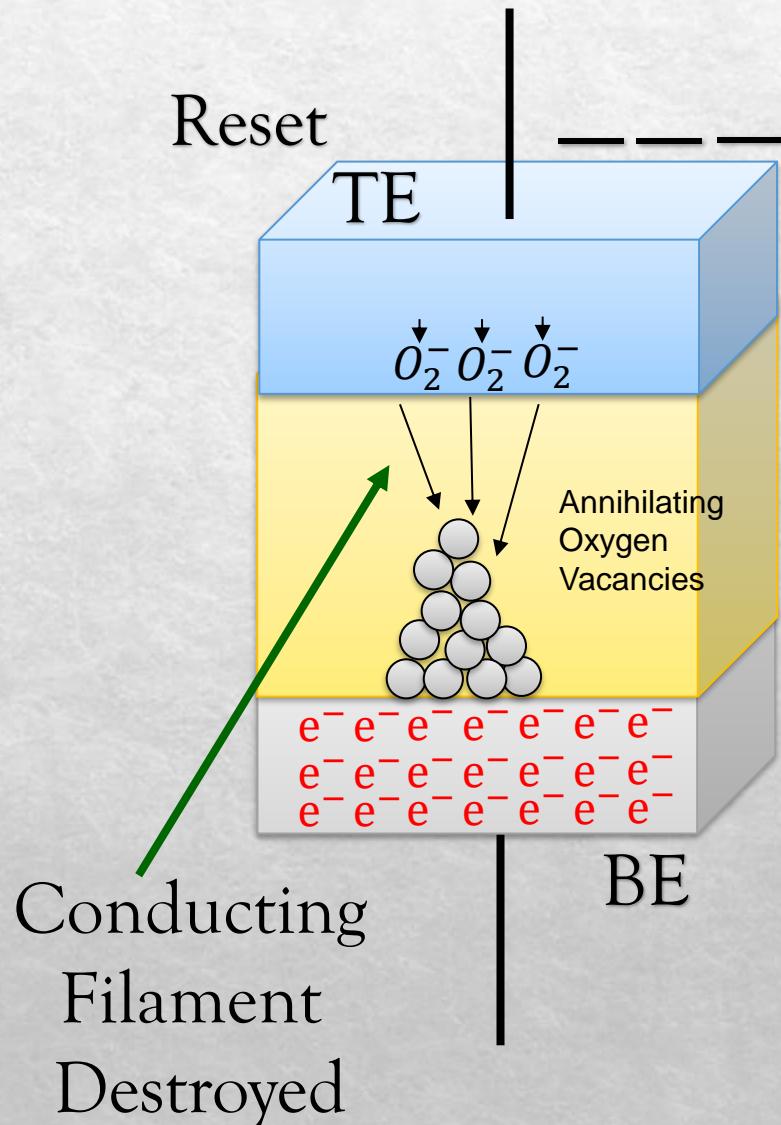
2. Transition from SET to RESET in ReRAM

- **Reverse Polarity Voltage:** A reverse polarity voltage is applied to the top electrode (TE) and bottom electrode (BE).
- **Electric Field:** The reverse voltage creates an electric field that drives oxygen ions (O_2^-) back into the conductive filament region.
- **Filament Disruption:** Oxygen ions (O_2^-) combine with oxygen vacancies (V_O), reducing the number of free electrons and weakening the conductive path.



3. RESET Operation (High Resistance State - HRS):

- In the RESET state, the conductive filament is **completely destroyed**, and the device transitions to a **high resistance state (HRS)**.
- **Filament Breakdown:** The annihilation of oxygen vacancies continues until the conductive filament is fully broken, making the path between the top and bottom electrodes highly resistive.
- **No Current Flow:** With no conductive filament, the current flow through the memory cell is minimal, resulting in a high resistance state.
- This is what effectively "programs" the ReRAM cell to HRS.



Summarized Phenomenon:

- The **RESET process** disrupts the conductive filament by causing oxygen vacancies to move away from the filament area, resulting in **high resistance**.
- The **SET process** reforms the conductive filament by driving oxygen vacancies and electrons back into the filament region, resulting in **low resistance**.
- The switching between **HRS and LRS** through the control of oxygen vacancies and filament formation is what enables the non-volatile memory behavior of ReRAM.

This **bipolar resistive switching** is typical for many **oxide-based ReRAM** devices, including those using HfO₂, and it allows data to be stored by manipulating the resistance state of the memory cell.

Read and Write Operations in ReRAM with Bit-line, Word-line, and Source Line

1. Write Operation (SET/RESET):

In ReRAM, writing can involve either:

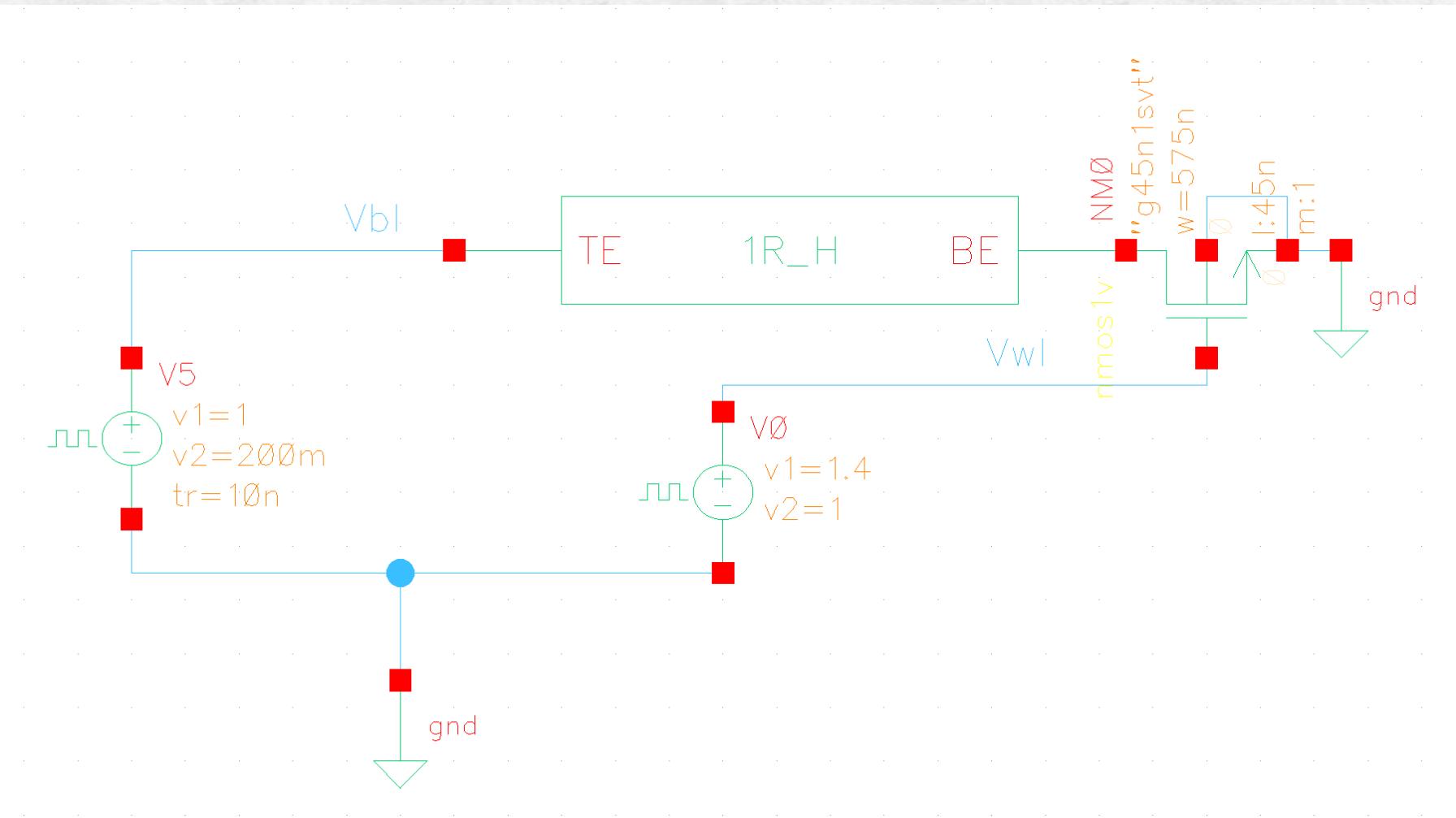
- **SET operation:** Changing the resistance from a high resistance state (HRS) to a low resistance state (LRS), which corresponds to writing a "1".
- **RESET operation:** Changing the resistance from a low resistance state (LRS) to a high resistance state (HRS), which corresponds to writing a "0".

The voltages applied to the **bit-line**, **word-line**, and **source line** control whether a SET or RESET operation occurs.

Write Operation (SET - Write "1"):

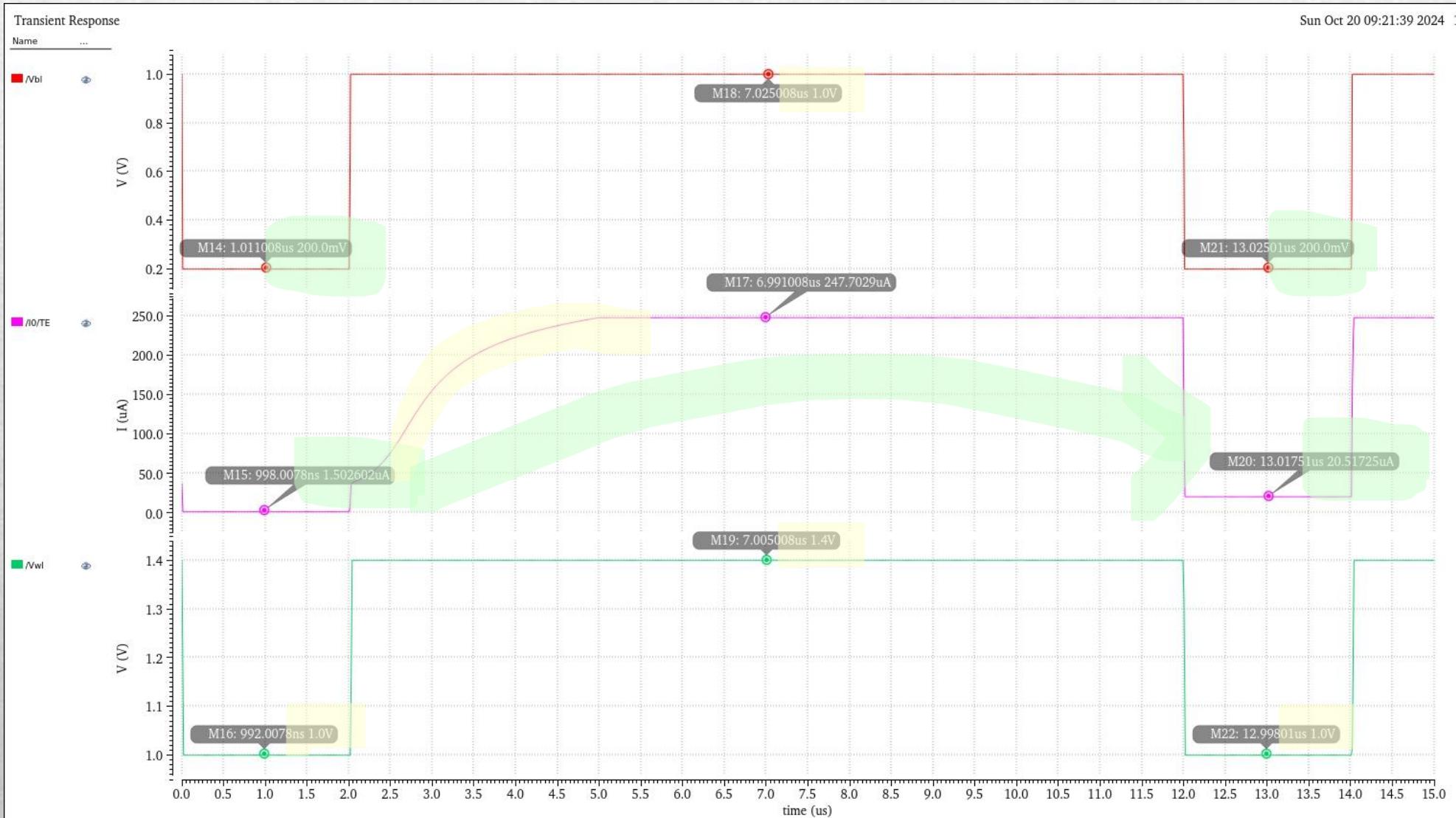
- **Bit-line (BL):** A **positive voltage (+)** is applied to the bit-line (drain of the transistor), high enough to trigger the formation of a conductive filament in the ReRAM cell.
- **Word-line (WL):** A **positive voltage** is applied to the **gate (G)** of the transistor (T1 or T2), turning it on and allowing current to flow from the bit-line to the source line.
- **Source Line (SL):** The source line is grounded (GND) or set to a low voltage to create a potential difference that causes the ions (such as oxygen vacancies or metal ions) to move and form a conductive filament.
- **Result:** The resistance of the ReRAM cell switches to **Low Resistance State (LRS)**, storing a "1". This is known as the **SET operation**.

SET - Write "1"



SET - Write "1"

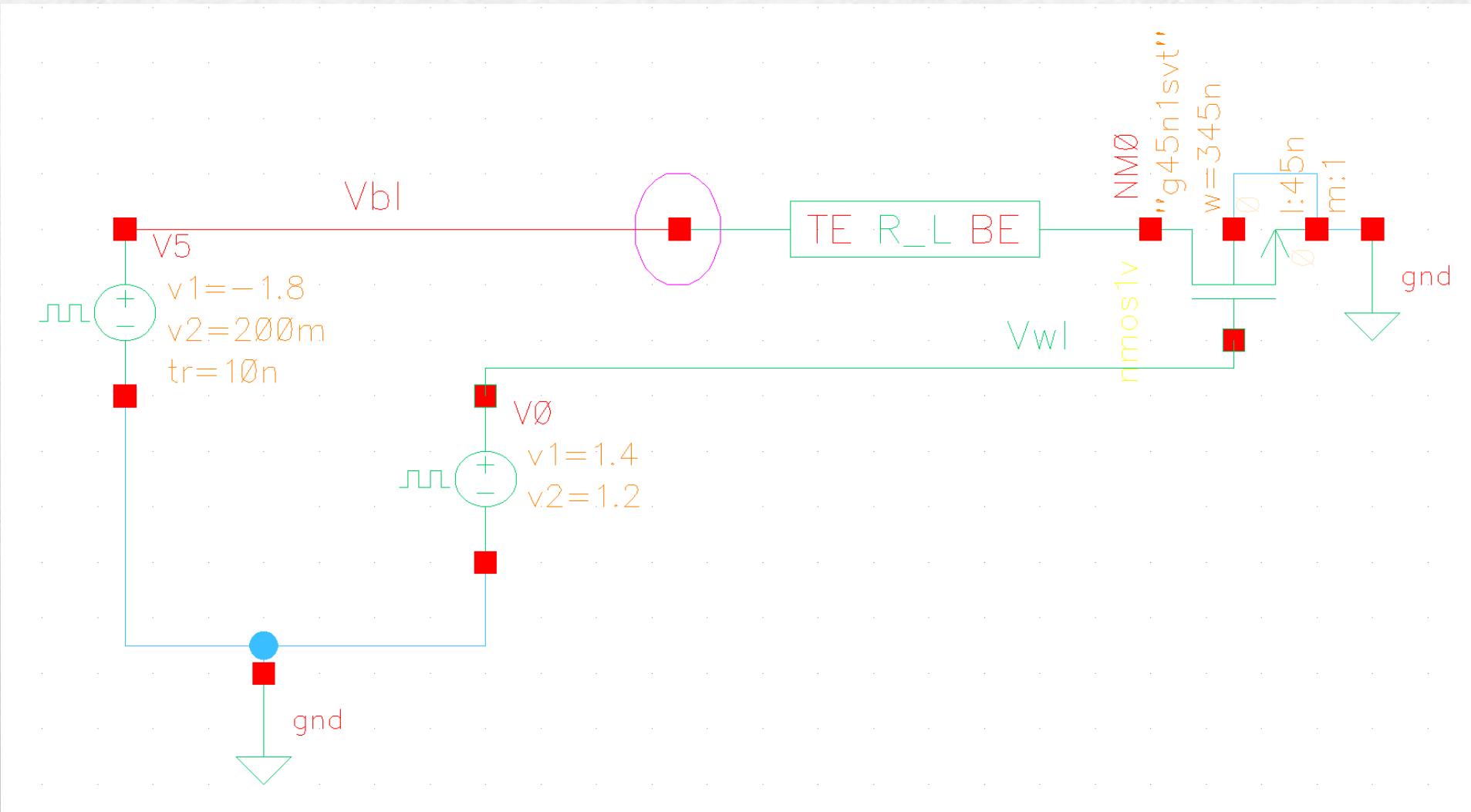
Time (μs)	Word Line Voltage (V _{wl})	Bit Line Voltage (V _{bl})	Source Line	Operation	Current μA	Resistance State / Value KΩ	Description
0 - 2	1 V	200 mV	Gnd	Initial Read	~1.5	~133.3 (HRS)	Safe sensing of the ReRAM's resistance without altering its state.
2-12	1.4 V	1-1.3 V	Gnd	Set Operation	~250	LRS	Applying 1 V to the Bit line initiates the set process, forming a conductive filament (LRS).
12-14	1 V	200 mV	Gnd	Final Read	~20.5	~9.76 (LRS)	Confirms that the Set operation took place in the ReRAM cell without disturbing the state.



Write Operation (RESET - Write "0"):

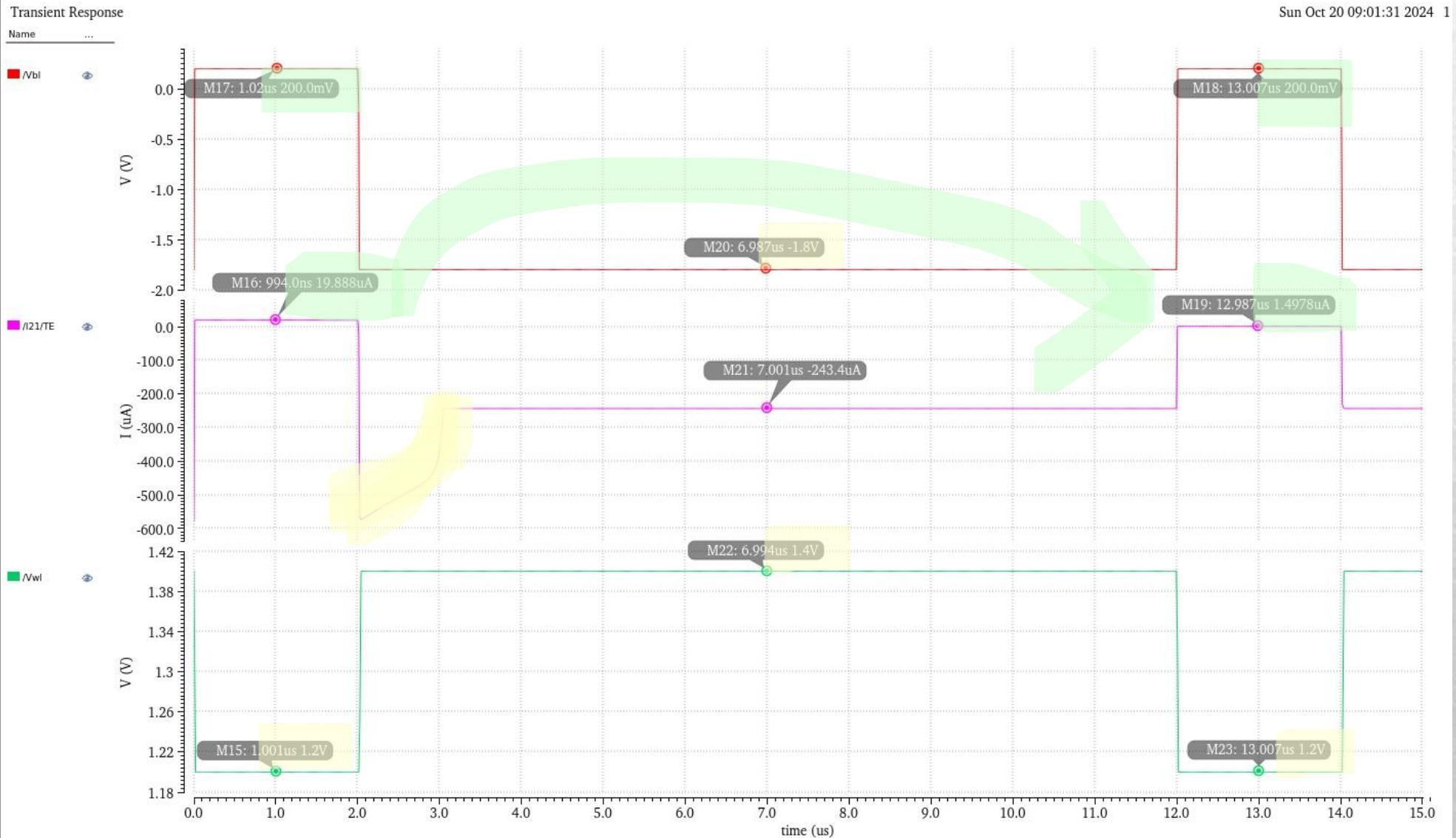
- **Bitline (BL):** A **higher positive voltage (++)** is applied to the bitline compared to the SET operation. This higher voltage is sufficient to rupture the previously formed conductive filament.
- **Wordline (WL):** Again, a **positive voltage** is applied to the gate (WL), enabling the transistor and allowing current to flow.
- **Source Line (SL):** The source line is grounded (GND) or set to a slightly lower voltage to allow current flow.
- **Result:** The conductive filament in the ReRAM cell breaks, switching the cell back to the **High Resistance State (HRS)**, which represents a "0". This is called the **RESET operation**.

RESET - Write “0”



RESET - Write “0”

Time (μs)	Word Line Voltage (V _{wl})	Bit Line Voltage (V _{bl})	Source Line	Operation	Current μA	Resistance State / Value KΩ	Description
0 - 2	1 V	200 mV	Gnd	Initial Read	~20.5	~9.76 (LRS)	Safe sensing of the ReRAM's resistance without altering its state.
2-12	1.4 V	[-1.3,-1.8 V]	Gnd	Reset Operation	~250	HRS	Applying -1.8 V to the Bit line initiates the reset process, disrupting the conductive filament (HRS).
12-14	1 V	200 mV	Gnd	Final Read	~1.5	~133.3 (HRS)	Confirms that the Reset operation took place in the ReRAM cell without disturbing the state.



2. Read Operation:

In the **read operation**, a small voltage is applied across the cell, and the resulting current is measured to determine if the cell is in the high resistance state (HRS, logic "0") or low resistance state (LRS, logic "1"). The key here is to apply a voltage low enough to not disturb the stored data.

- **Bit-line (BL)**: A **small positive voltage** (much smaller than the SET/RESET voltage) is applied to the bit-line to avoid disturbing the cell's resistance state.
- **Word-line (WL)**: A **positive voltage** is applied to the word-line to turn on the transistor, allowing a small current to flow through the ReRAM cell.
- **Source Line (SL)**: The source line is grounded (GND), completing the circuit for the small read current.
- **Result**: The magnitude of the current is measured to determine the resistance of the ReRAM cell:
- **Low resistance (LRS)**: Higher current flows → cell stores a "1".
- **High resistance (HRS)**: Lower current flows → cell stores a "0".

Word Line Voltage (Vwl)	Bit Line Voltage (Vbl)	Source Line	Operation	Description	Resistance State
1V	200mV	Gnd	Read Operation	Bit-line at 200mV and word-line at 1V allows for safe sensing of RRAM's resistance without changing its state.	Unknown (Assumed LRS if no reset operation has occurred)
1.4V	-1.8V	Gnd	Reset Operation	Wordline at 1.4V and bitline at -1.8V create a large potential difference, breaking the conductive filament and switching RRAM to high-resistance state (HRS).	HRS
1V	200mV	Gnd	Read Operation	Again, set to 1V and 200mV, this read operation measures the RRAM resistance to confirm it is in HRS without disturbing the cell's state.	HRS
1.4V	1-1.2V	Gnd	Set Operation	Bit-line at 1.2V and word-line at 1.4V initiate the Set operation, forming a conductive filament and switching RRAM to LRS.	LRS
1V	200mV	Gnd	Read Operation	Again, set to 1V and 200mV, this read operation measures the RRAM resistance to confirm it is in LRS without disturbing the cell's state.	LRS

Operation	Bit-line (BL)	Word-line (WL)	Source Line (SL)	Description
SET (Write "1")	Positive Voltage (+)	Positive Voltage (G)	Ground (GND)	The SET operation forms a conductive filament in the ReRAM material, reducing the resistance (LRS).
RESET (Write "0")	Negative Voltage (--)	Positive Voltage (G)	Ground (GND)	The RESET operation ruptures the filament, increasing the resistance (HRS).
Read	Small Positive Voltage	Positive Voltage (G)	Ground (GND)	A small voltage is applied to the bit-line, and the current is sensed to determine the resistance state (LRS or HRS).

Low Resistance state Code

```
// initial gap distance, gap_ini  
parameter real  
// minimum gap distance, gap_min  
parameter real  
// maximum gap distance, gap_max  
parameter real  
// thermal resistance  
parameter real Rth  
// oxide thickness, thickness  
parameter real tox
```

gap_ini = 0.85e-9 from(0:100e-10);
gap_min= 0.85e-9 from(0:100e-10);
gap_max = 18e-10 from(0:100e-10);
= 1500 from(0:inf);
= 6e-9 from(0:100e-9);

High Resistance state Code

```
// initial gap distance, gap_ini  
parameter real  
// minimum gap distance, gap_min  
parameter real  
// maximum gap distance, gap_max  
parameter real  
// thermal resistance  
parameter real Rth  
// oxide thickness, thickness  
parameter real tox
```

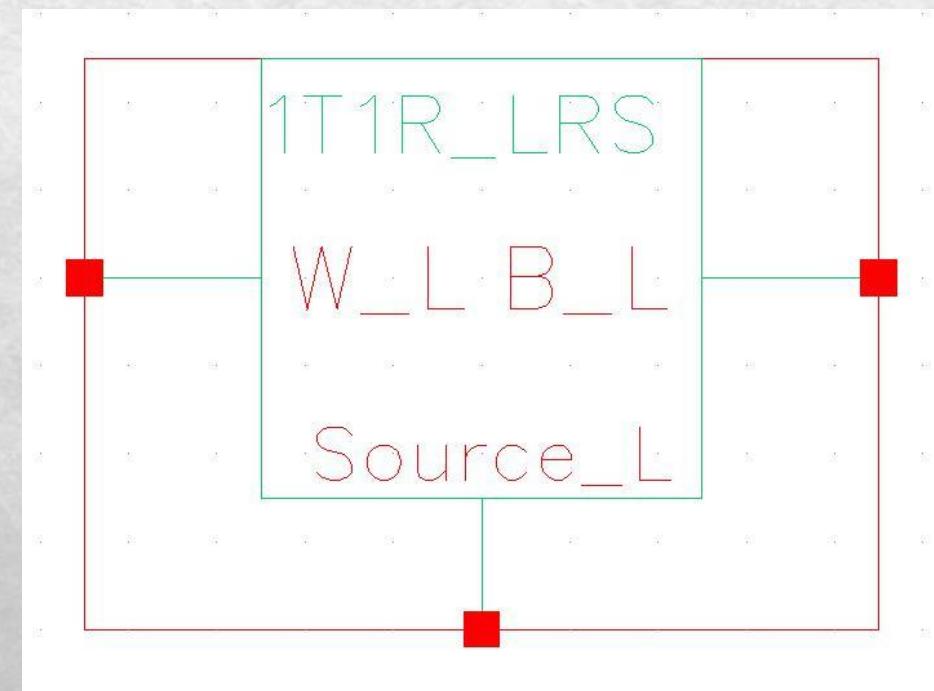
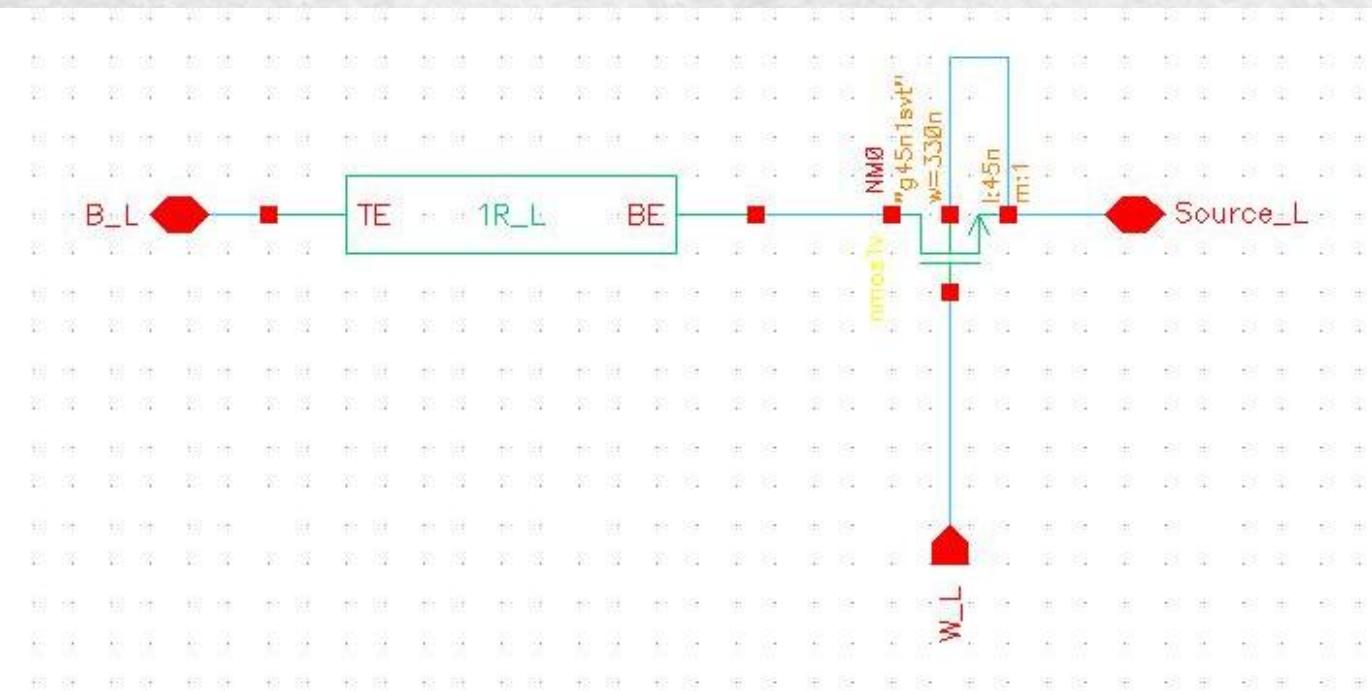
gap_ini= 18e-10 from(0:100e-10);
gap_min= 0.85e-9 from(0:100e-10);
gap_max= 18e-10 from(0:100e-10);
= 1500 from(0:inf);
= 6e-9 from(0:100e-9);



Transistor Sizing
 $L = 45n$
 $W = 330n$

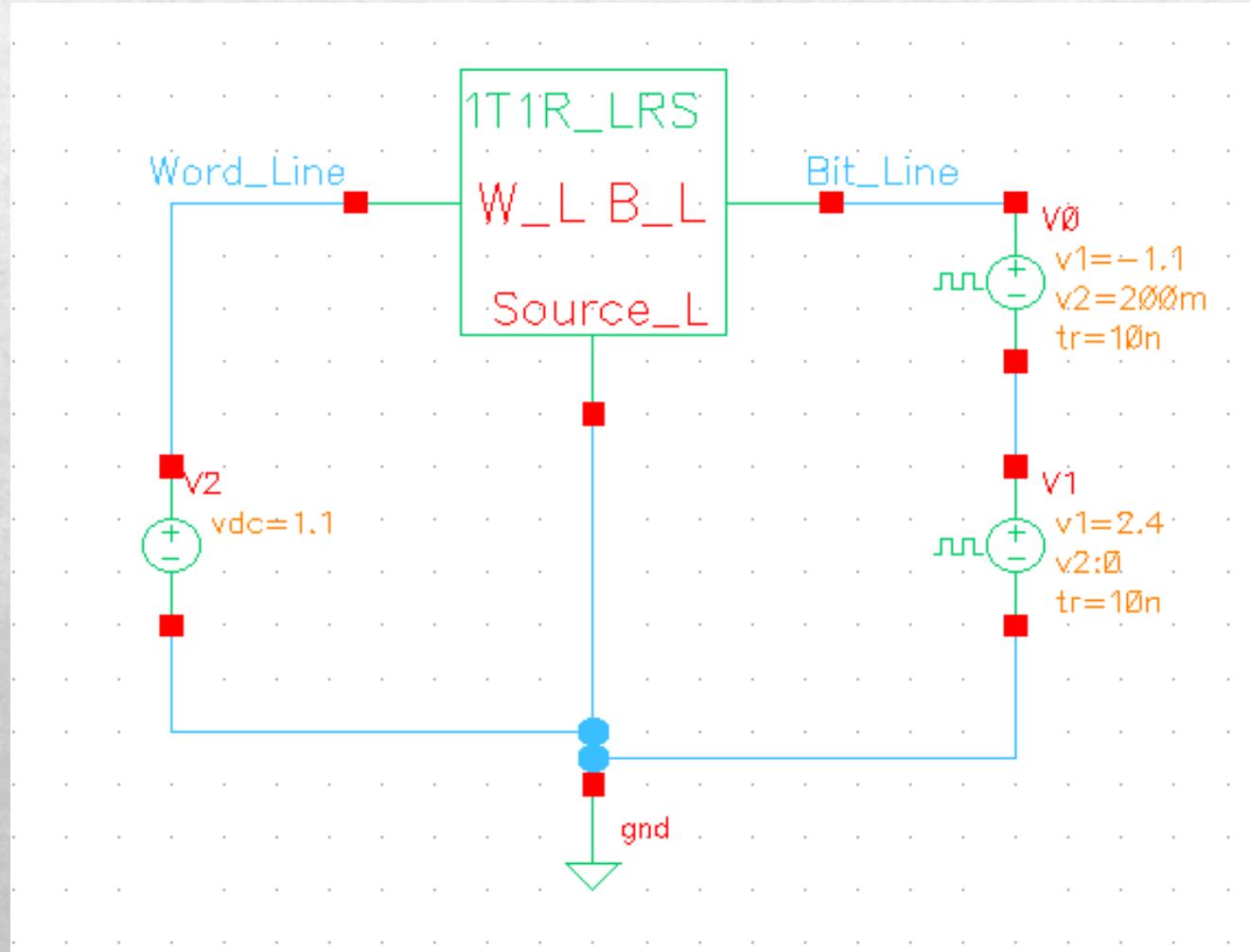


Schematic Diagram of 1T1R-LRS



Schematic Diagram of 1T1R with test voltages

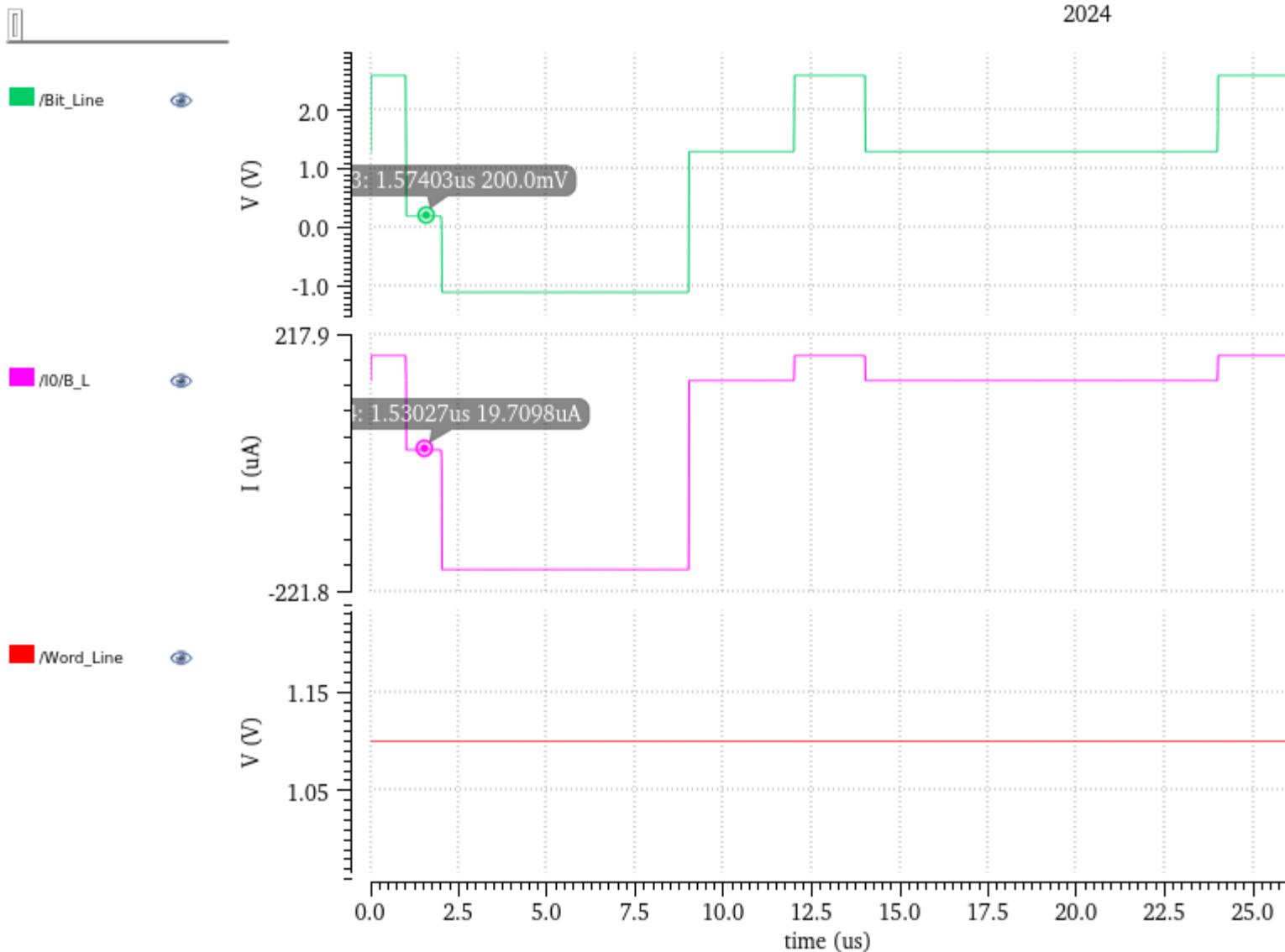
For Testing Low Resistance state



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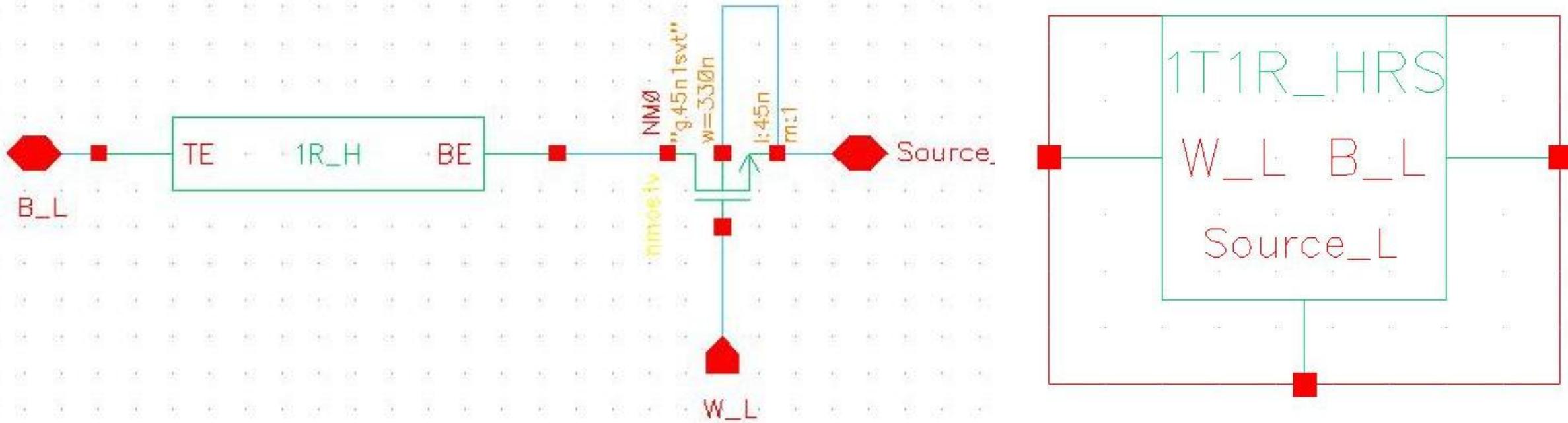


If the current is indeed 1 microampere (1uA) and the voltage is 200 millivolts (200mV), then the resistance can be calculated using Ohm's Law as follows:

$$\begin{aligned}R &= V / I \\R &= 200mV / 19.7uA \\R &= 10,152 \text{ ohms} \\R &= 10.1k \text{ ohms}\end{aligned}$$

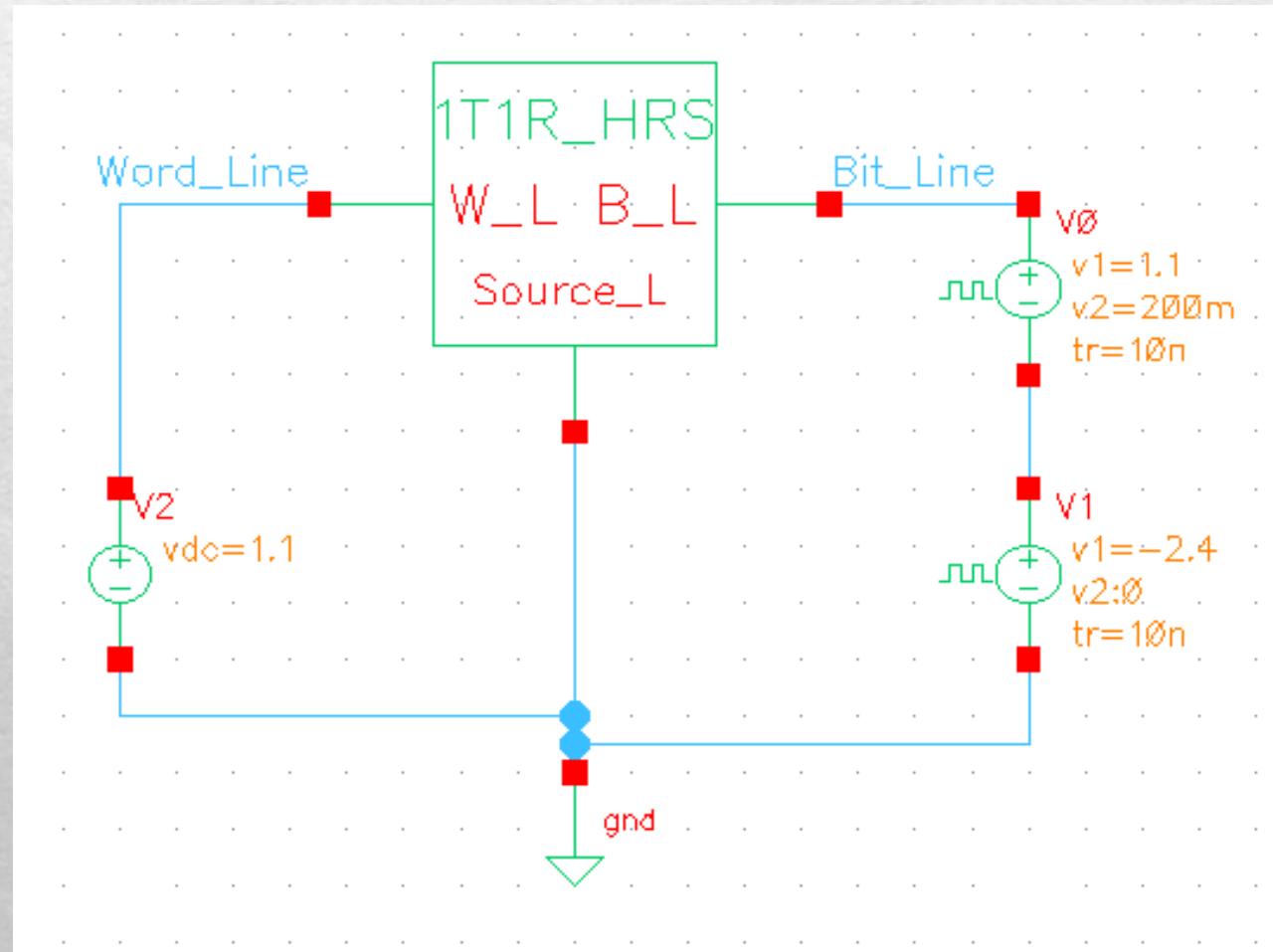
Therefore, with these given values, the resistance is indeed 200k ohms.

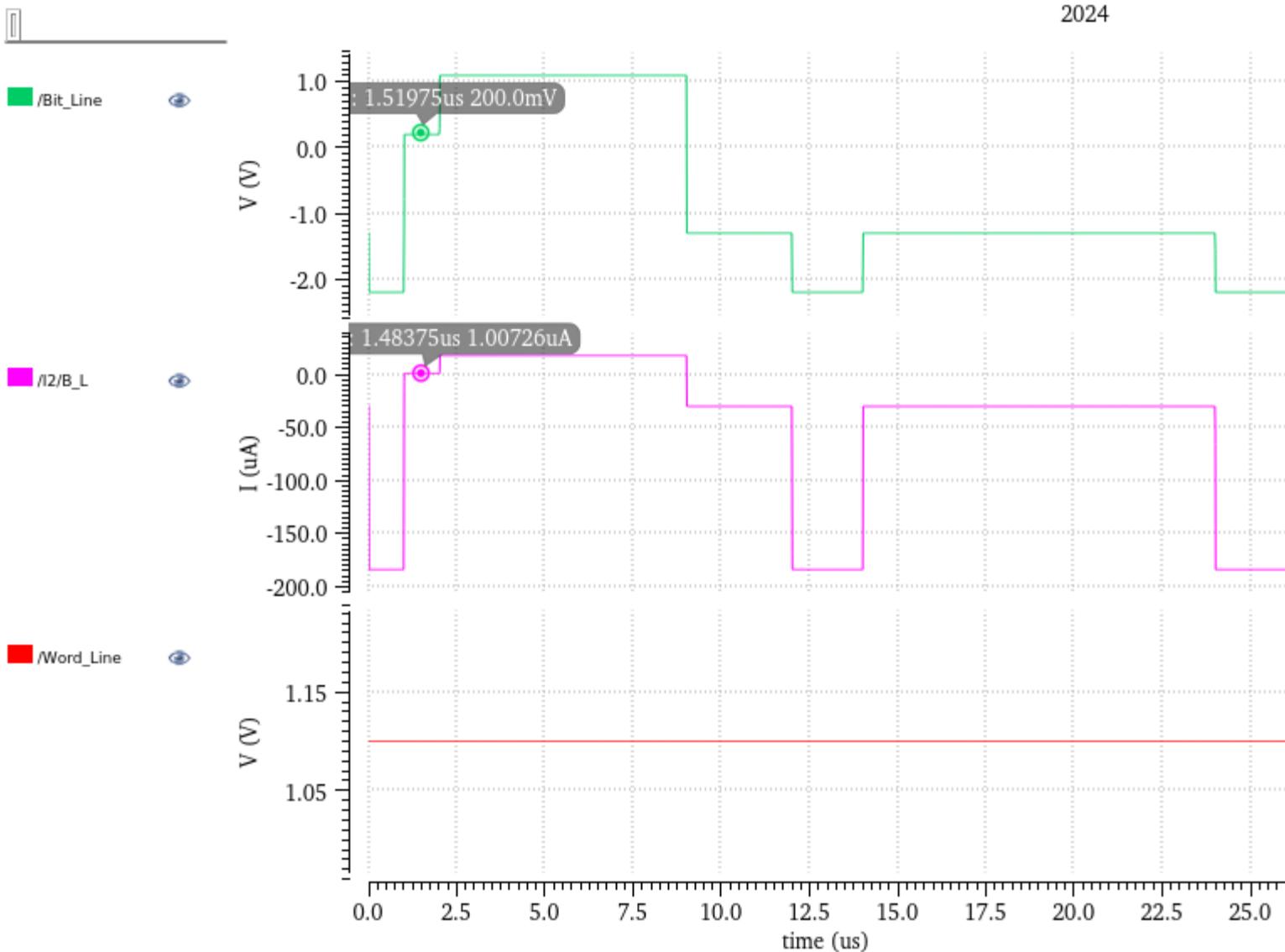
Schematic Diagram of 1T1R-HRS



Schematic Diagram of 1T1R with test voltages

For Testing High Resistance state





If the current is indeed 1 microampere (1uA) and the voltage is 200 millivolts (200mV), then the resistance can be calculated using Ohm's Law as follows:

$$\begin{aligned}R &= V / I \\R &= 200mV / 1uA \\R &= 200,000 \text{ ohms} \\R &= 200k \text{ ohms}\end{aligned}$$

Therefore, with these given values, the resistance is indeed 200k ohms.

Majority Gate Principle

$$M(A, B, C) = AB + BC + AC$$

- ❑ **Definition:** A majority gate is a digital logic gate that produces a high output (1) if the majority of its inputs are high, and a low output (0) otherwise.
- ❑ **Inputs:** Typically, a majority gate has three inputs, but it can also have more.
- ❑ **Output:** The output is determined by the majority of the input values. $MAJ(a,b,c)=a \cdot b + b \cdot c + a \cdot c$ for Boolean variables a, b, and c.
- ✓ **Applications:** Majority gates are used in various digital circuits, including: **Error detection and correction, Voting circuits, Sequential circuits**

MAJORITY LOGIC AS A LOGIC PRIMITIVE

Why?

In-Memory Computation:

- **Proposed Gate:** A majority gate structure is proposed for parallel processing within memory arrays.
- **Majority logic primitive** was used for addition since it is better than NAND/NOR/IMPLY primitives.
- **NOT Gate Implementation:** A method is also proposed for implementing a NOT gate in memory.
- **Functional Completeness:** Majority logic combined with NOT is functionally complete, enabling the expression of any Boolean logic.

In this manner, an in-memory multiplier of $O(n \cdot \log(n))$ latency is achieved which outperforms all reported in-memory multipliers.

Majority gate: Operating principle

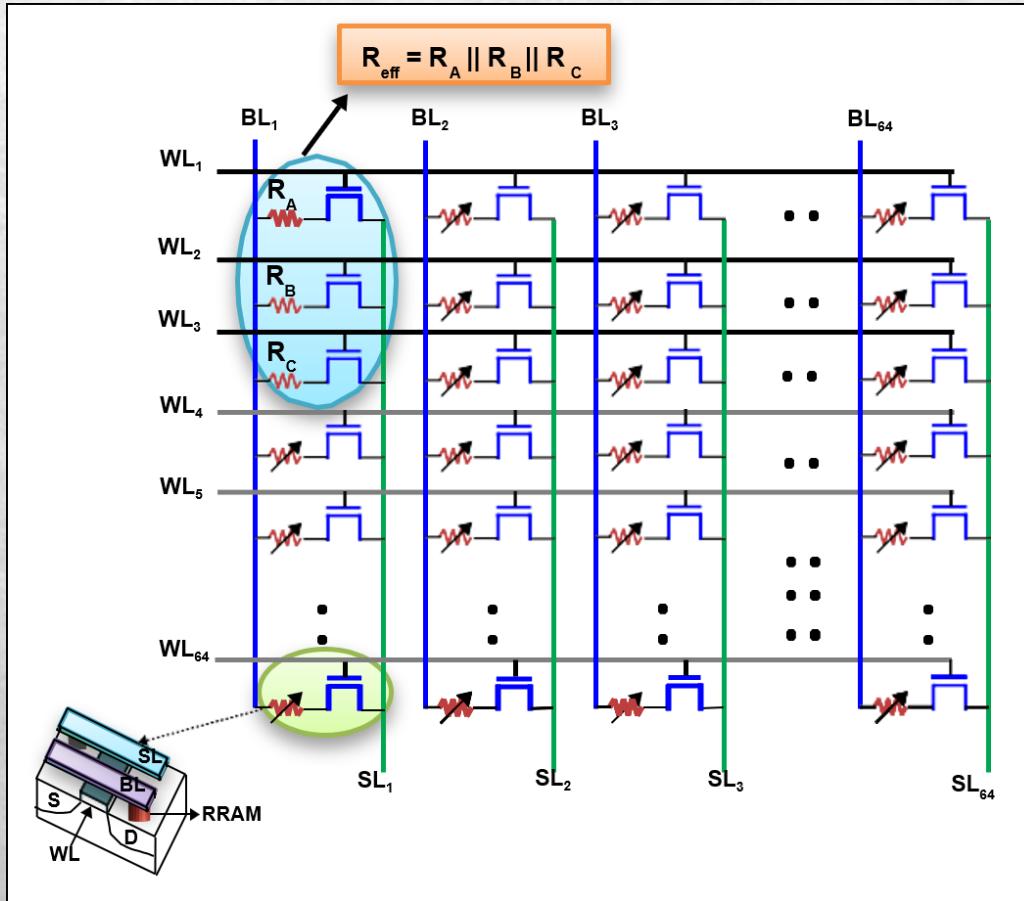


Fig. : When three rows are activated (WL1-3) simultaneously in a 1T-1R array, the resistances of the three ReRAM devices are in parallel.

An ‘in-memory’ majority gate can be implemented by accurately sensing the effective resistance R_{eff} .

Circuit Diagram:

The diagram depicts a circuit that implements a majority gate using ReRAM cells and a Sense Amplifier (SA).

Operation:

1. Input: The input signals a, b, and c are applied to the ReRAM cells.

2. Read Operation: When the IREAD signal becomes active, the SA reads the effective resistance of the ReRAM cells.

3. Majority Calculation: The SA determines whether the majority of the ReRAM cells have a high or low resistance.

4. Output: The output Q is set to 1 if the majority of the ReRAM cells have a high resistance, indicating that the majority of the input signals are 1. Otherwise, Q is set to 0.

Majority Gate (as a READ Operation)

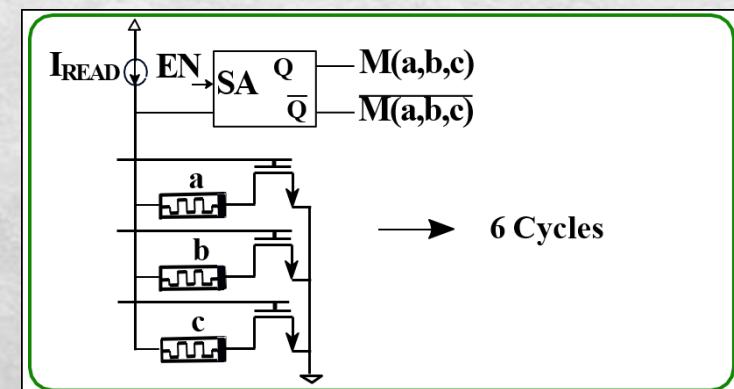
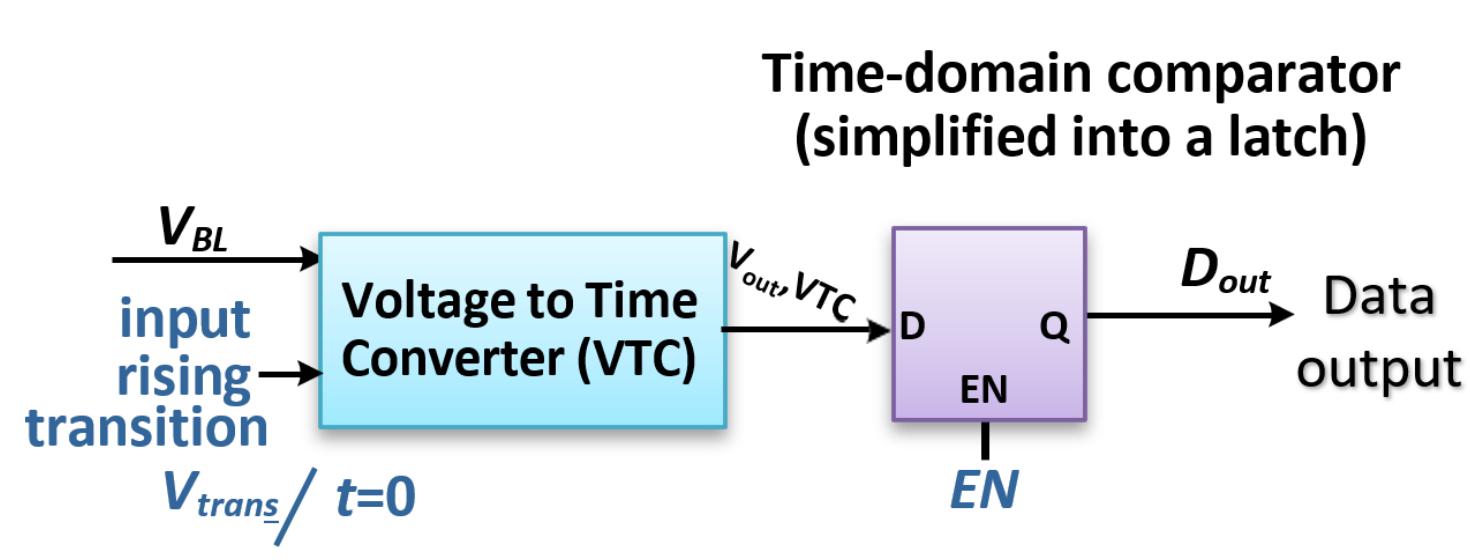


TABLE : Precisely sensing R_{eff} results in majority: Logic '0' is *LRS* (10 k Ω) and logic '1' is *HRS* (133.3 k Ω)

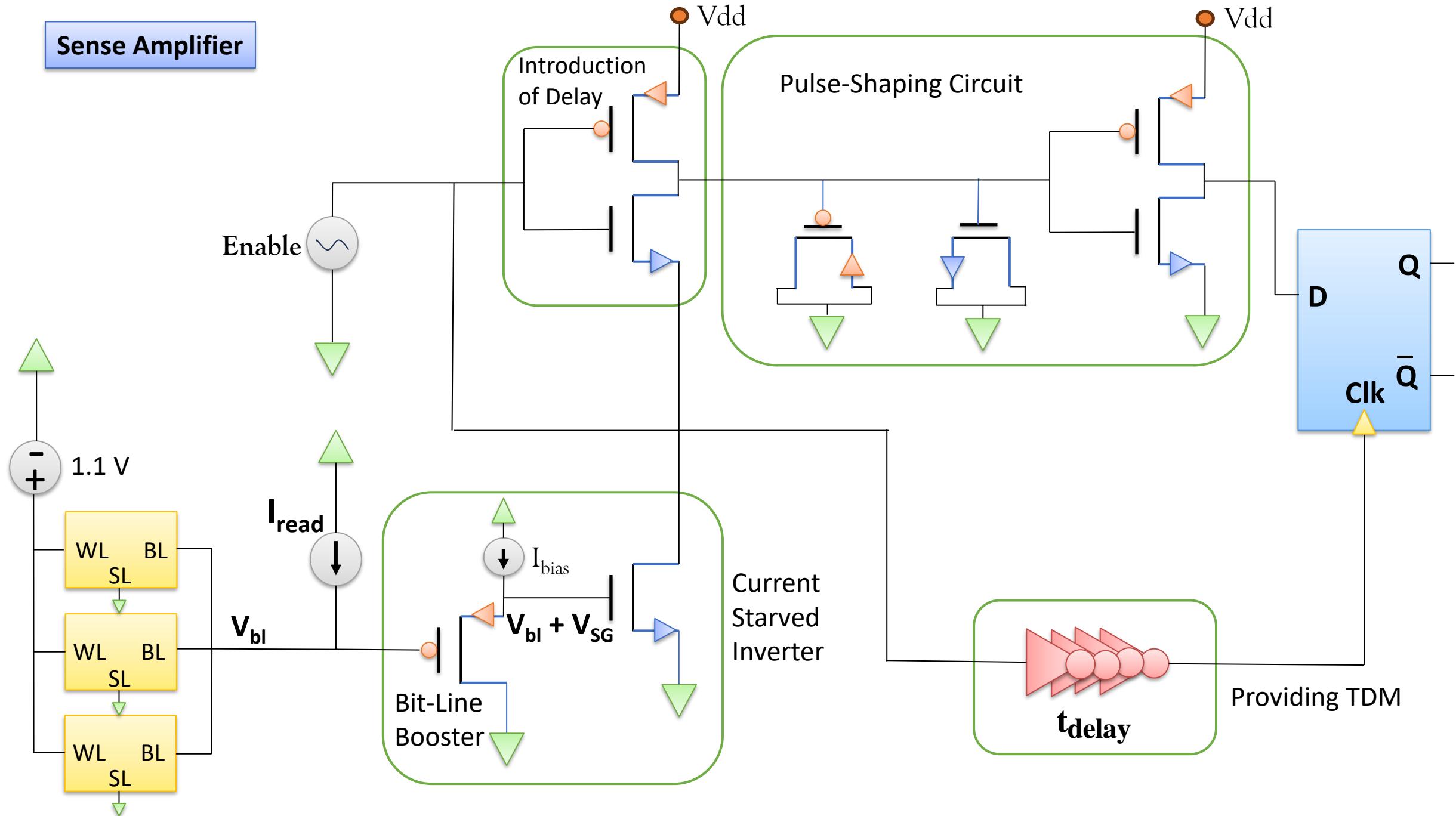
A	B	C	$M_3(A, B, C)$	R_{eff}	R_{eff}
0	0	0	0	$\frac{LRS}{3}$	3.3 k Ω
0	0	1	0	$\frac{HRS \cdot LRS}{LRS + 2 \cdot HRS}$	4.8 k Ω
0	1	0	0	$\frac{HRS \cdot LRS}{LRS + 2 \cdot HRS}$	4.8 k Ω
0	1	1	1	$\frac{HRS \cdot LRS}{HRS + 2 \cdot LRS}$	8.7 k Ω
1	0	0	0	$\frac{HRS \cdot LRS}{LRS + 2 \cdot HRS}$	4.8 k Ω
1	0	1	1	$\frac{HRS \cdot LRS}{HRS + 2 \cdot LRS}$	8.7 k Ω
1	1	0	1	$\frac{HRS \cdot LRS}{HRS + 2 \cdot LRS}$	8.7 k Ω
1	1	1	1	$\frac{HRS}{3}$	44.4 k Ω

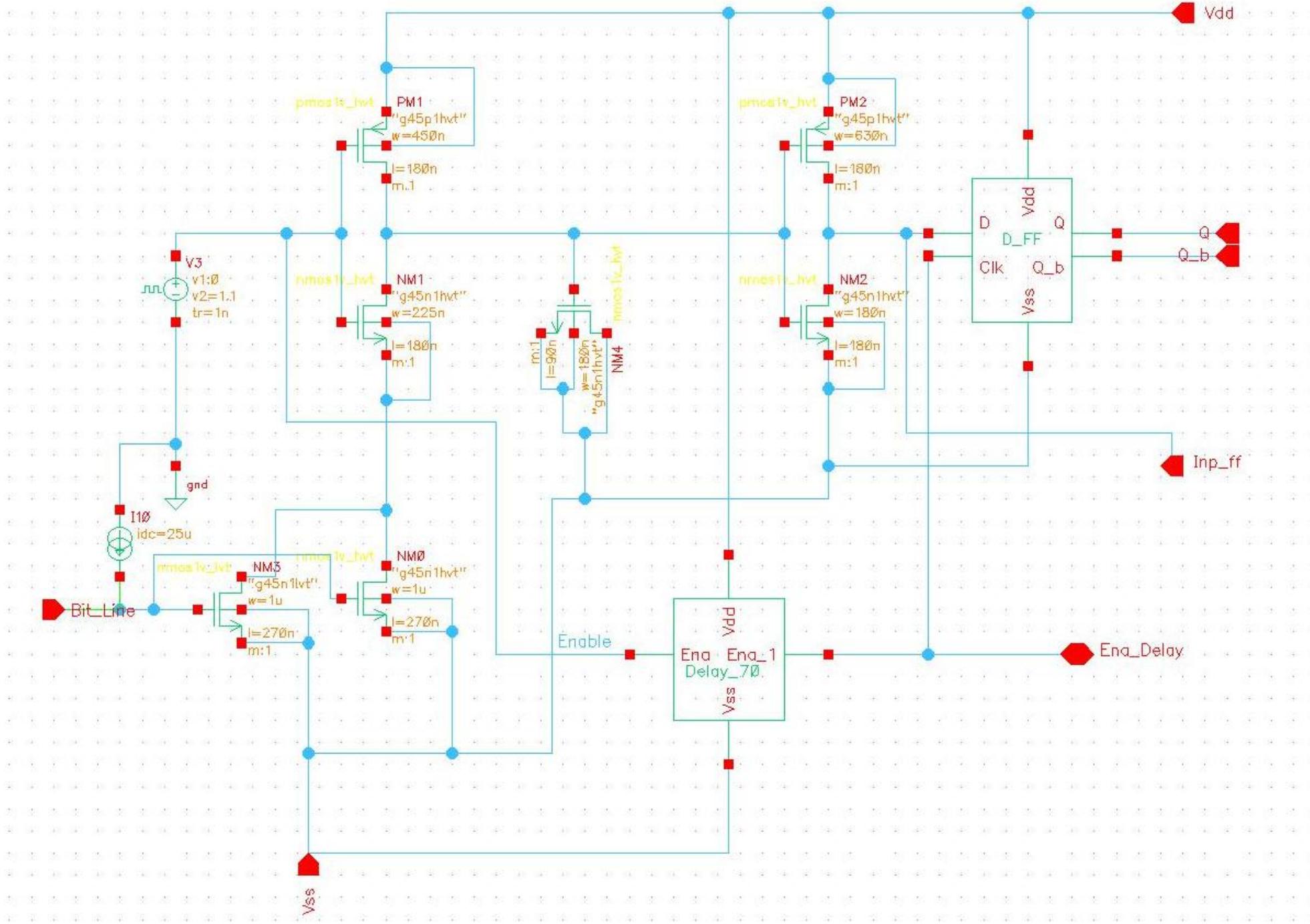
Read circuit /Sense Amplifier



General architecture of time-based sensing schemes

Sense Amplifier



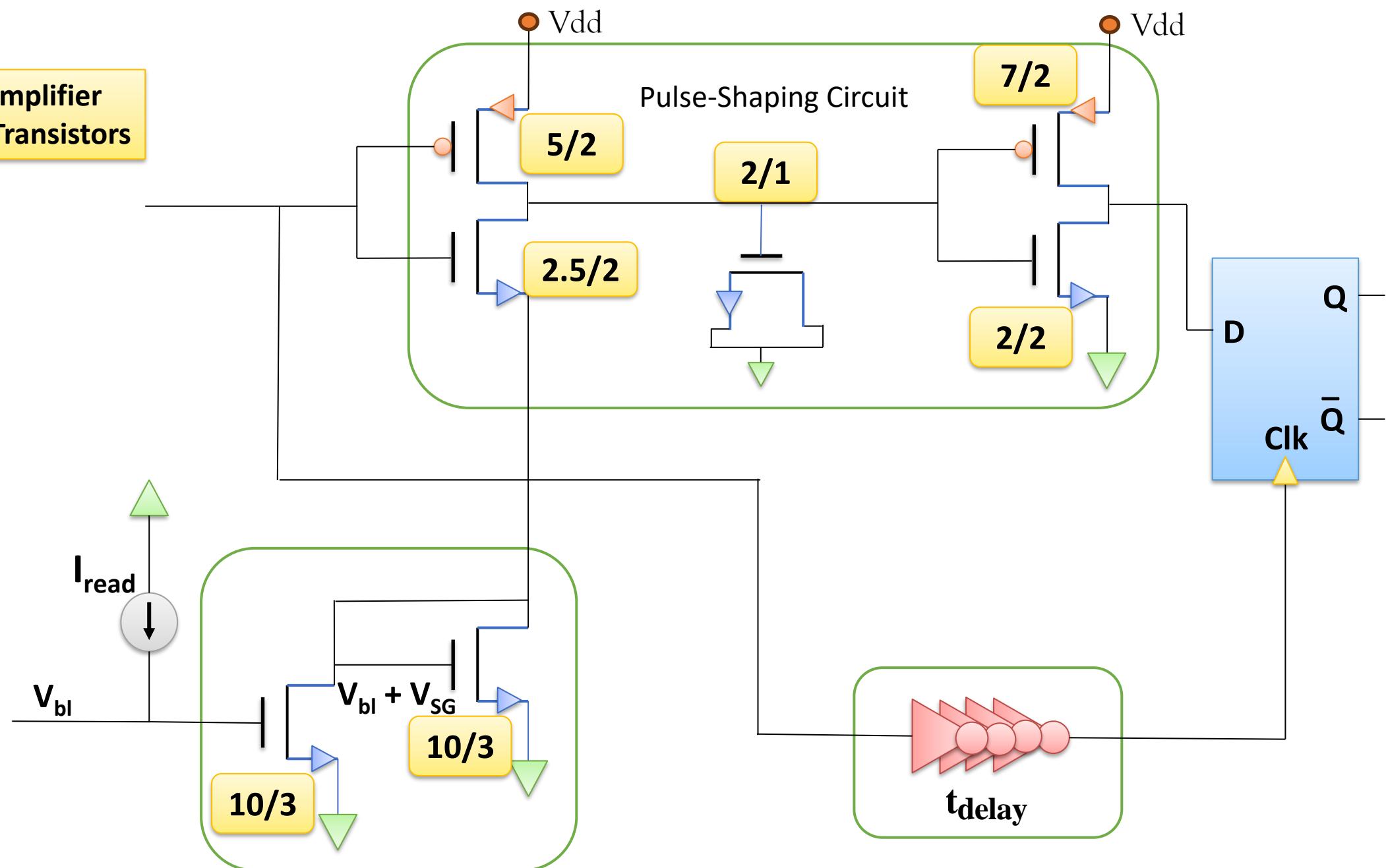


W/L Ratios

- In CMOS circuit design, the W/L ratio (width-to-length ratio) of a transistor is a critical parameter that determines its electrical characteristics. It influences factors such as:
 - **Current-carrying capacity:** A larger W/L ratio allows a transistor to conduct more current.
 - **Switching speed:** A larger W/L ratio can reduce switching time, leading to faster circuit operation.
 - **Power consumption:** A larger W/L ratio can increase power consumption due to higher current flow.
 - **Noise immunity:** A larger W/L ratio can improve noise immunity, making the circuit less susceptible to interference.

The notation "x/y" in the diagram likely indicates the relative W/L ratios of transistors compared to a reference transistor.

Sense Amplifier Sizing of Transistors



Decision Moment

The Time Decision Moment (TDM) refers to the specific point in time when a decision is made in a time-based sensing circuit, particularly in memory sensing circuits like those used for ReRAM.

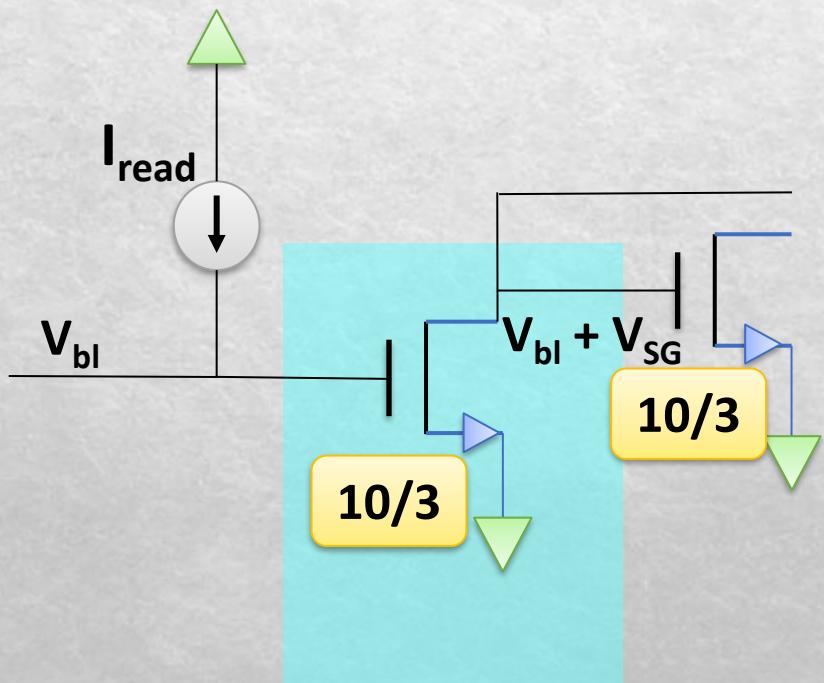
This decision is typically captured by a **time-domain comparator**, such as a D-flip flop (D-FF), which samples the input signal and provides a logical output indicating the state of the memory cell (high or low resistance).

- **Time-based sensing:** Decision based on signal timing, not voltage level.
- **TDM:** Critical moment for decision-making.
- **Voltage-to-time conversion:** Current-starved inverters convert voltage to time.
- **Decision process:** Comparator (D-FF) samples output signal at TDM.
- **LRS:** More current, **Short delay, early** TDM for correct decision.
- **HRS:** Less current, **Long delay, later** TDM for correct decision.
- TDM is between 4.8K & 8.7K.

Components of Sense Amplifier

- Common drain MOS (BL Booster)
- Current starved inverters
- Mos-Cap M5
- SHAPING INVERTER
- CHAIN OF INVERTERS
- D Flip flop

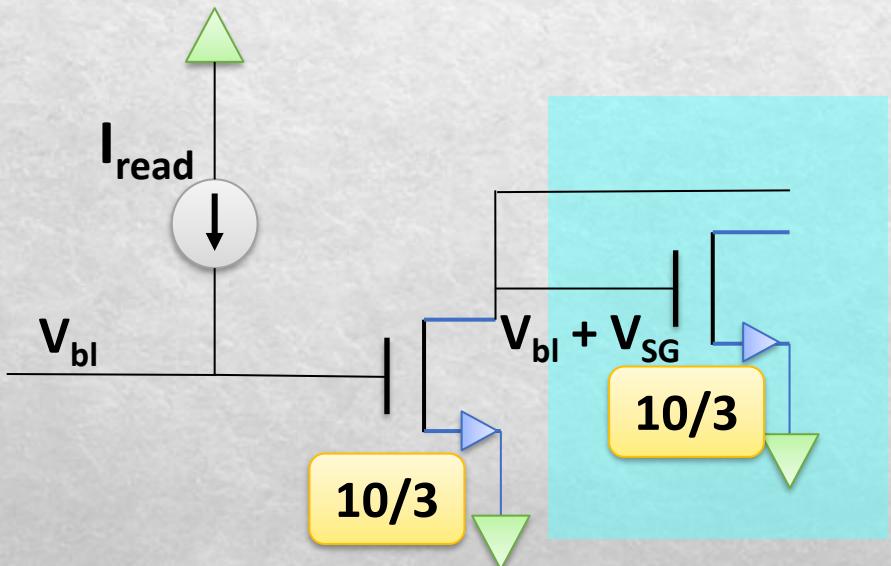
Common drain MOS (BL Booster)



The **common-drain stage** uses **M1**, which is a **PMOS transistor**, to boost the bit-line voltage to a level suitable for time-based comparison.

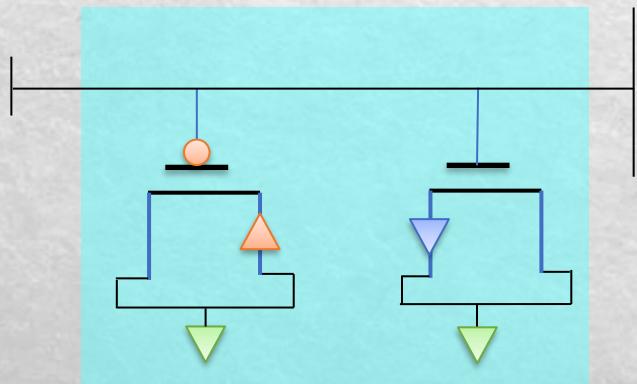
- **M1's Role:**
 - PMOS transistor with source connected to the **Bit Line (BL)**, and drain connected to ground.
 - This stage is known as a **voltage follower** or **source-follower**, which buffers the bit-line voltage without significant loading.
 - It boosts the **bit-line voltage VBL** by adding the **source-gate voltage VSG** of M1. The output of M1 is the sum of VBL and the voltage drop across the source-gate.

Current starved inverters



- **M2** is the **current-starving transistor** that limits or controls the current flowing through the **M3-M4 inverter**.
- **M2** is connected in series with **M3 (NMOS)**, forming a path to ground. The amount of current that can flow through this path depends on how much **M2** conducts.
- **Gate of M2:** The gate of M2 is controlled by the **boosted bit-line voltage** $V_{bl}+V_{SG}$

Mos-Cap M5



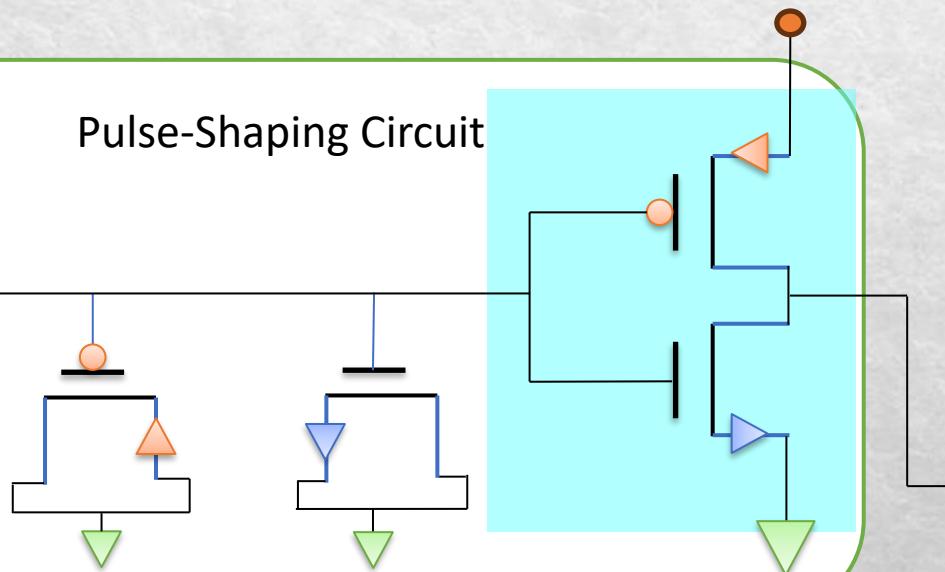
- Transistors **M₅** and **M₆** are typically connected in such a way that they behave like **capacitors** in this stage of the circuit.

Capacitive behavior:

- MOSFETs have inherent **gate capacitance** and **drain-source capacitance**, which can be exploited to act like a capacitor in the circuit.
- In this case, **M5** and **M6** are likely connected in such a way that they add **load capacitance** to the output of the current-starved inverter stage (M2, M3, M4).
- The capacitive load introduced by M5 and M6 slows down the rise and fall times of the signal, which helps in shaping the timing characteristics of the inverter's output signal.
- By adding a capacitive load, they create a **delayed response** and allow the signal to transition more smoothly or with a desired time constant.

SHAPING INVERTER

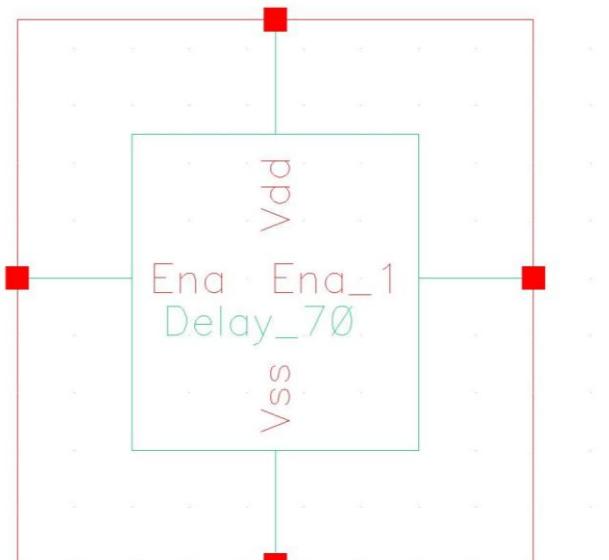
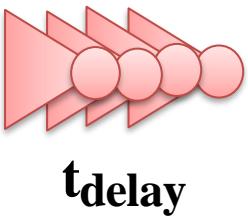
Pulse-Shaping Circuit



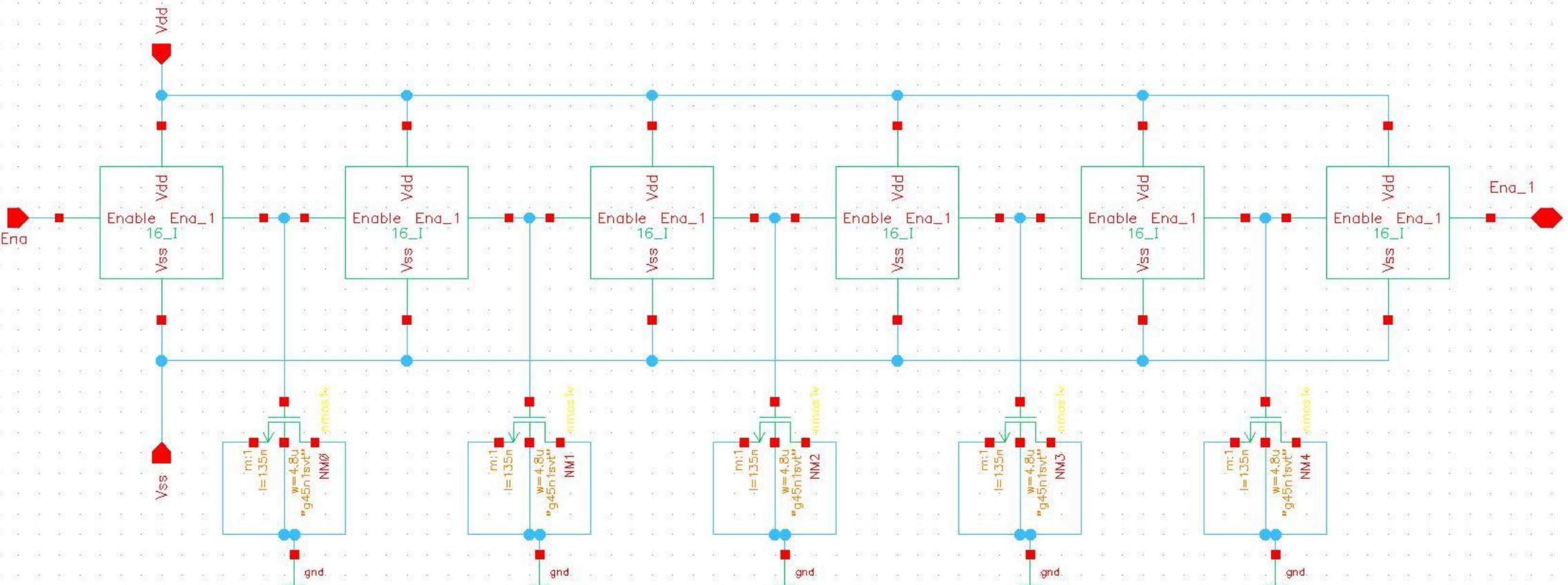
The **Pulse-Shaping Inverter Stage (M7–M8)** is a crucial part of the sense amplifier in time-based sensing circuits.

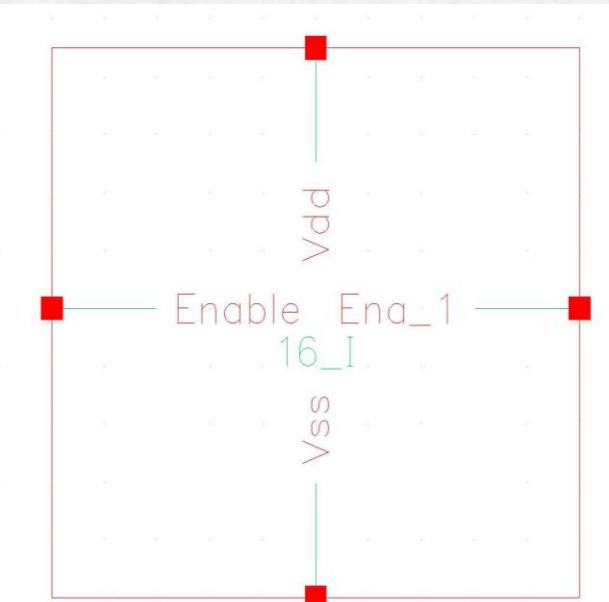
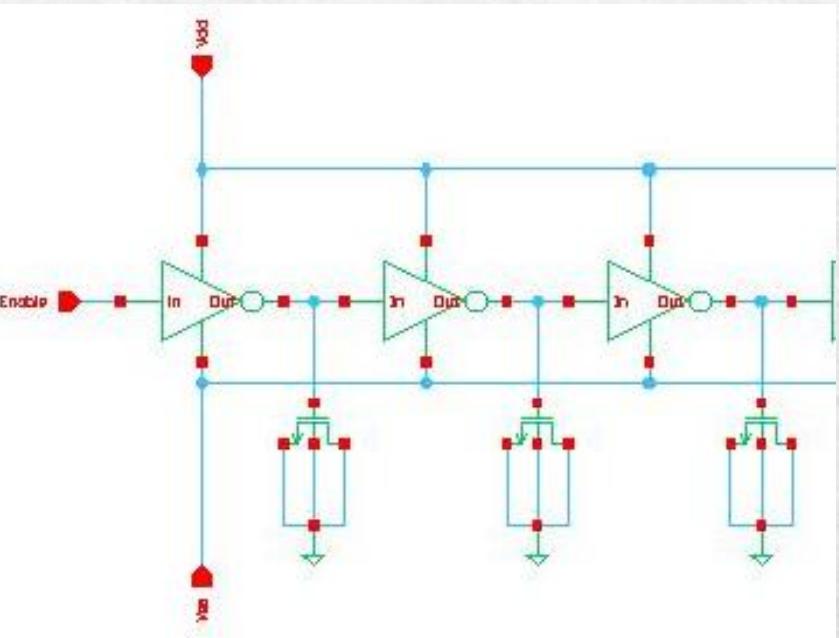
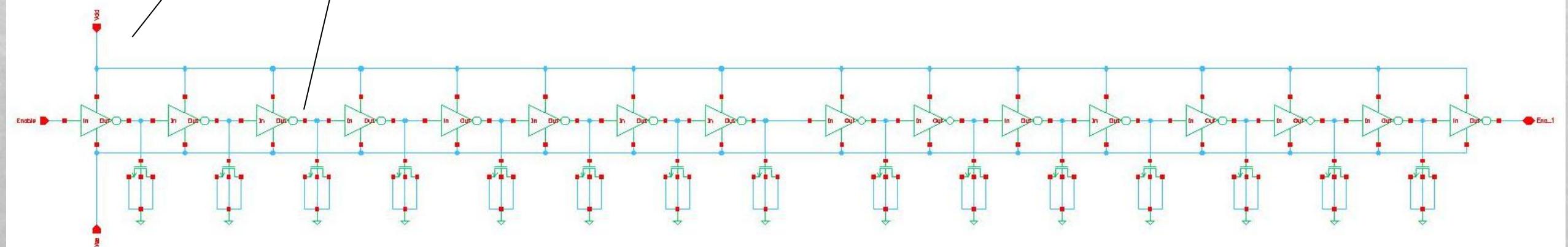
- After M5 and M6, the signal passes through another inverter pair, **M7** (PMOS) and **M8** (NMOS), which further sharpens the signal.
- This second inverter helps to
 - further clean up the signal,
 - ensuring that the edges are as sharp as possible before the signal is fed into the **D-flip flop** for decision-making.
- M7 and M8 work in the same manner as M5 and M6, but they further reduce any remaining signal distortion caused by noise or slow transitions from earlier stages.

CHAIN OF INVERTERS



- A **Programmable Delay Line (PDL)** is an important element in circuits where precise timing control is required, particularly in time-based sensing schemes.
- It allows you to adjust the time it takes for a signal to propagate through the circuit, which can be used to fine-tune the operation and improve accuracy.
- In the context of the **time-based sensing circuit** used for ReRAM majority gate sensing, the PDL ensures that the signal arrives at the **decision moment (TDM)** at exactly the right time, allowing the D-flip flop (D-FF) to latch the signal correctly.
- The delay produced by the PDL is adjustable, providing flexibility to account for variations in the bit-line voltage and resistances.

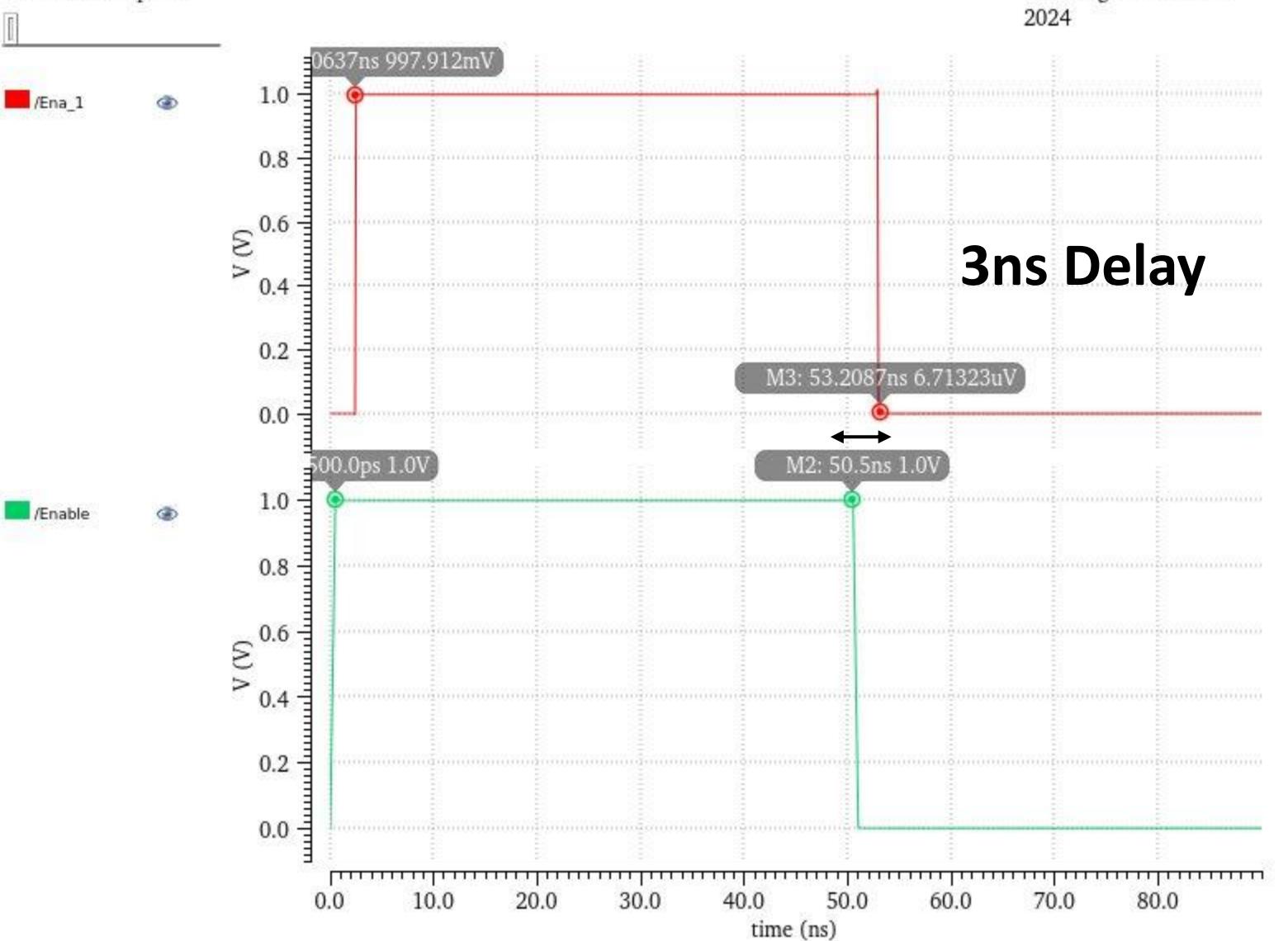




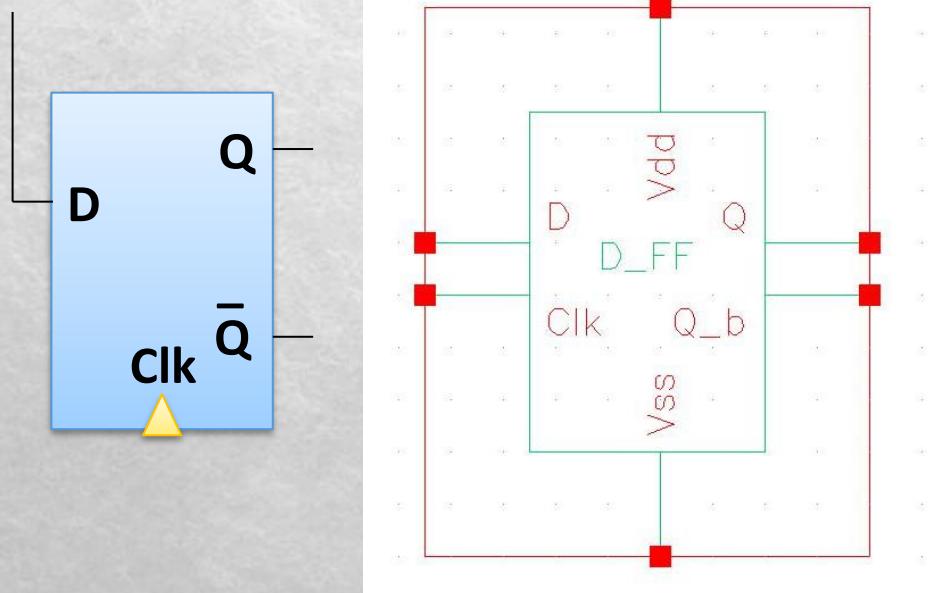
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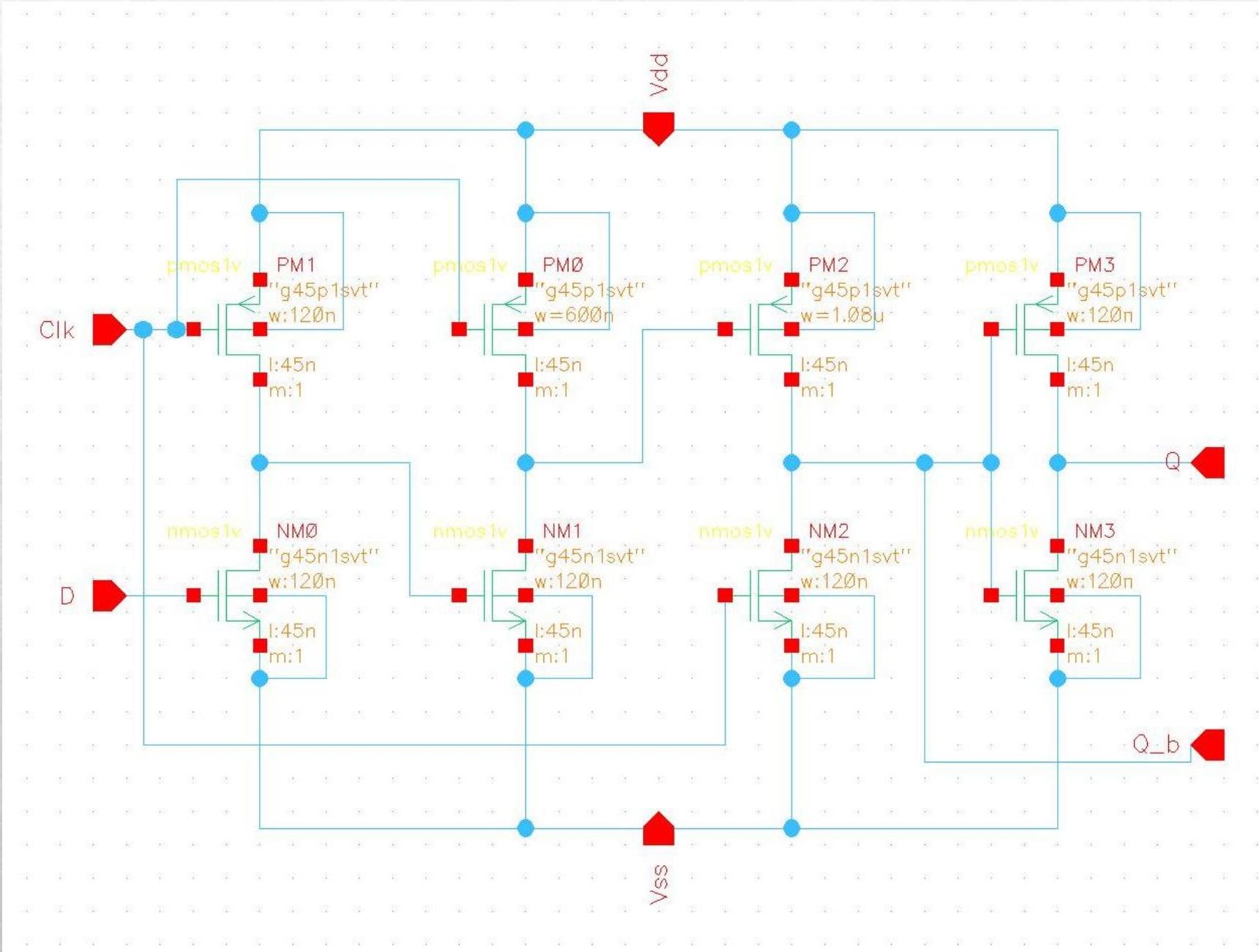
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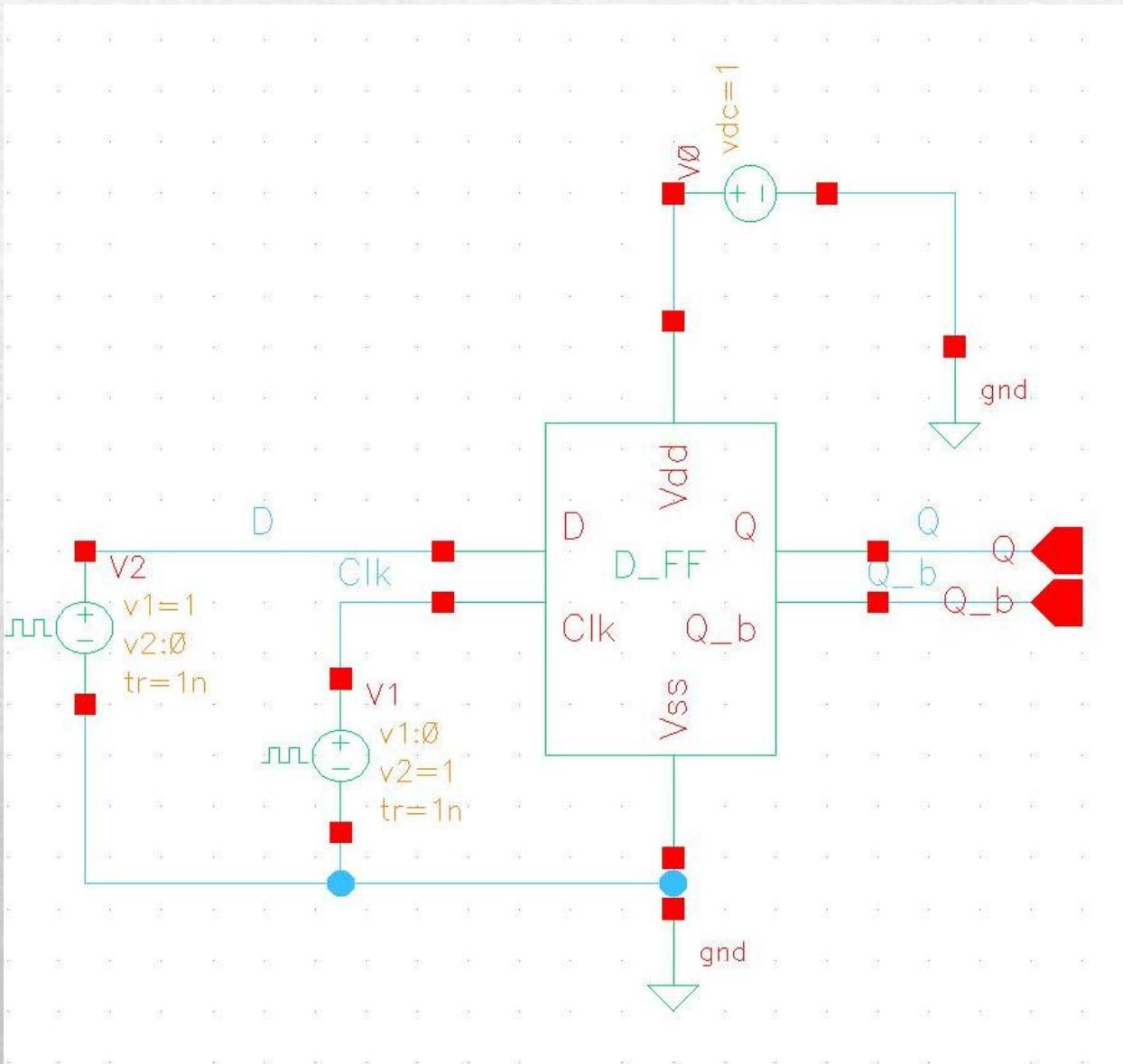


D-Flip flop



- The time-domain comparator, typically implemented using a D-flip flop (D-FF), captures the state of the signal at its input when the EN signal transitions high.
- This synchronization is critical because it ensures that the sensing circuit reads the correct state of the ReRAM cell at the right moment (TDM).
- If the D-FF samples the signal too early or too late, it may yield incorrect data, leading to errors in memory read operations.
- **Two possible outcomes:**
 - **If the delay is short (LRS):** The pulse reaches the D-FF input before the TDM, and the D-FF outputs a **low** state (indicating a low resistance).
 - **If the delay is long (HRS):** The pulse arrives after the TDM, and the D-FF outputs a **high** state (indicating high resistance).

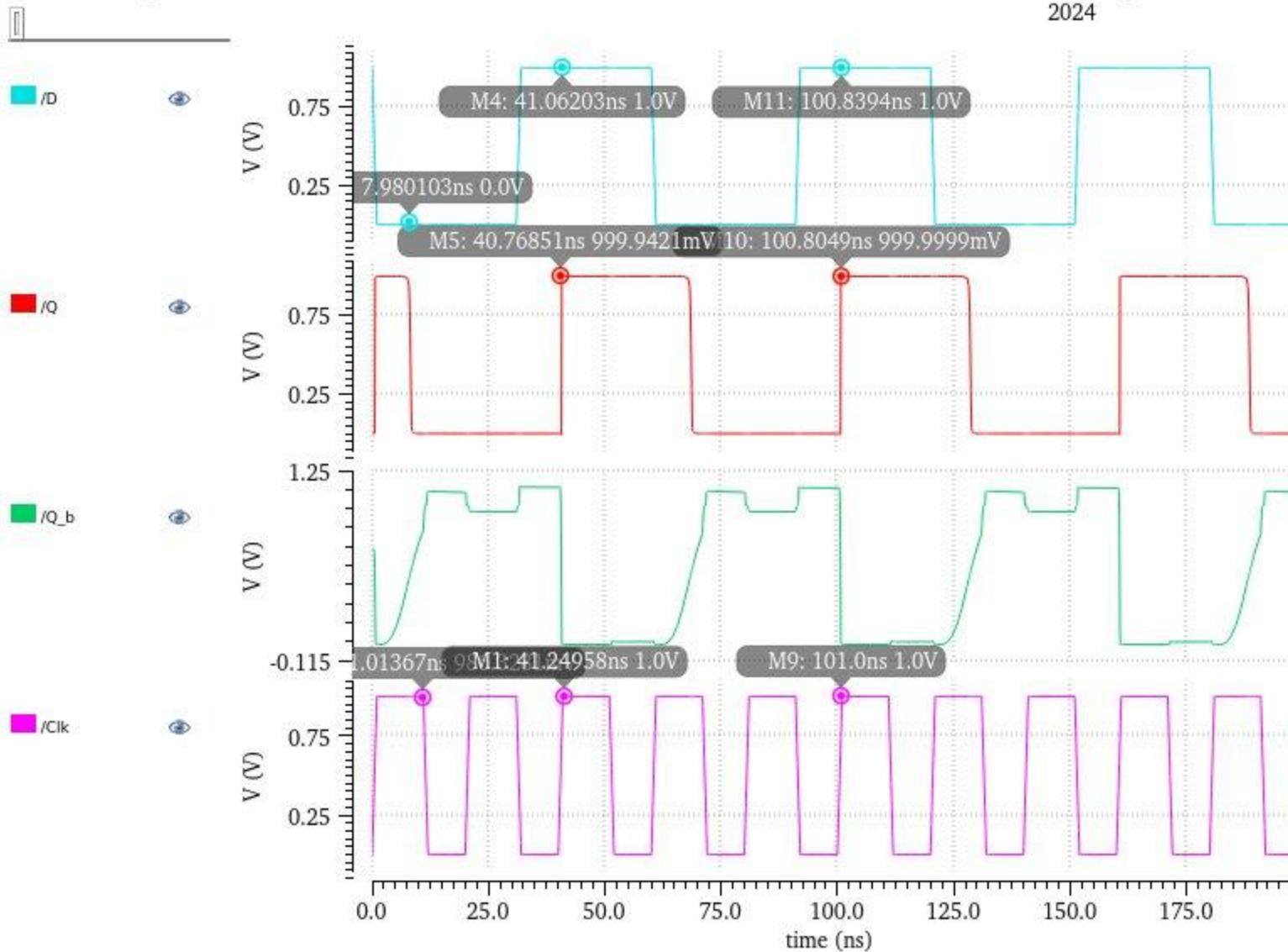




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Truth Table for a 3-Input Majority Gate

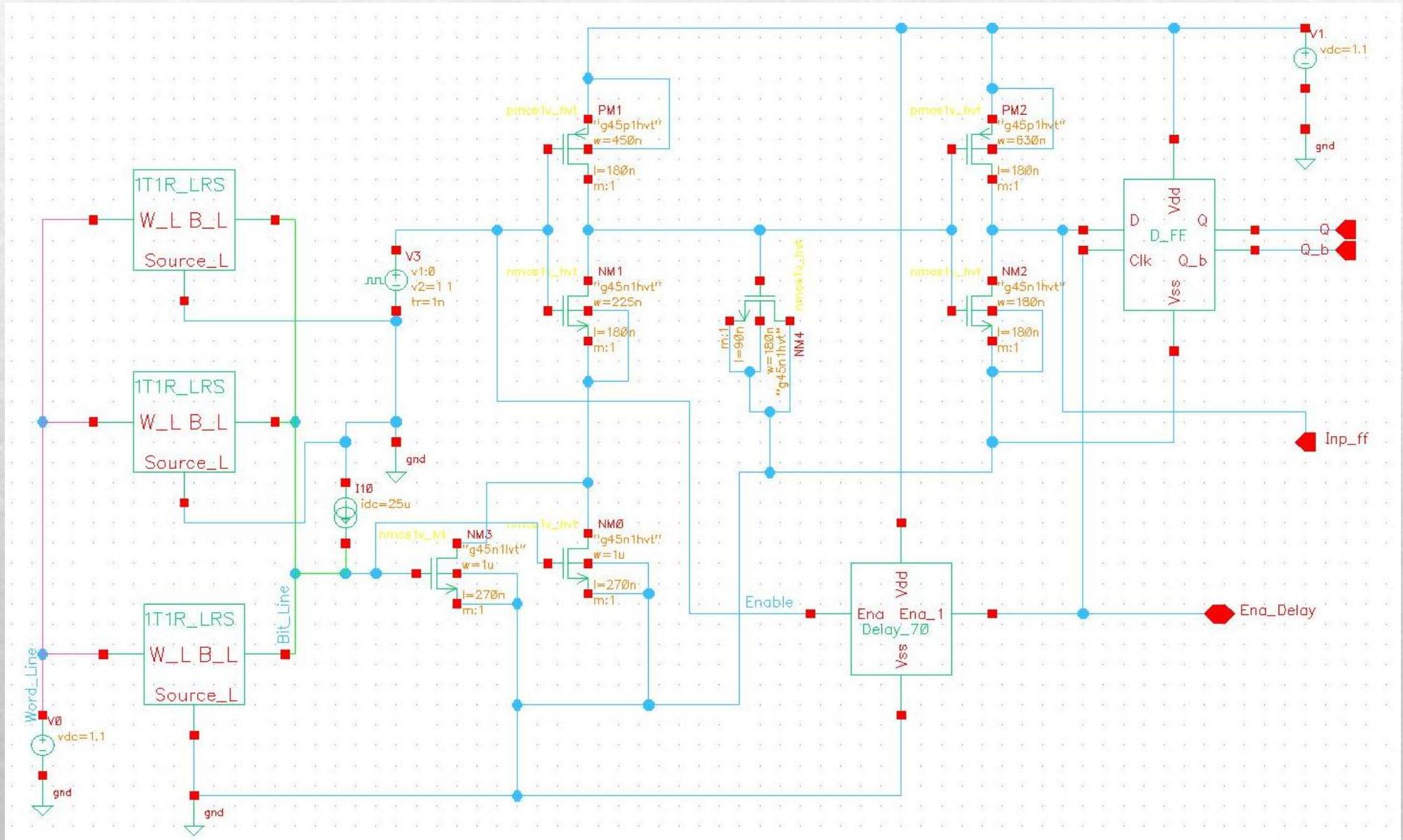
A	B	C	M₃(A, B, C)	V_{bl}	Digital Logic
0	0	0	0 (means LRS Here)	86.2261 mV	1
0	0	1	0	125.5681 mV	1
0	1	0	0	125.5681 mV	1
0	1	1	1	228.212 mV	0
1	0	0	0	125.5681 mV	1
1	0	1	1	228.212 mV	0
1	1	0	1	228.212 mV	0
1	1	1	1 means HRS here	648.261 mV	0

Explanation:

- The output is 1 if the majority (two or more) of the inputs are 1.
- The output is 0 if the majority of the inputs are 0.

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Experimental Observations

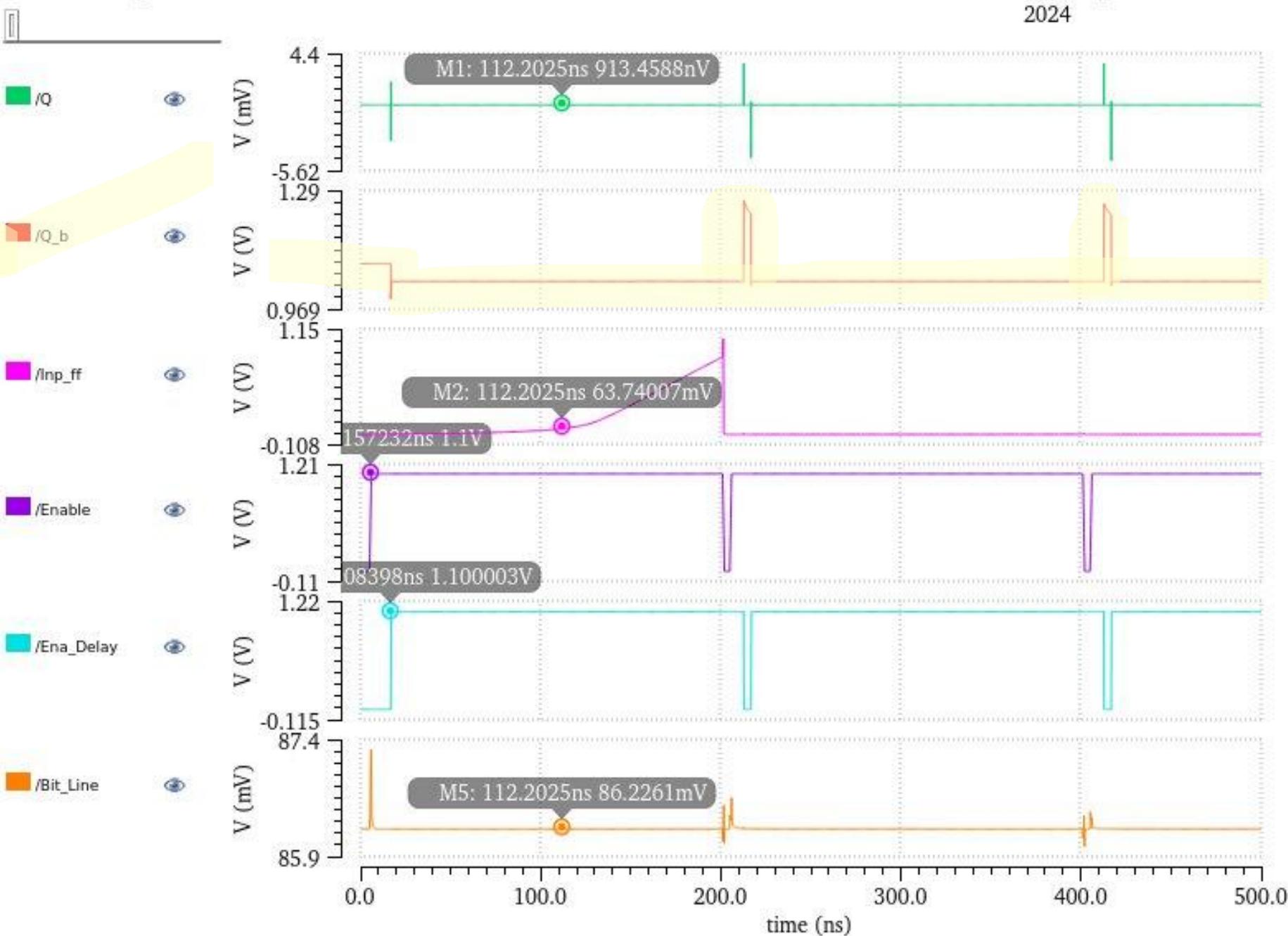


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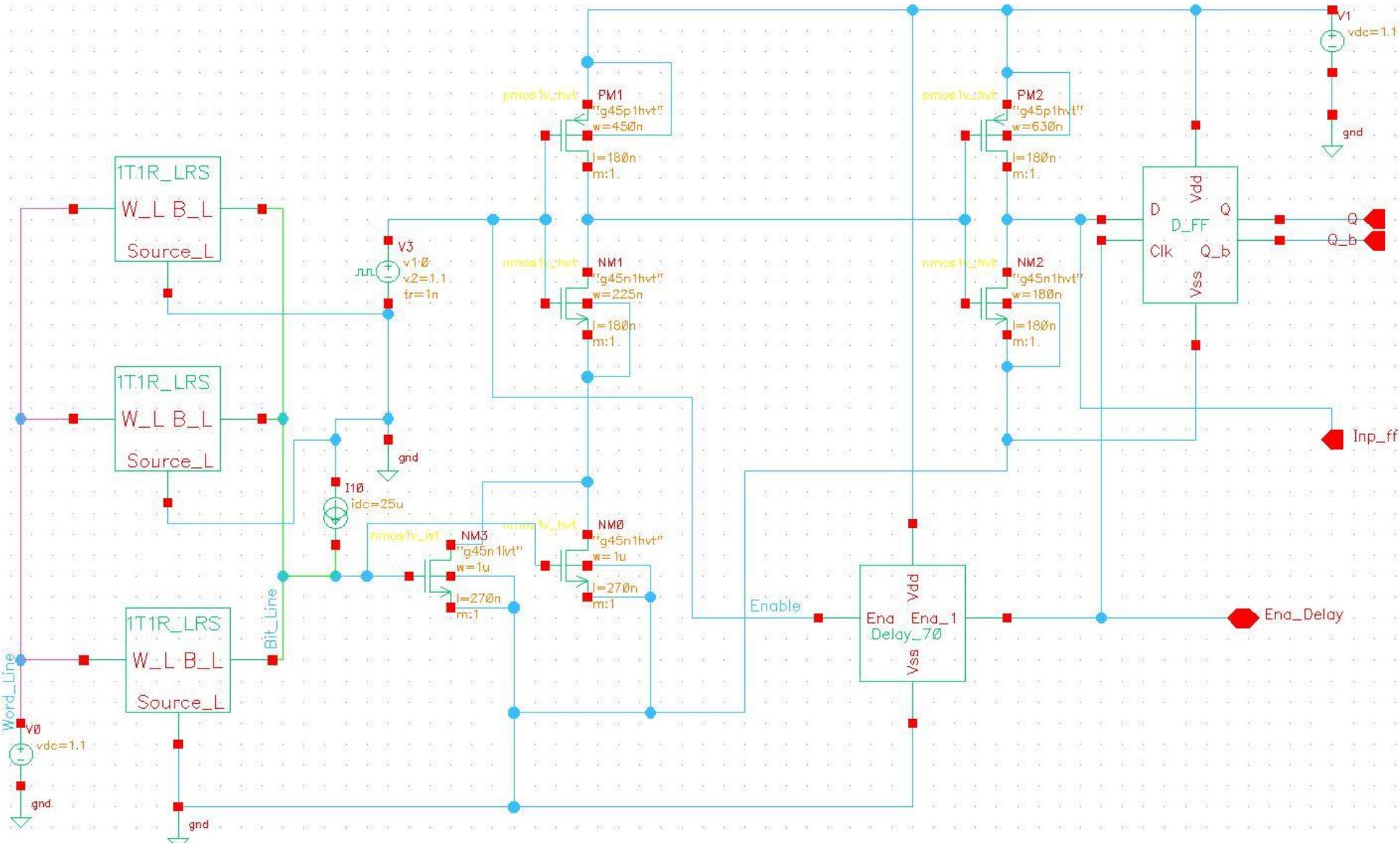
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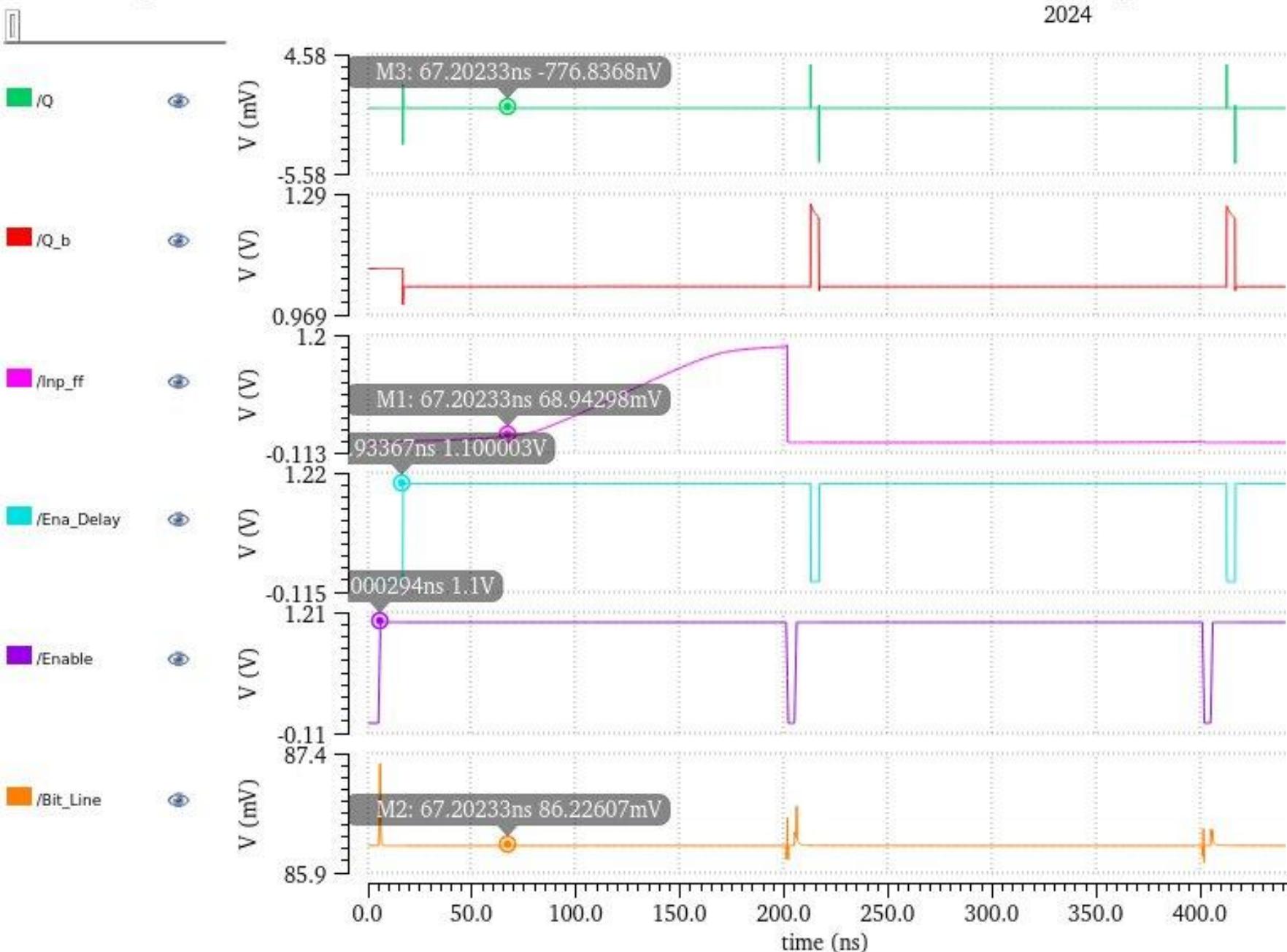
Without M₅



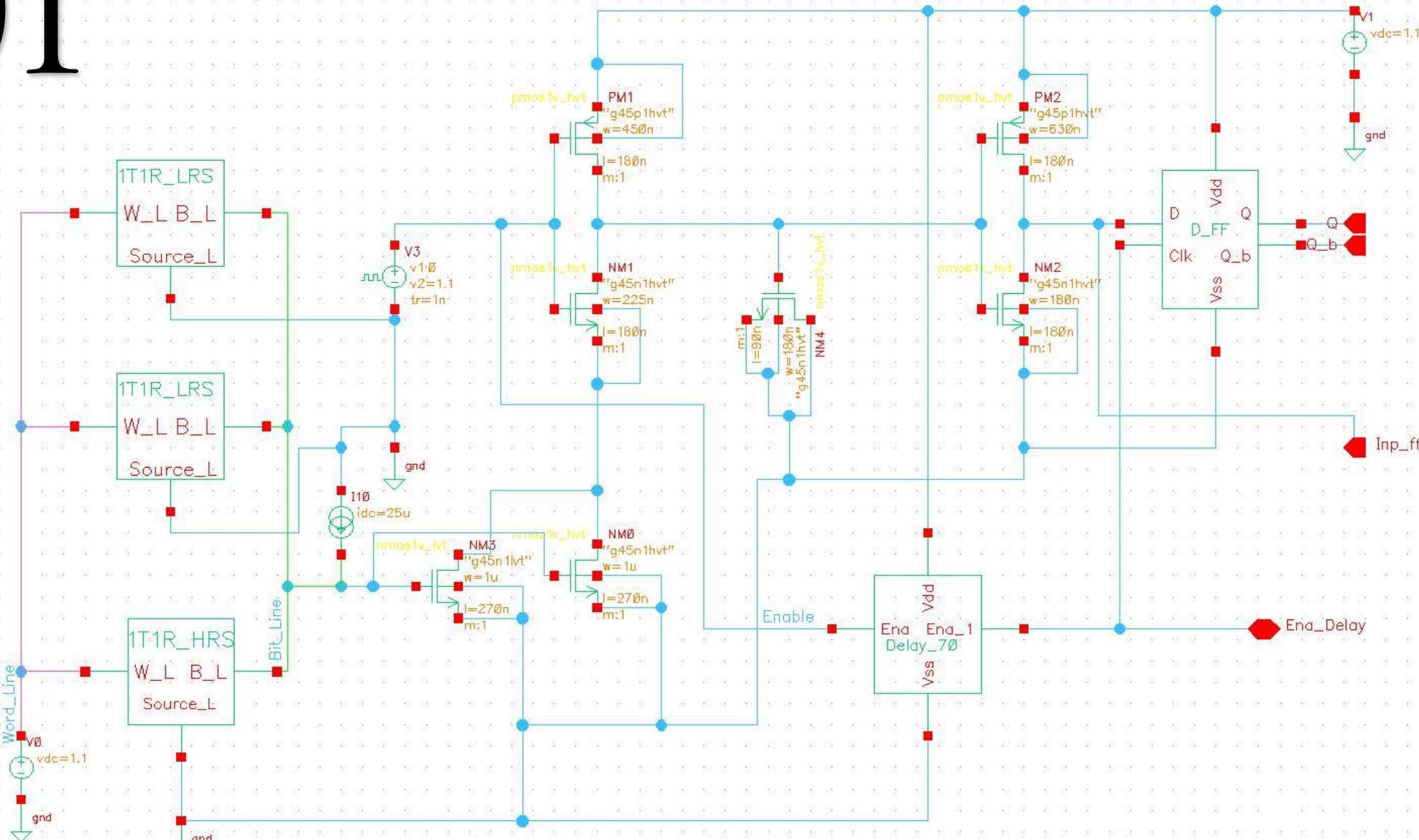
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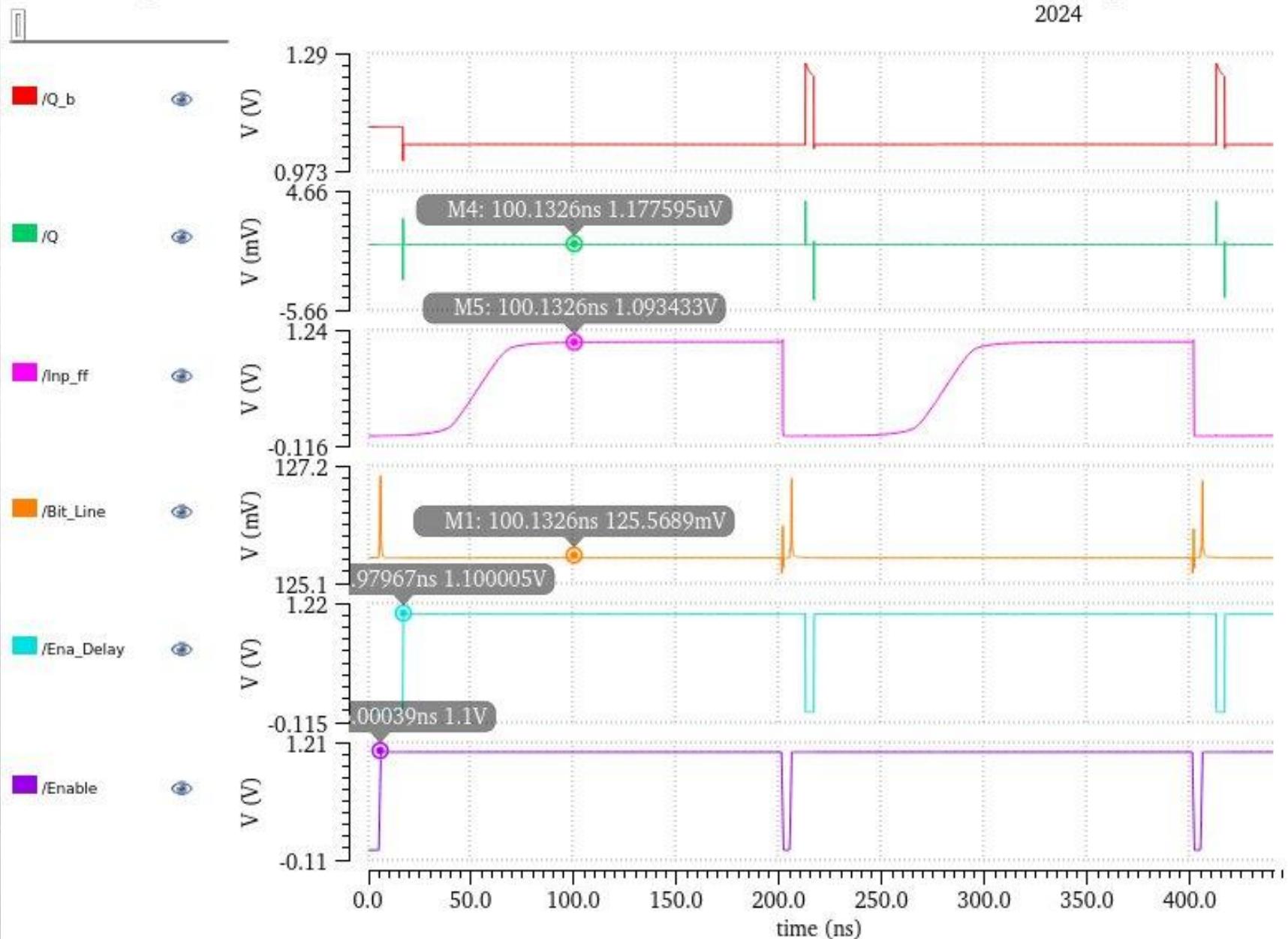
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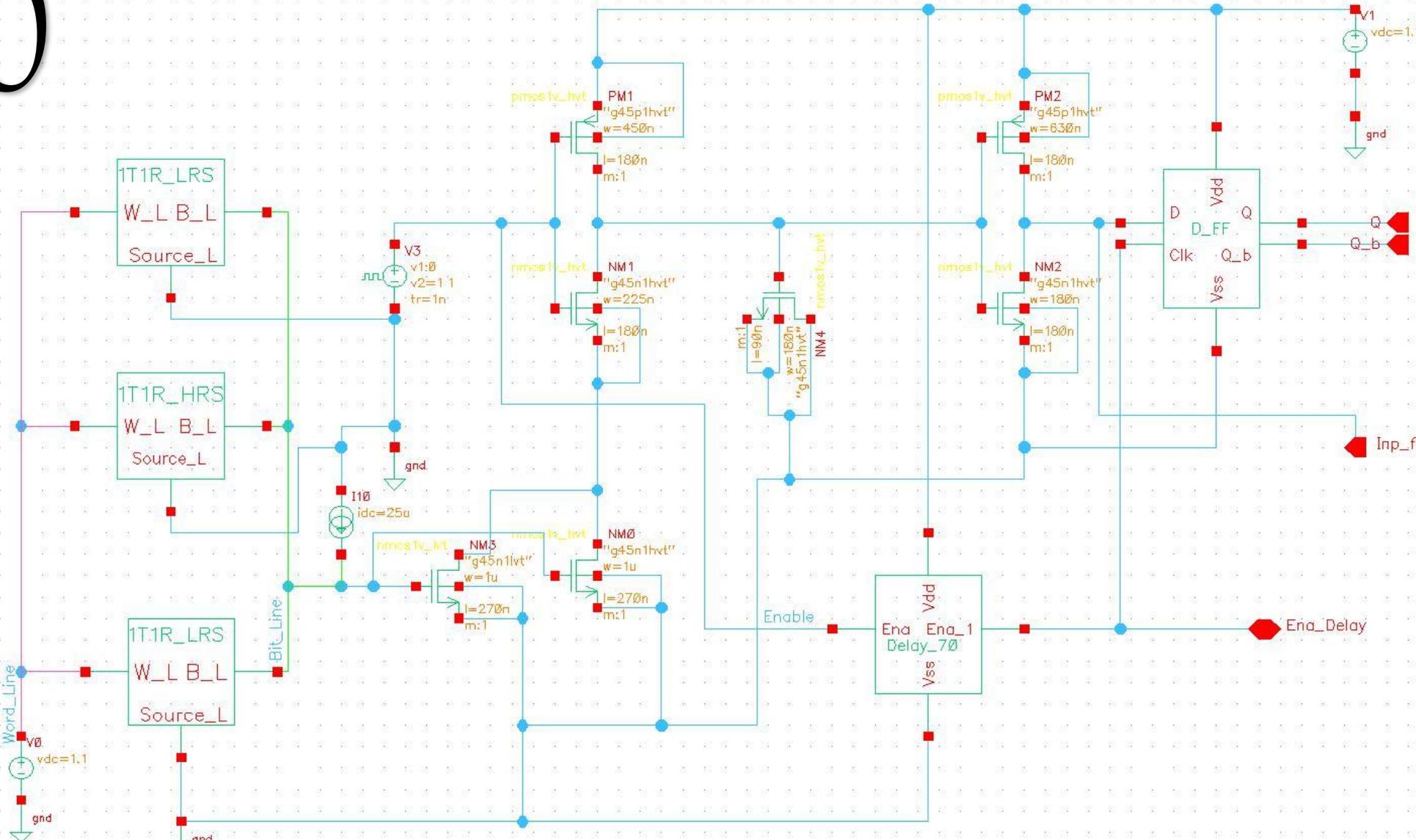
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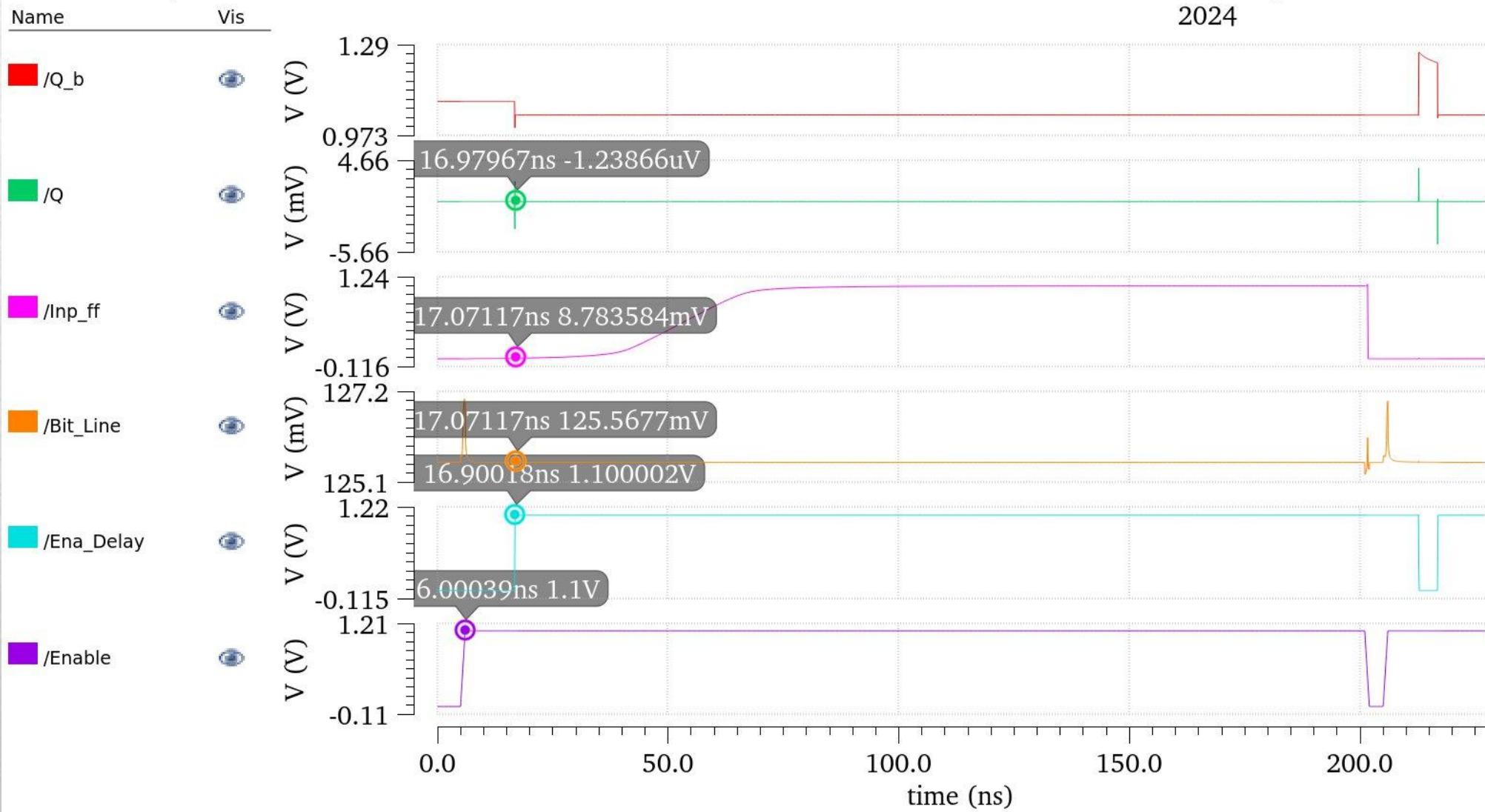
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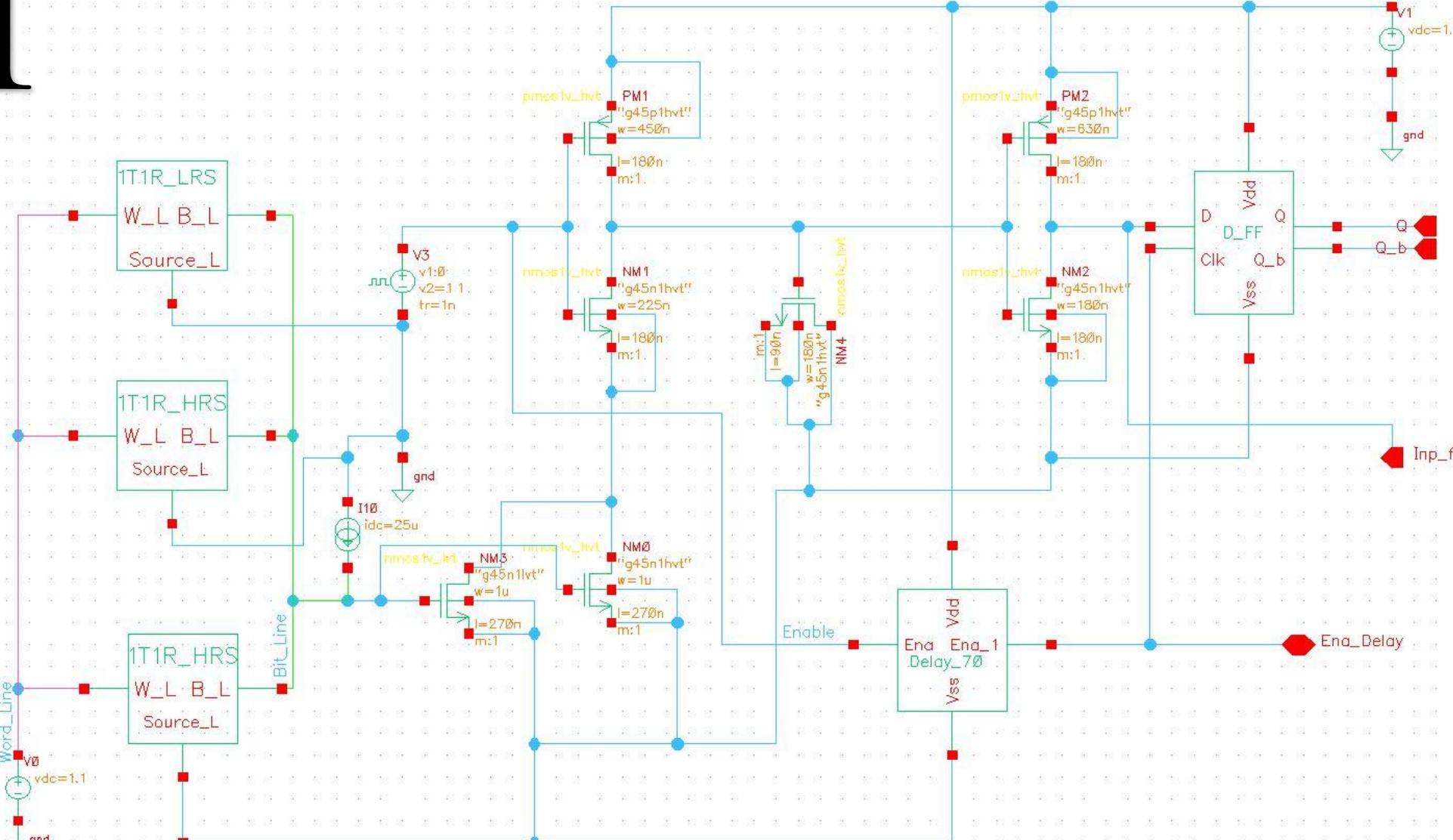
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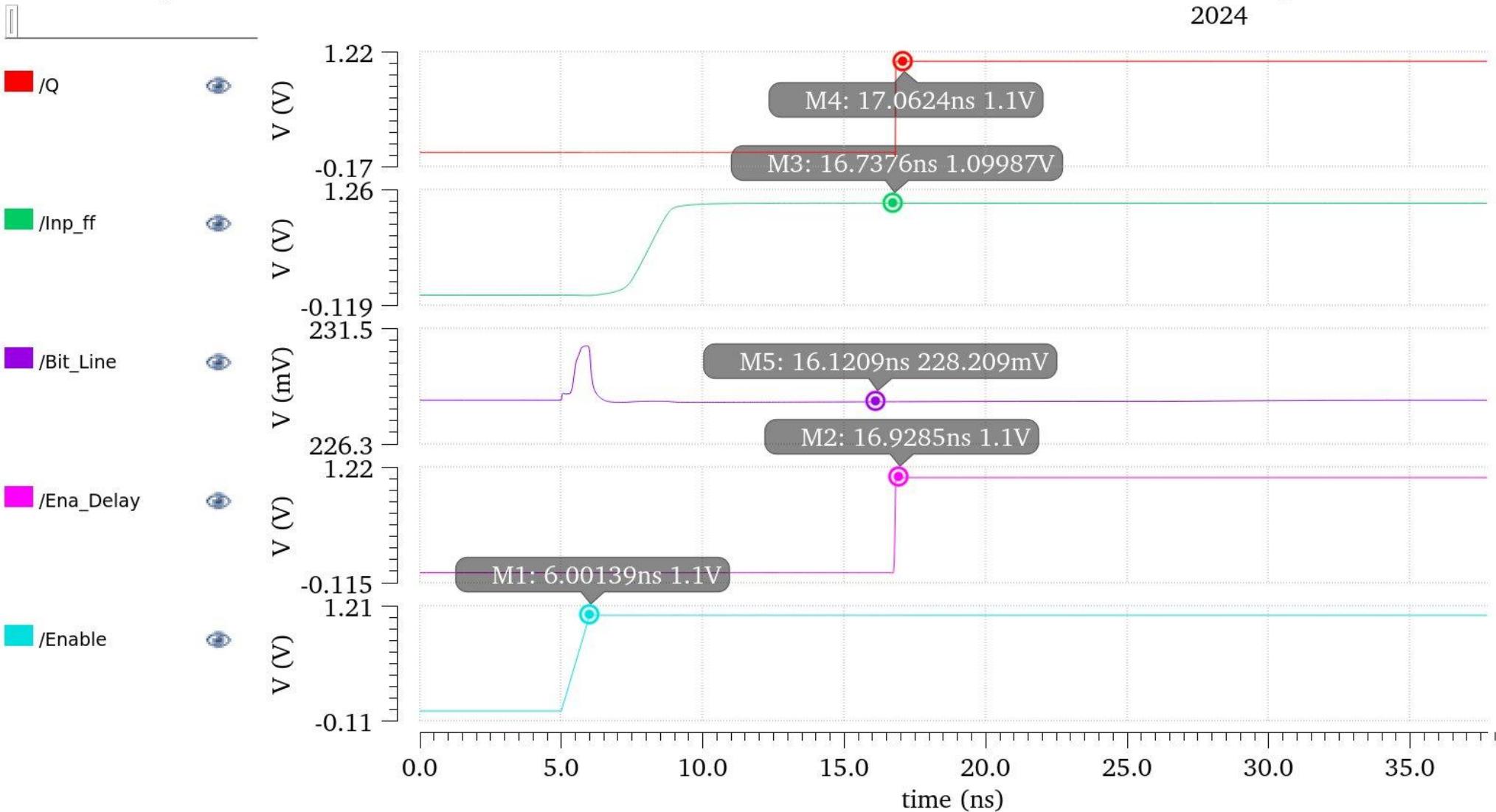
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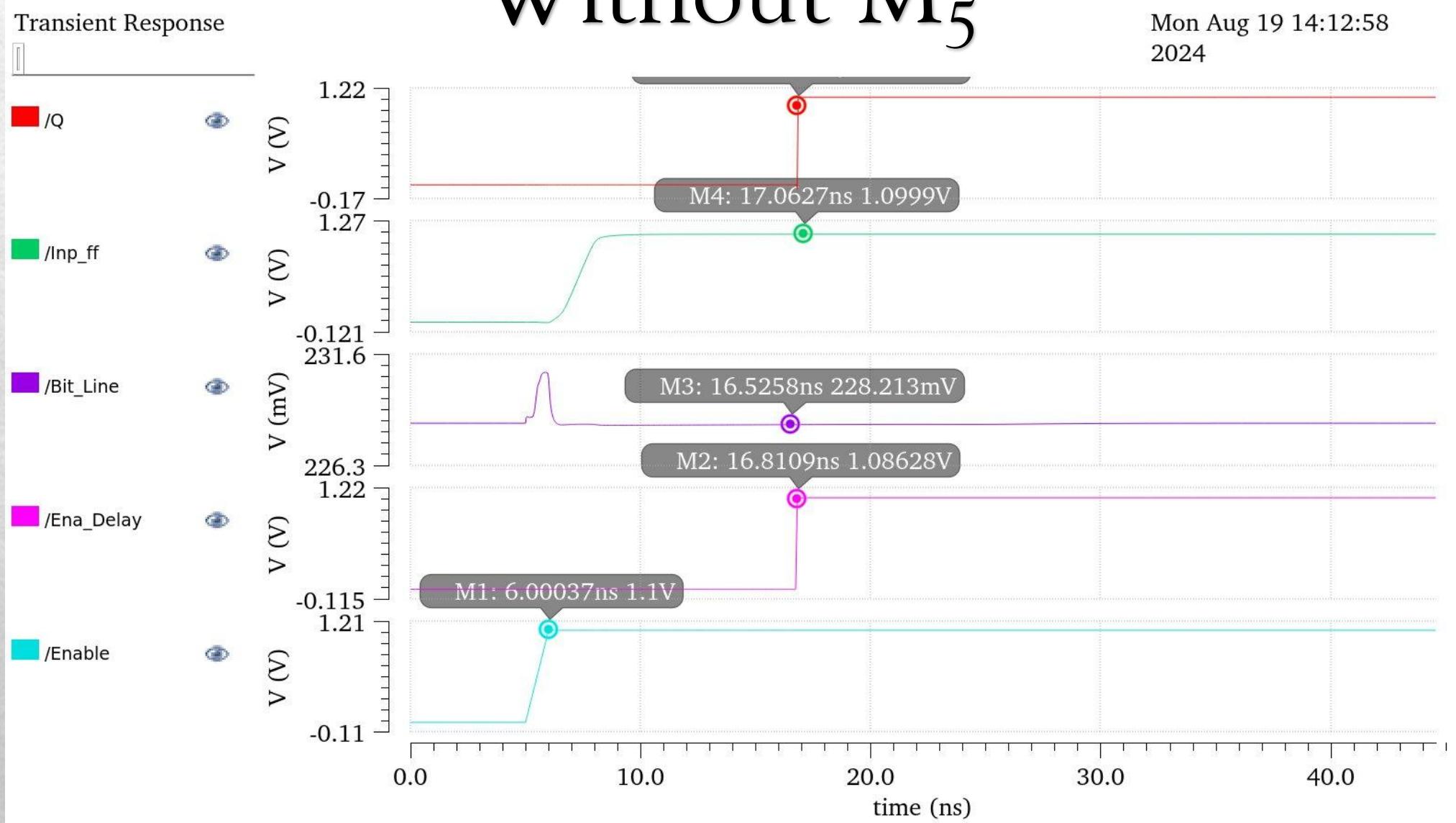
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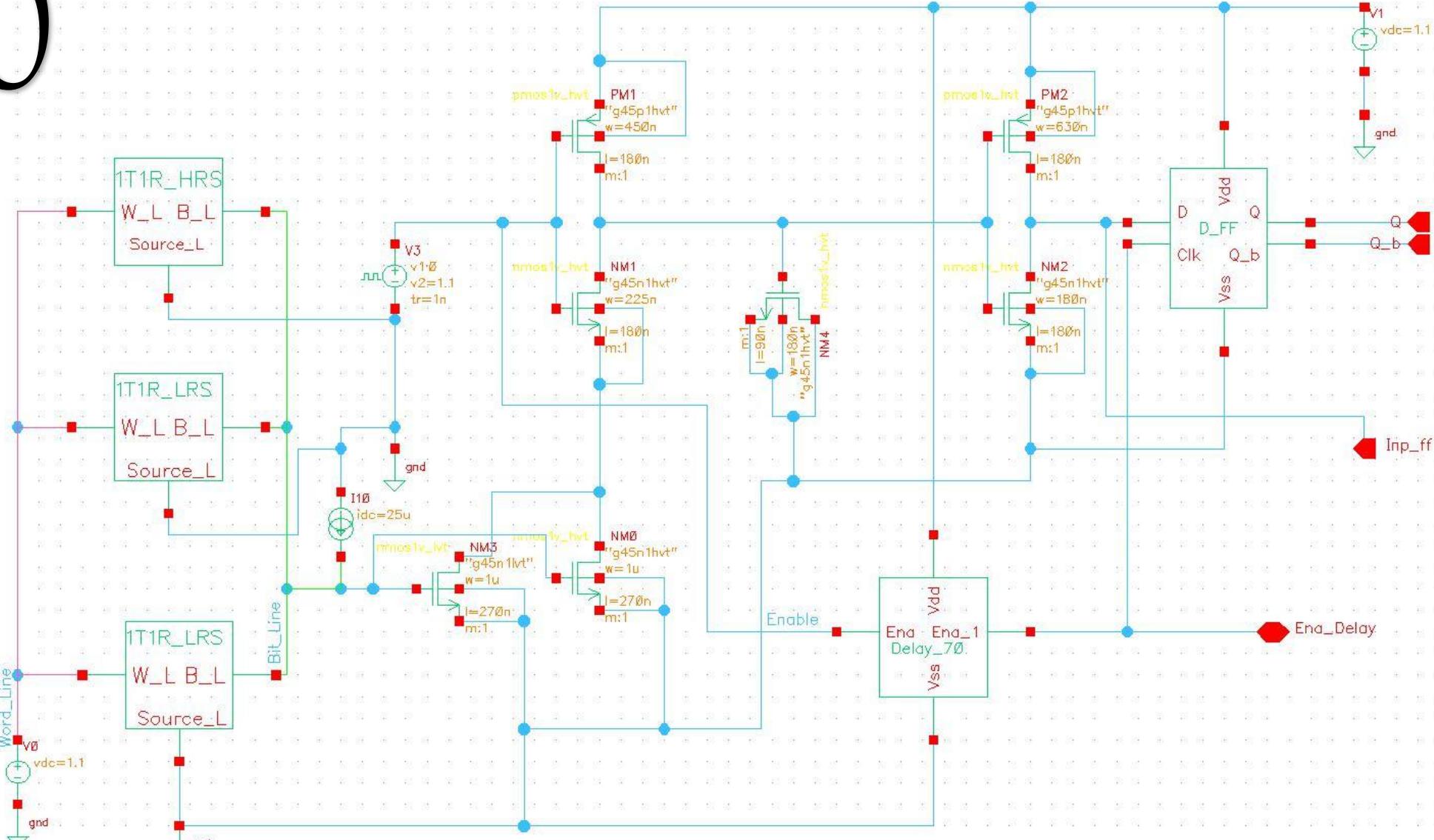
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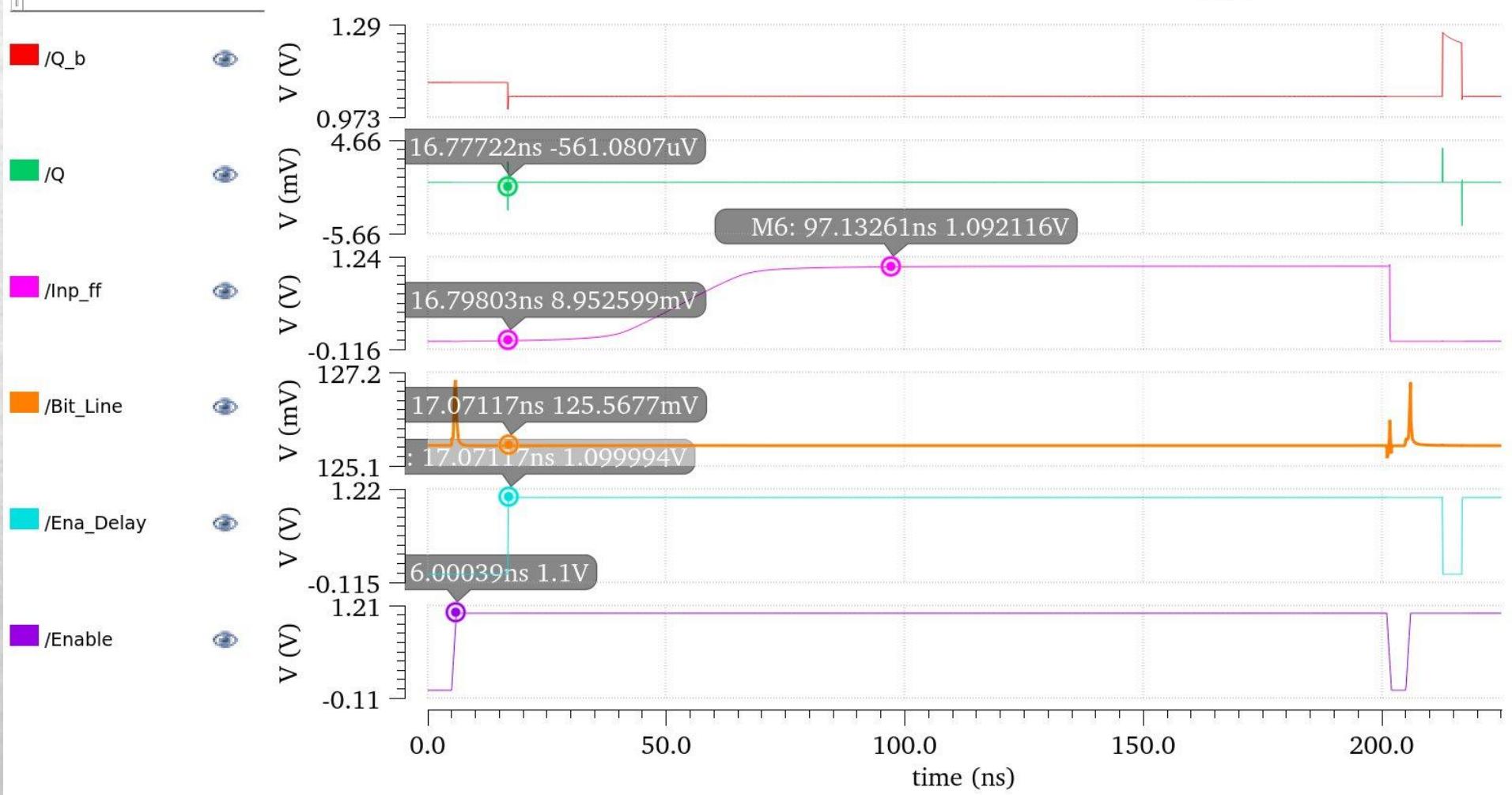
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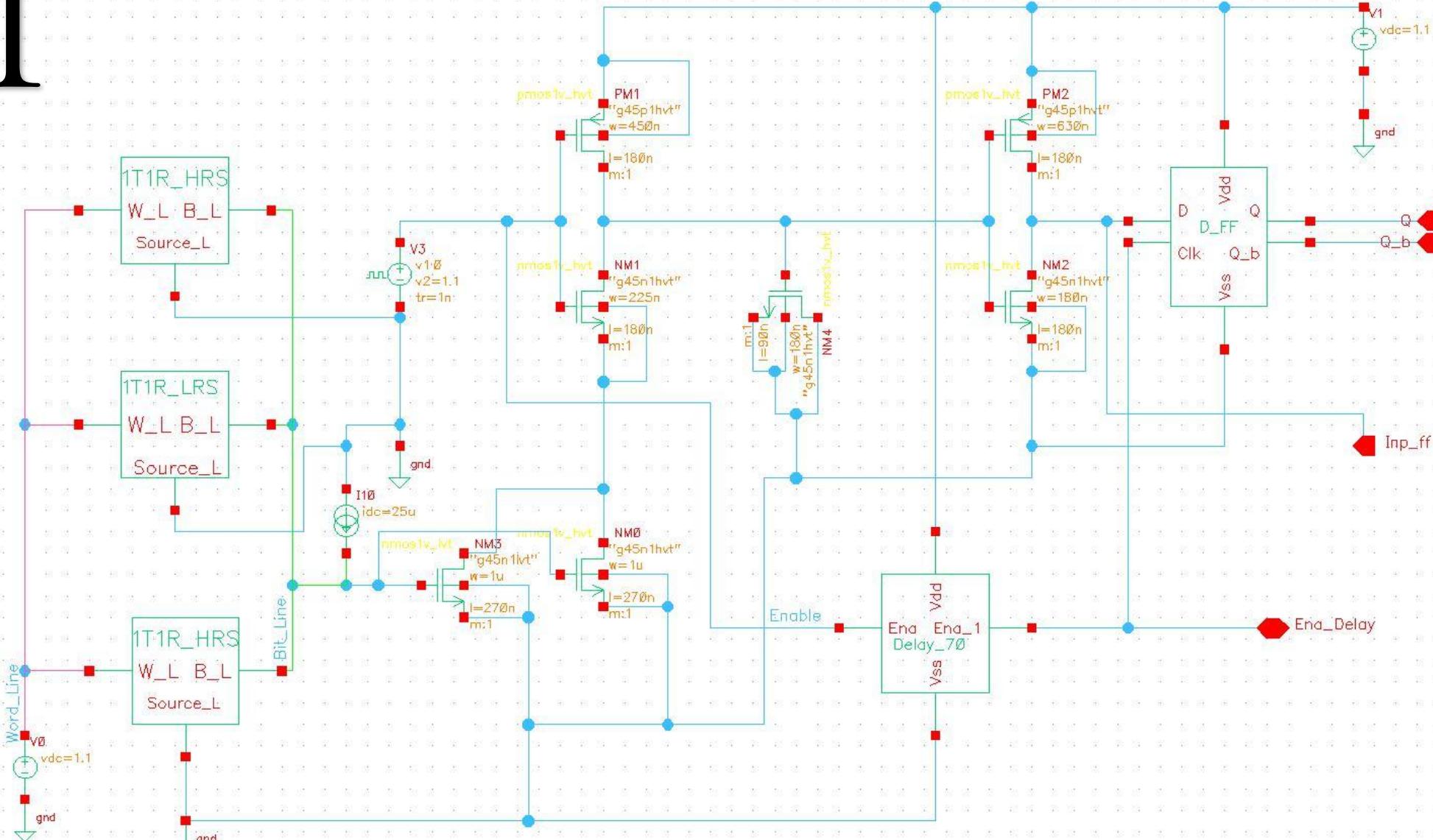
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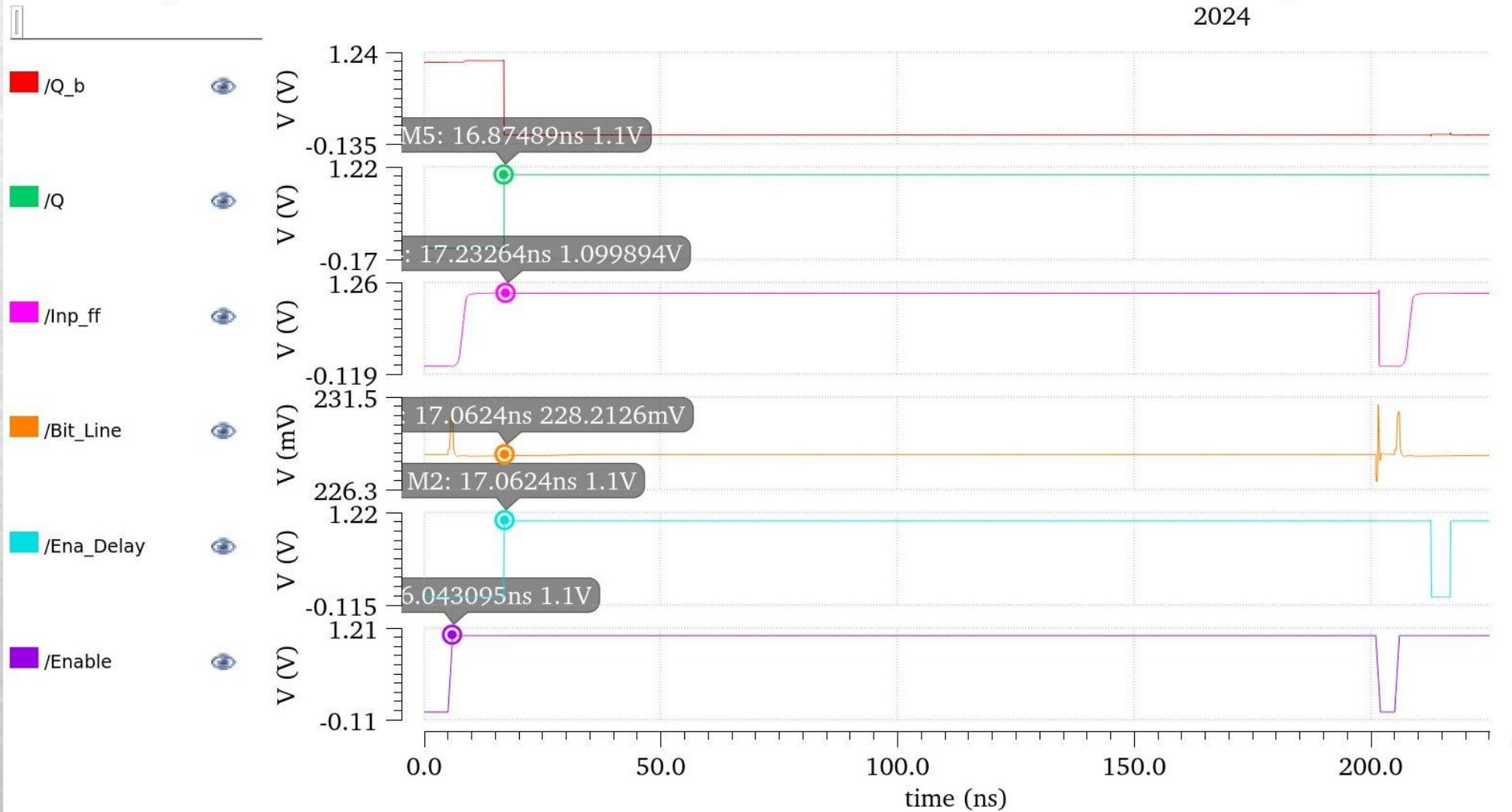
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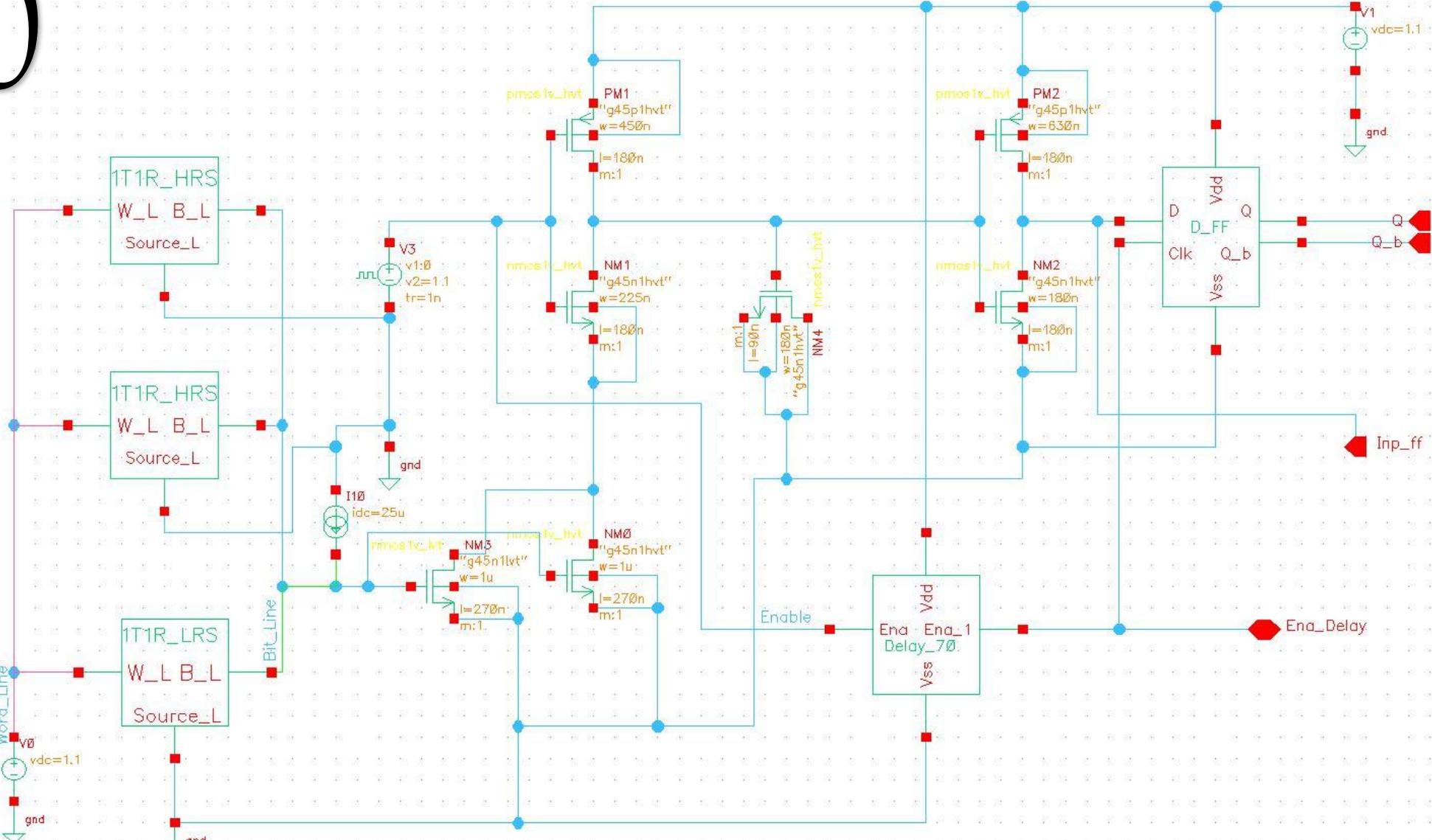
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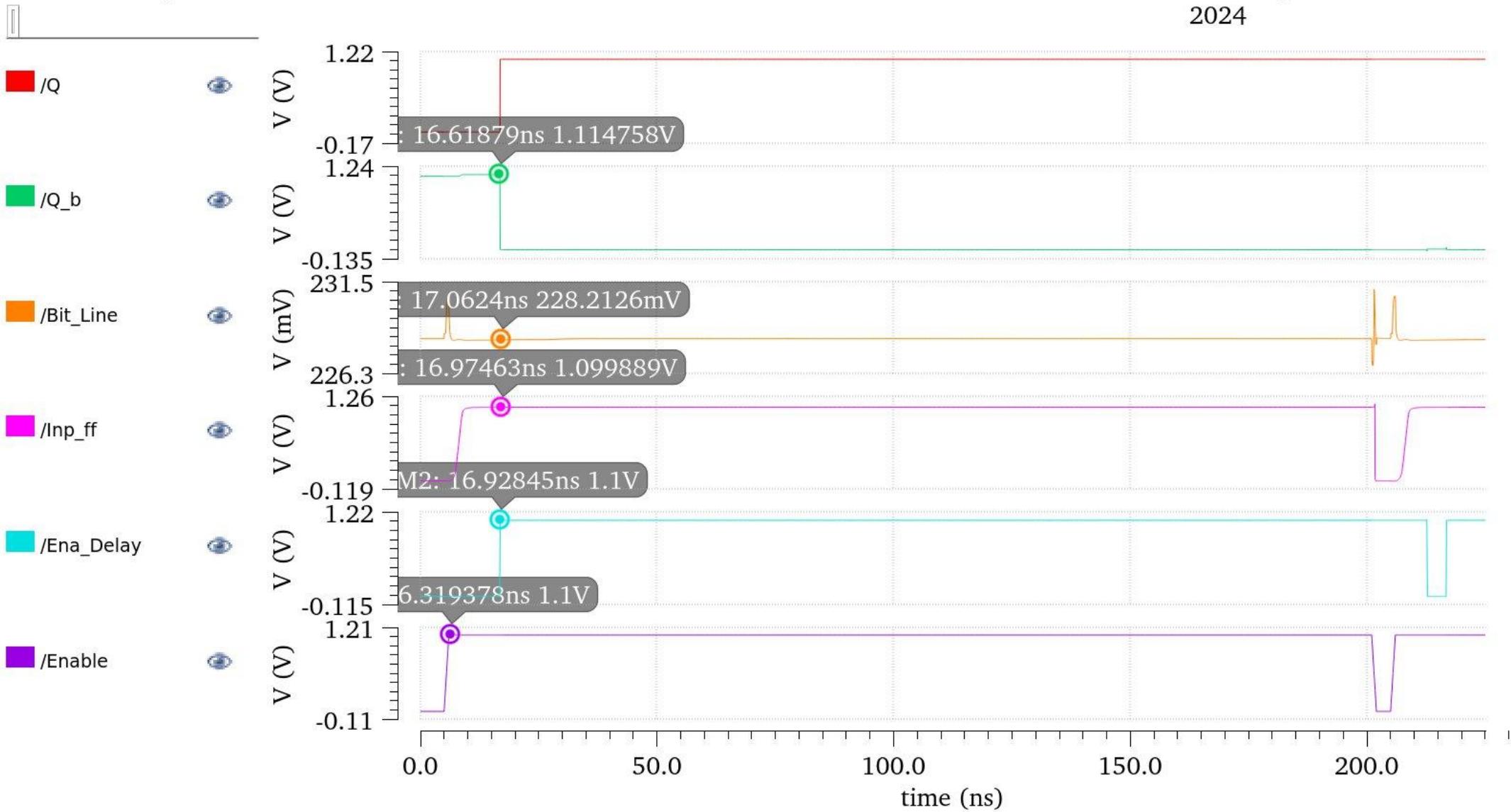
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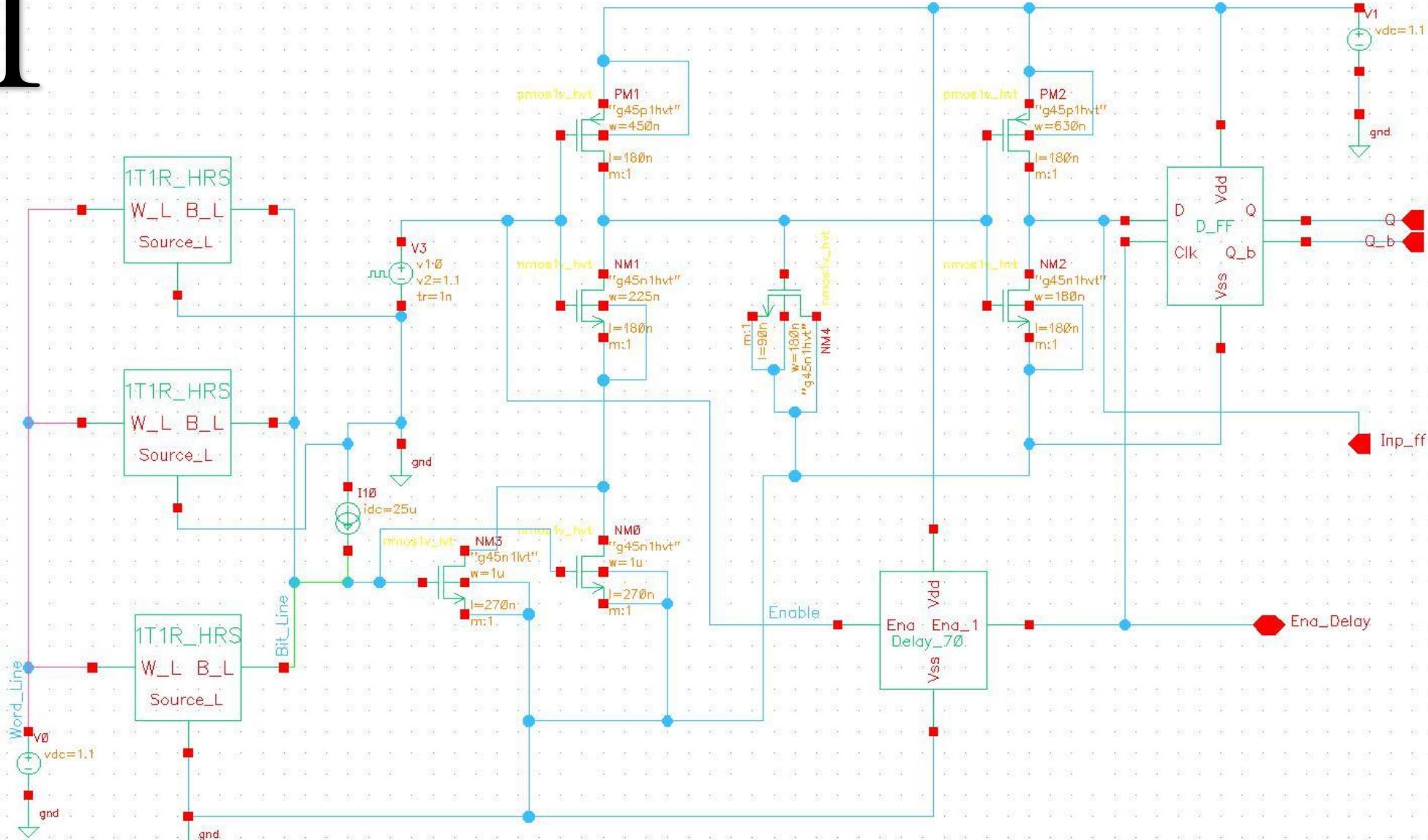
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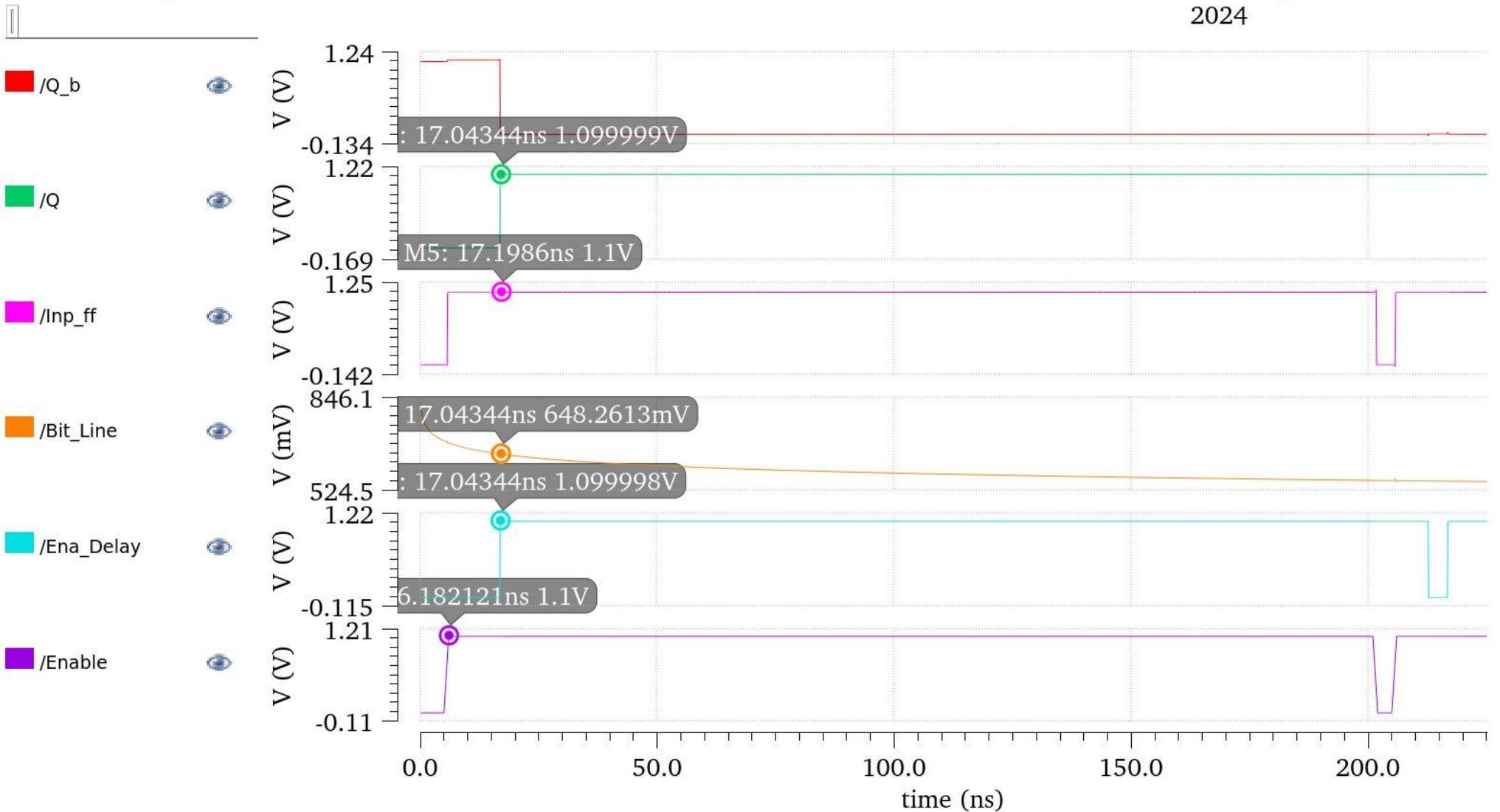
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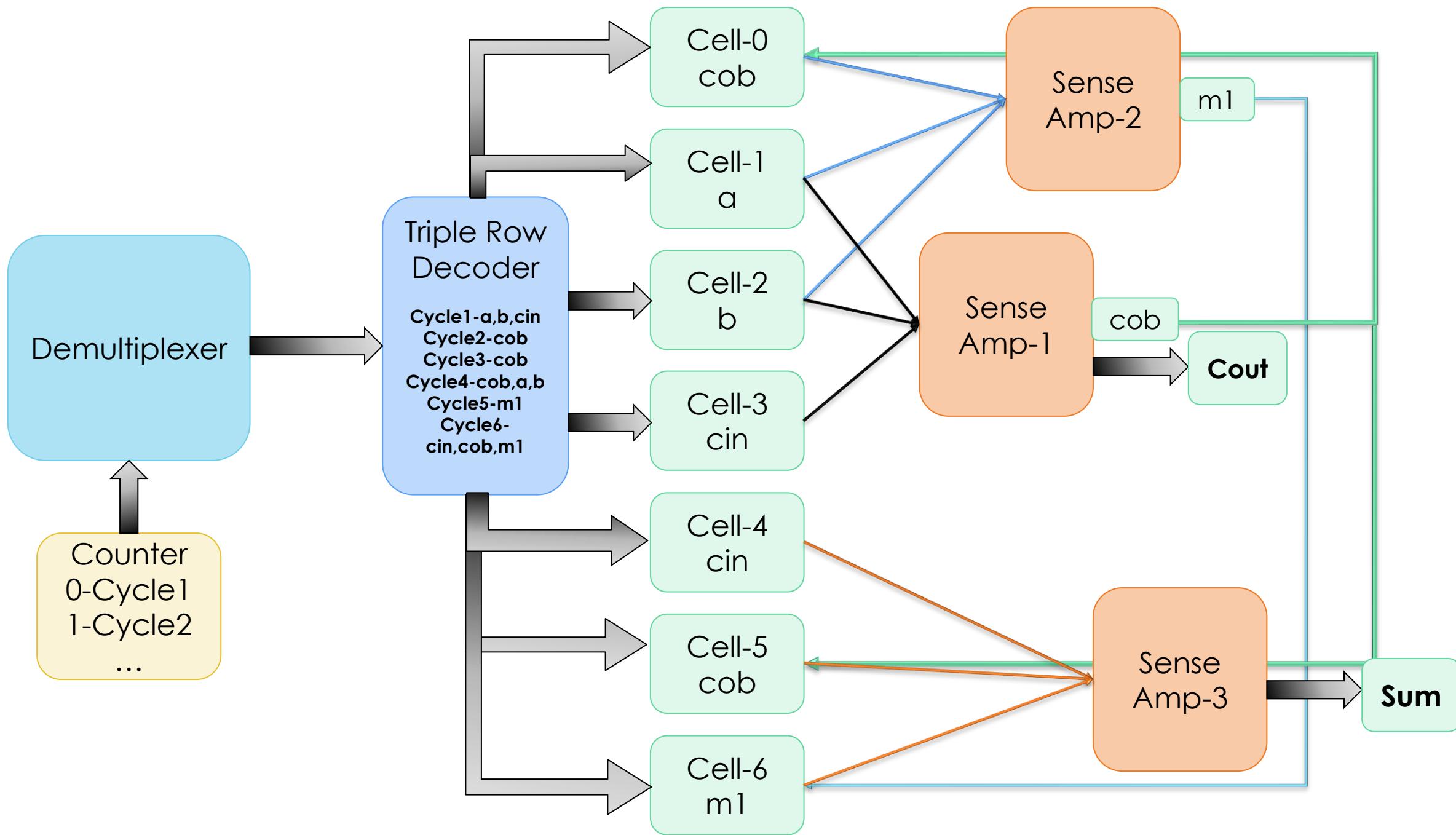


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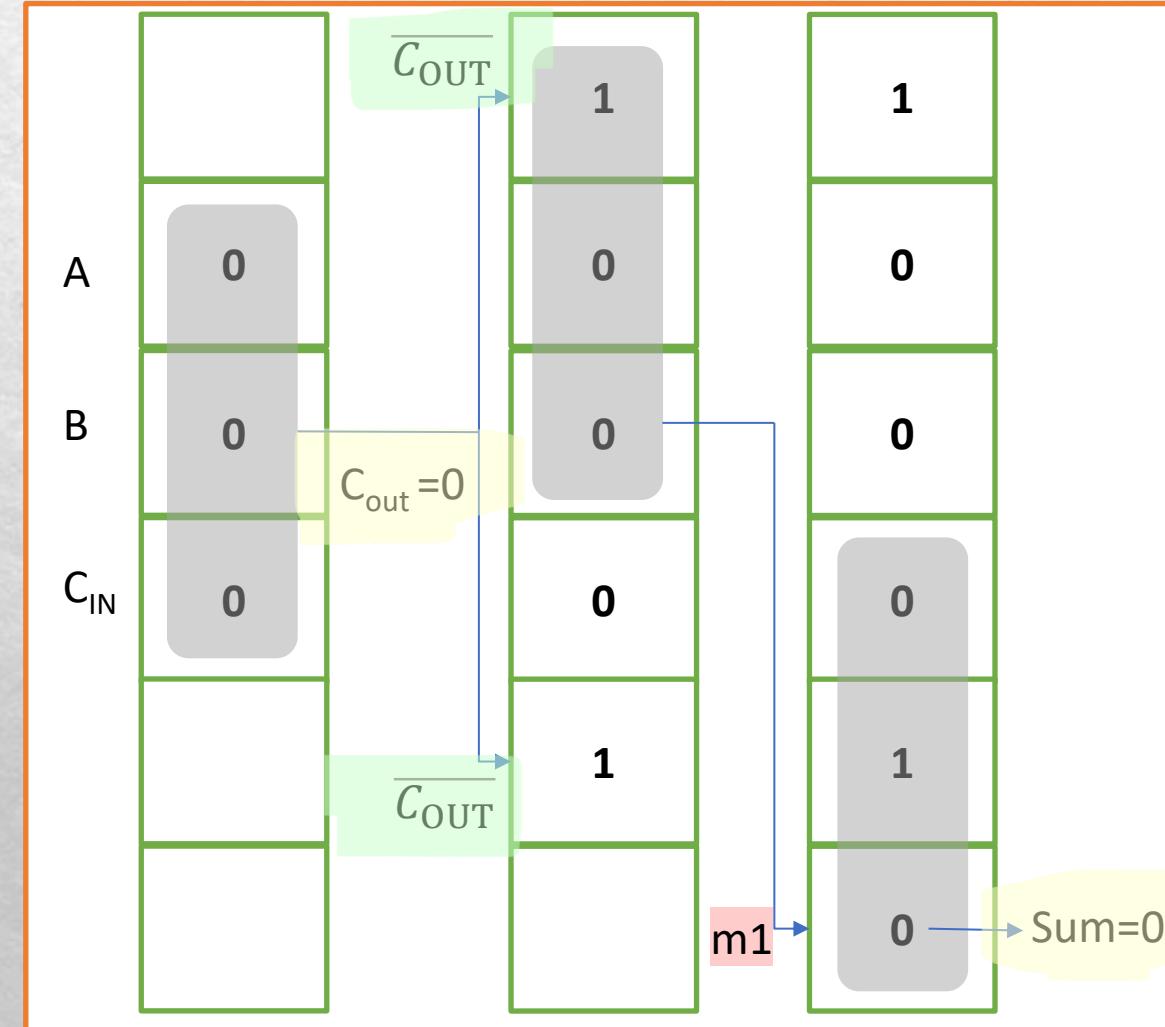
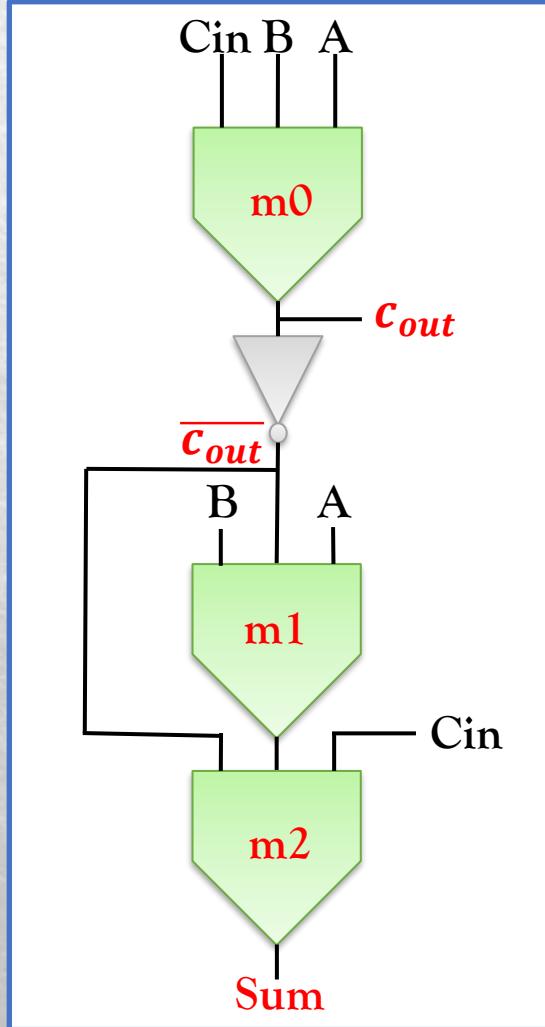
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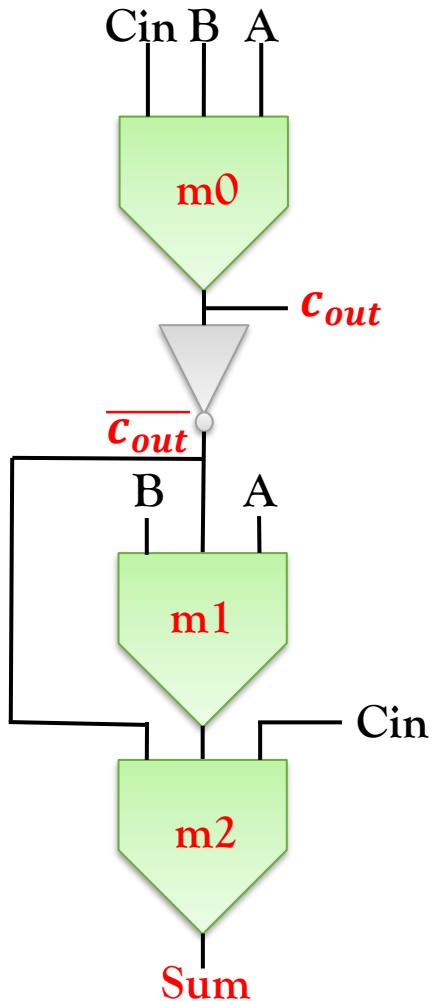
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Full Adder using Majority Gate 000



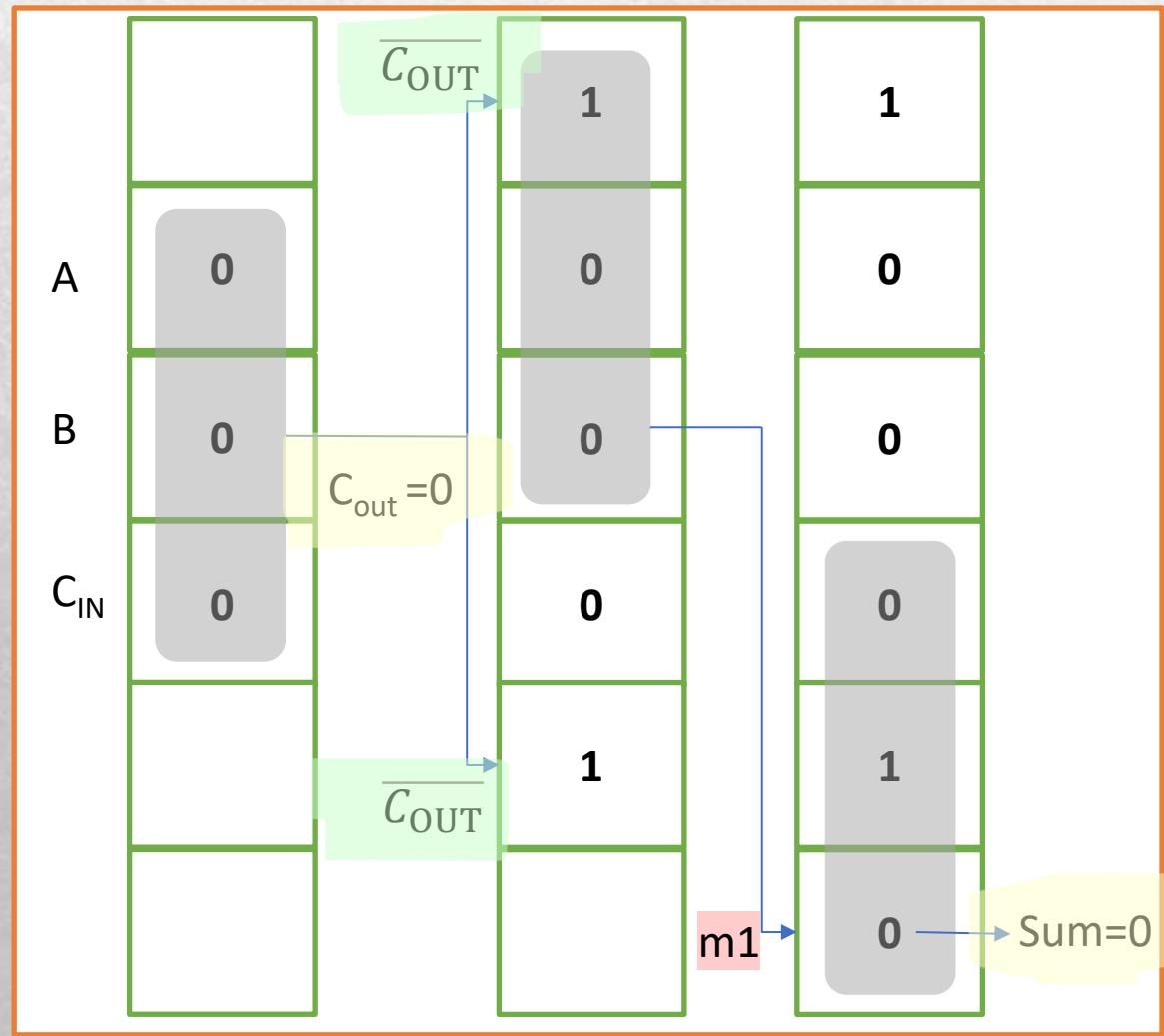


	cob		cob		
a			a		
b			b		
cin					cin
		cob			cob
				m1	m1

Step-1 : Making
A=HRS, B=HRS,
 $C_{IN}=HRS$

Step-2 : Reading
A=HRS, B=HRS,
 $C_{IN}=HRS$

Step-3 : Making/Reading
 $\overline{C_{OUT}}(1)$ and $\overline{C_{OUT}}(5)$ as LRS



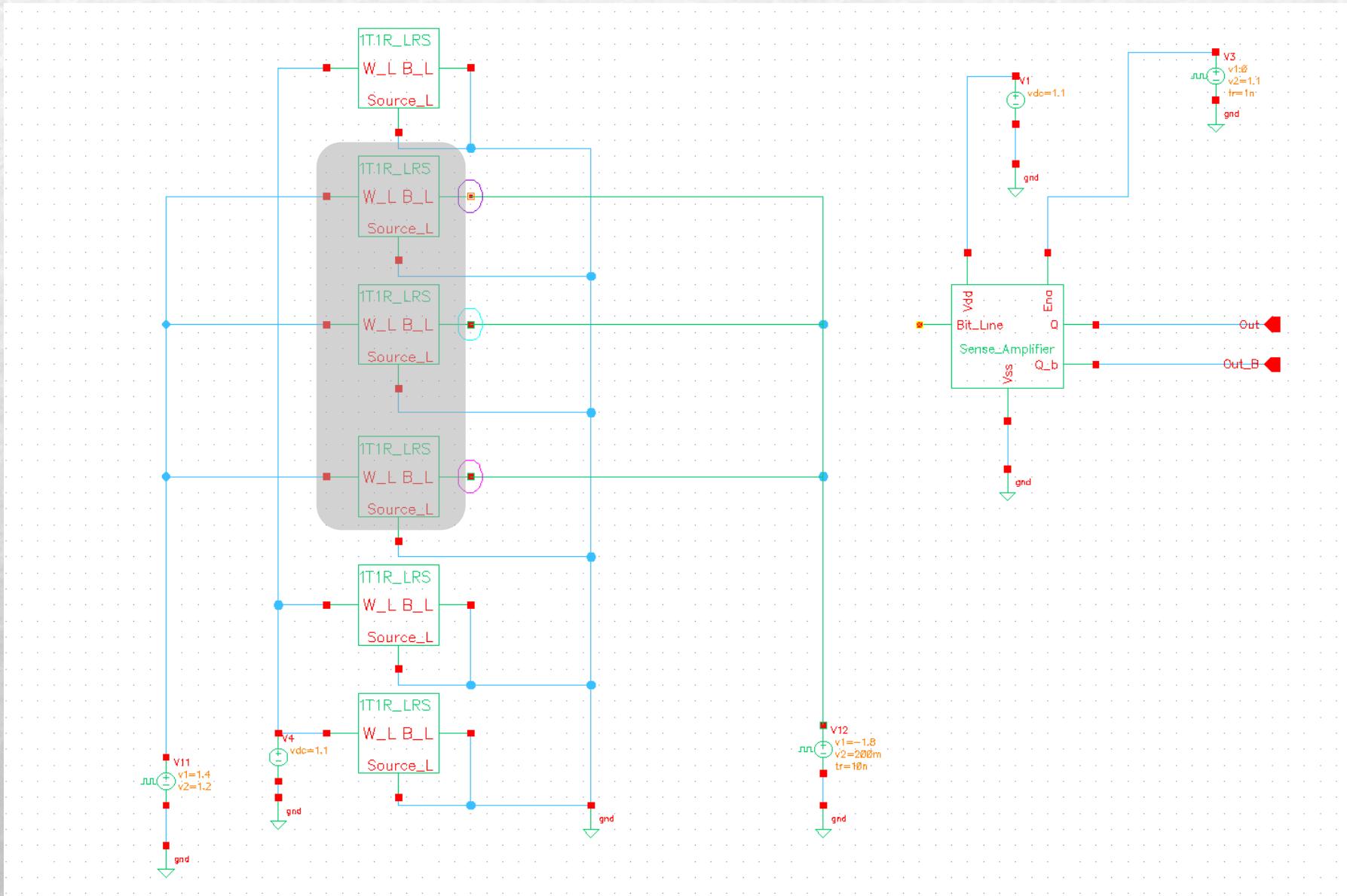
Step-4 : Reading
A=HRS, B=HRS,
 $\overline{C_{OUT}} = LRS$

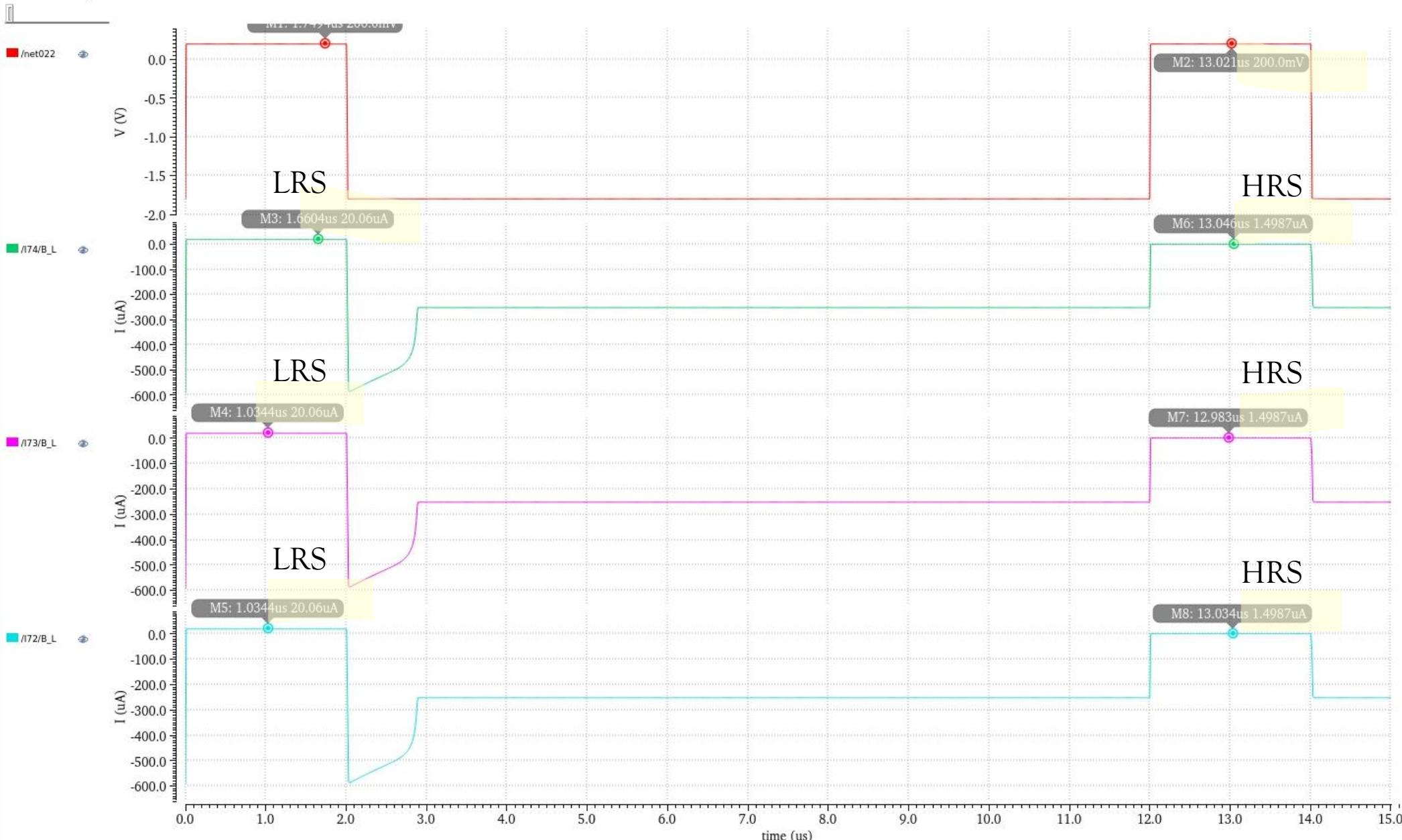
Step-5 : Making $m1(6)$
=HRS

Step-6 : Reading $\overline{C_{OUT}}=LRS$,
 $m1=HRS$, $C_{IN}=HRS$

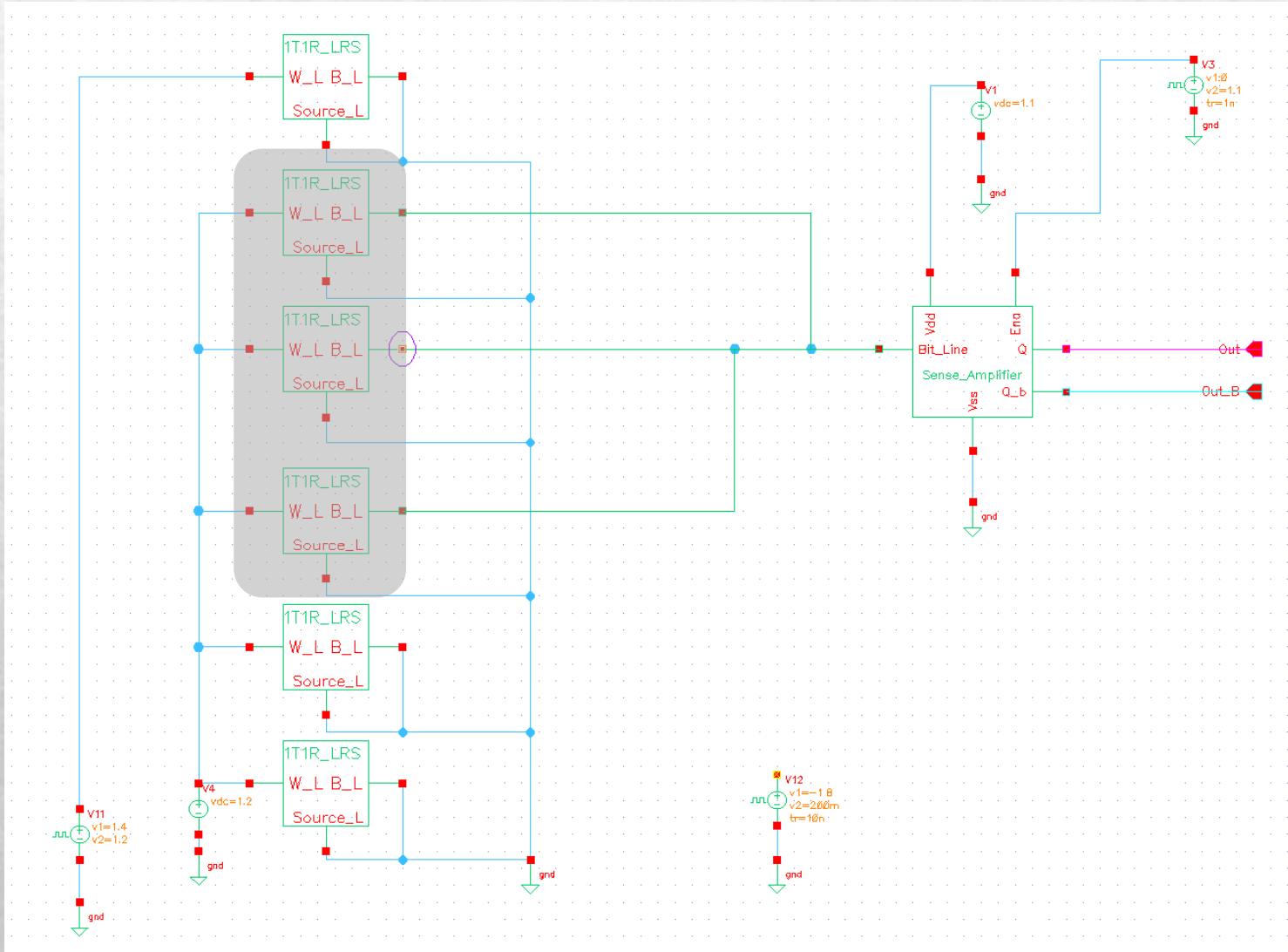
Step-1 : Making A=HRS, B=HRS, C_{IN}=HRS

- Initializing all as LRS



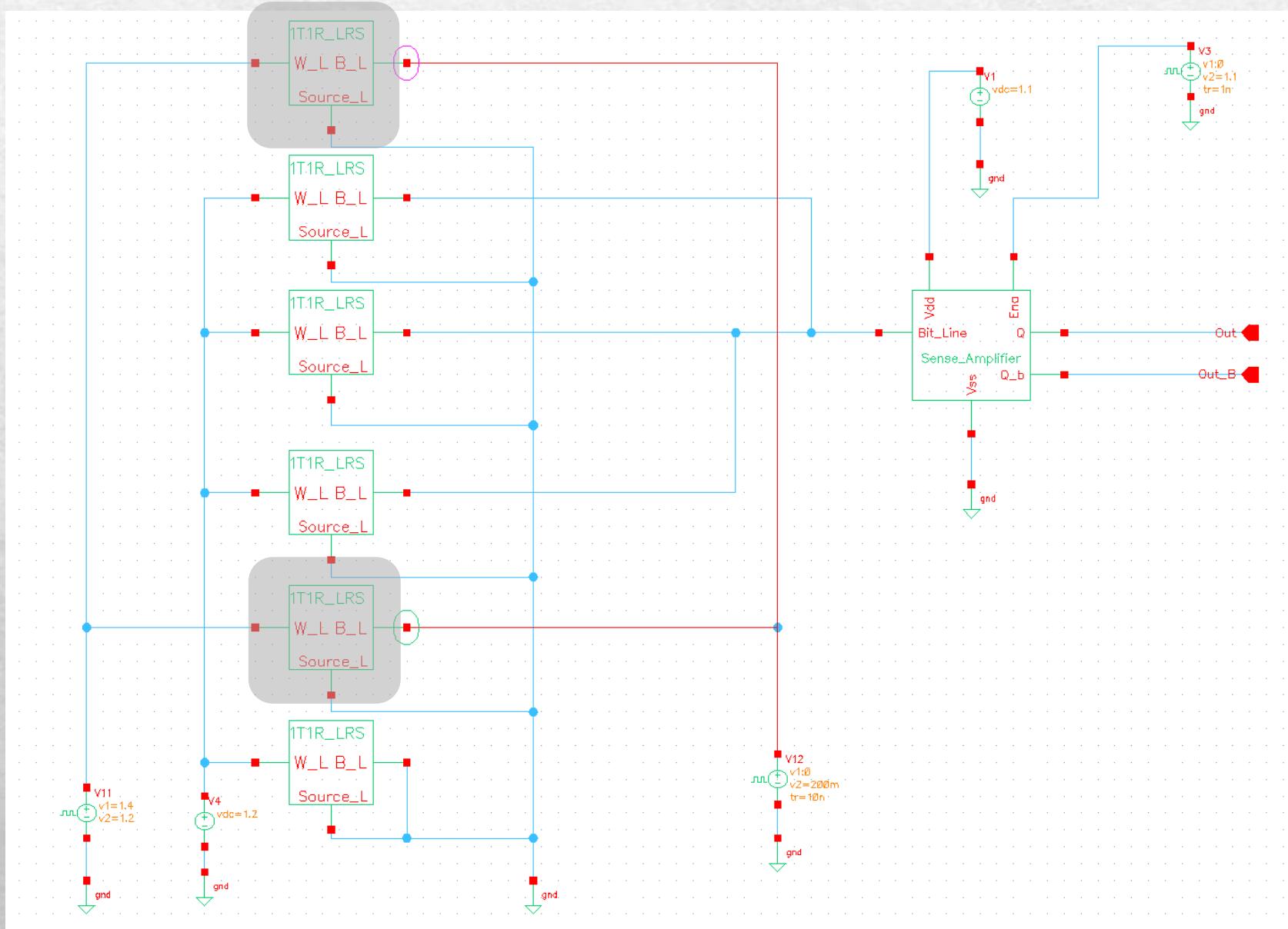


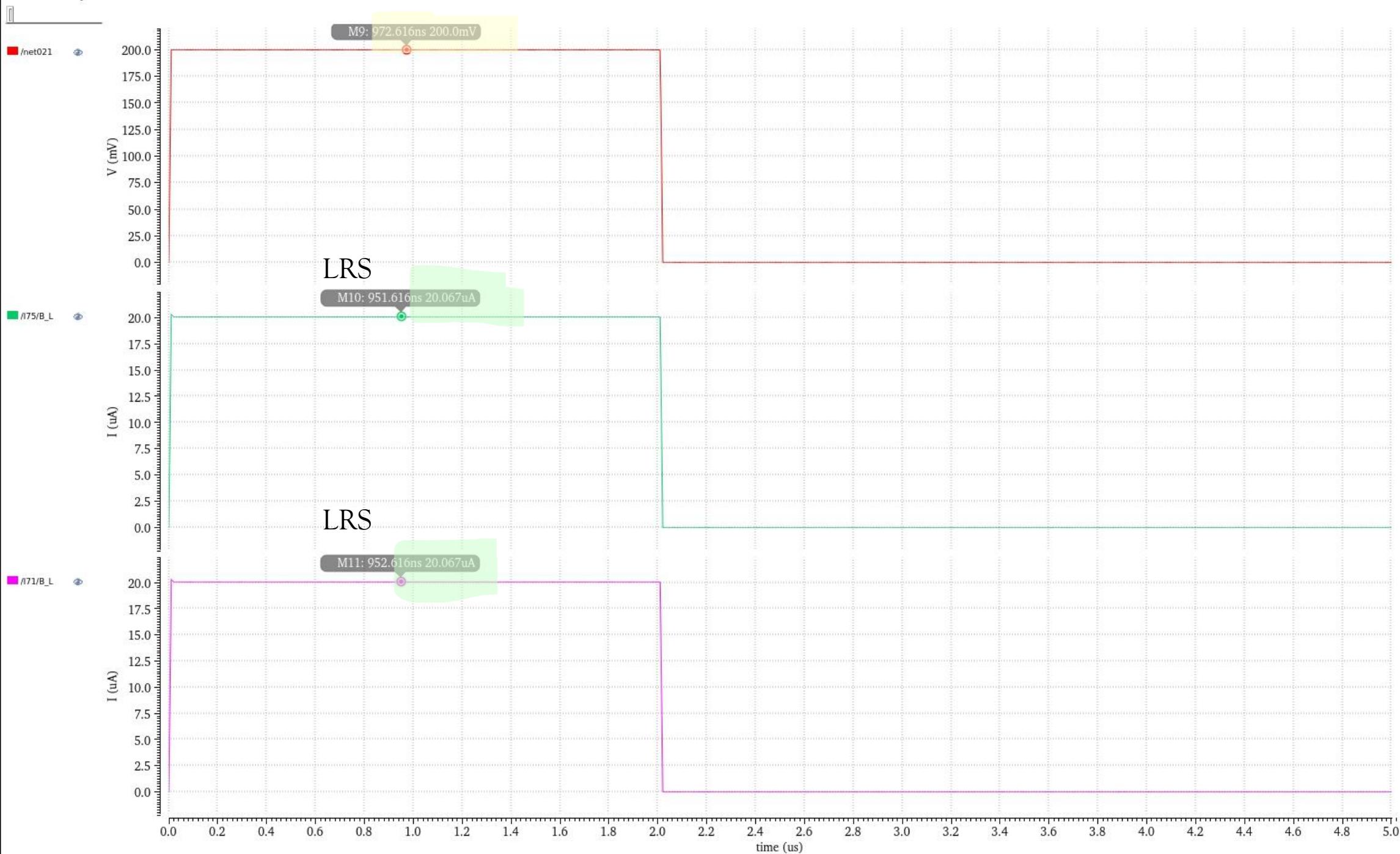
Step-2 : Reading A=HRS, B=HRS, C_{IN}=HRS



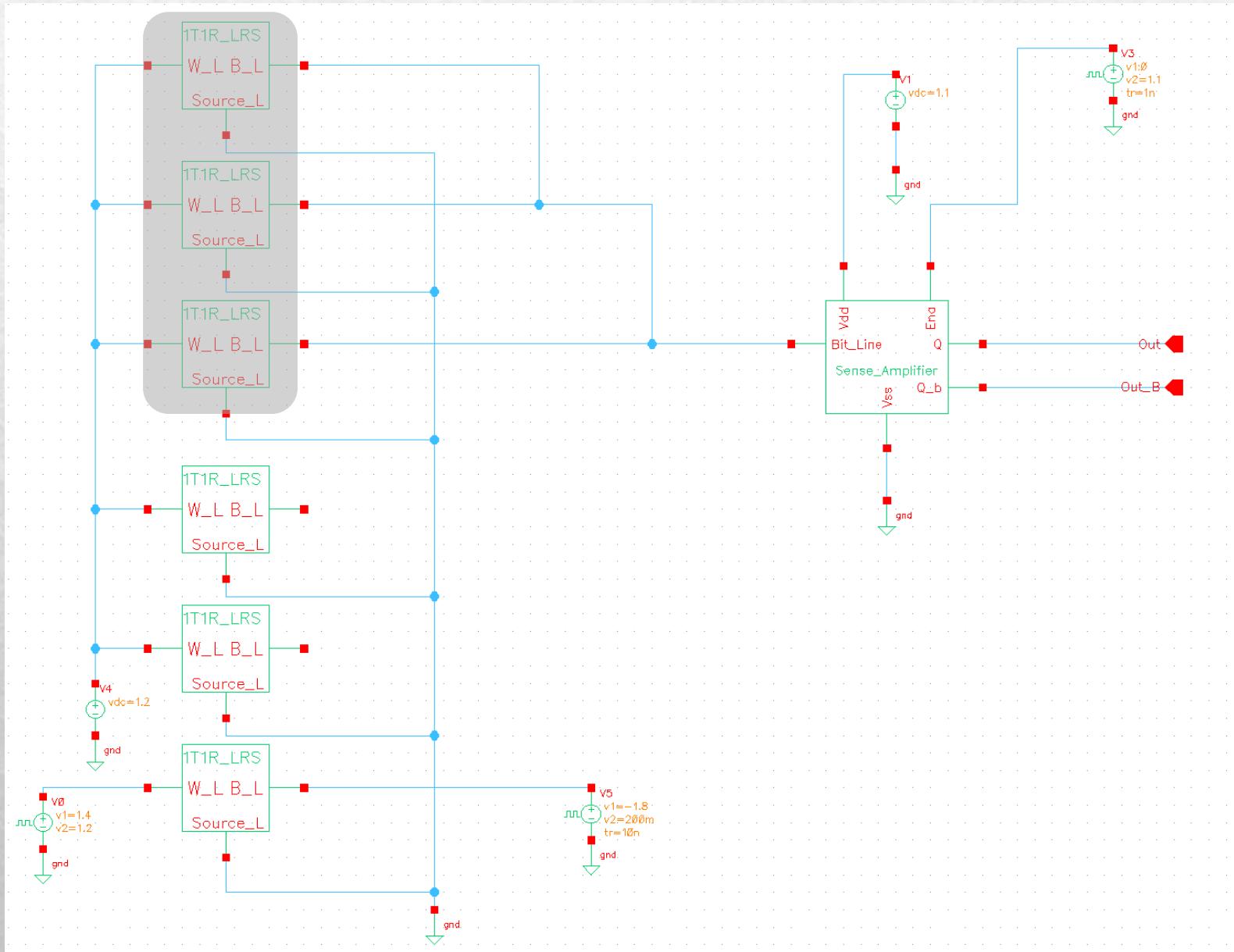


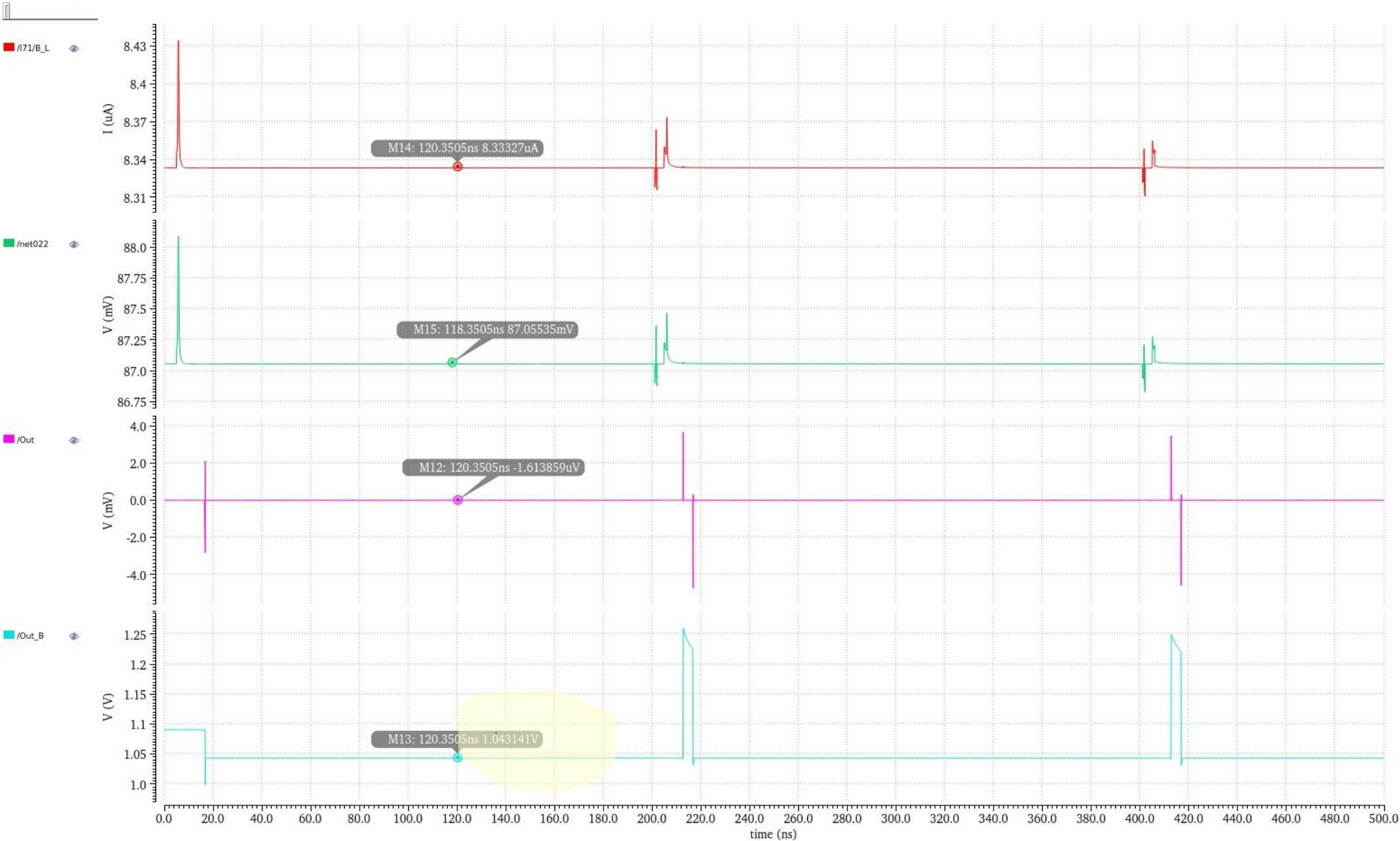
Step-3 : Making/Reading $\overline{C_{OUT}}(1)$ and $\overline{C_{OUT}}(5)$ as LRS



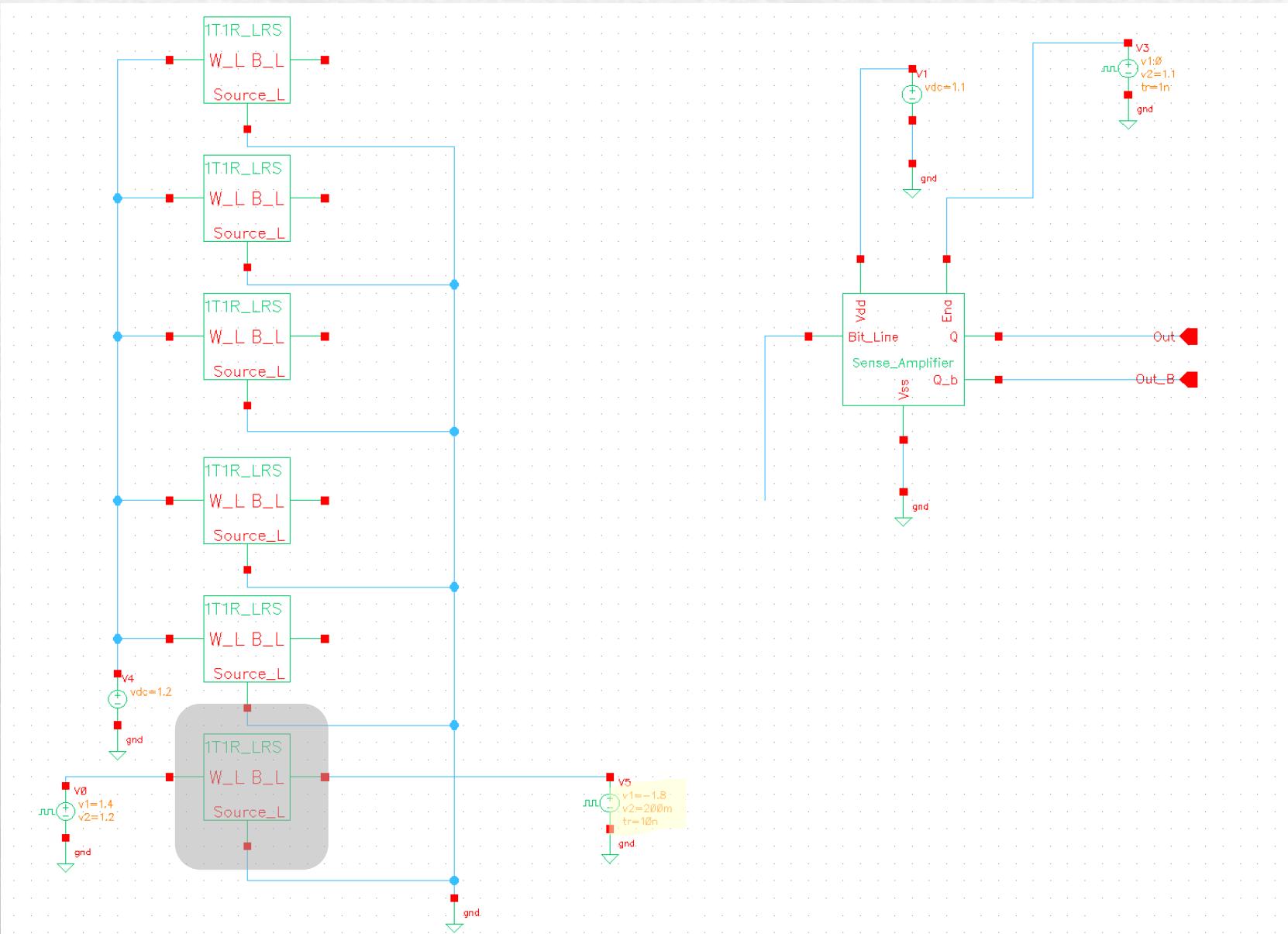


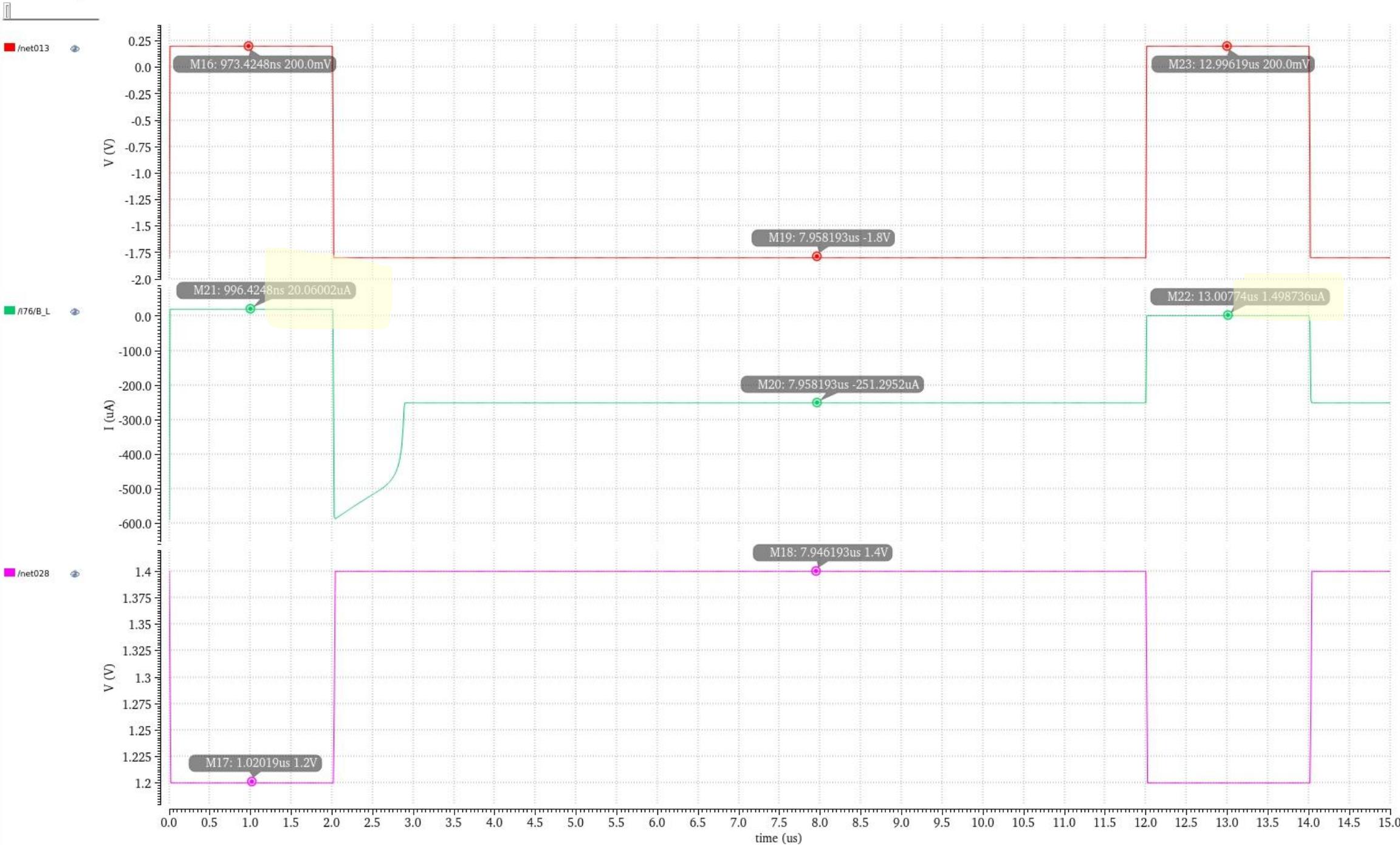
Step-4 : Reading A=HRS, B=HRS, $\overline{C_{OUT}}$ =LRS



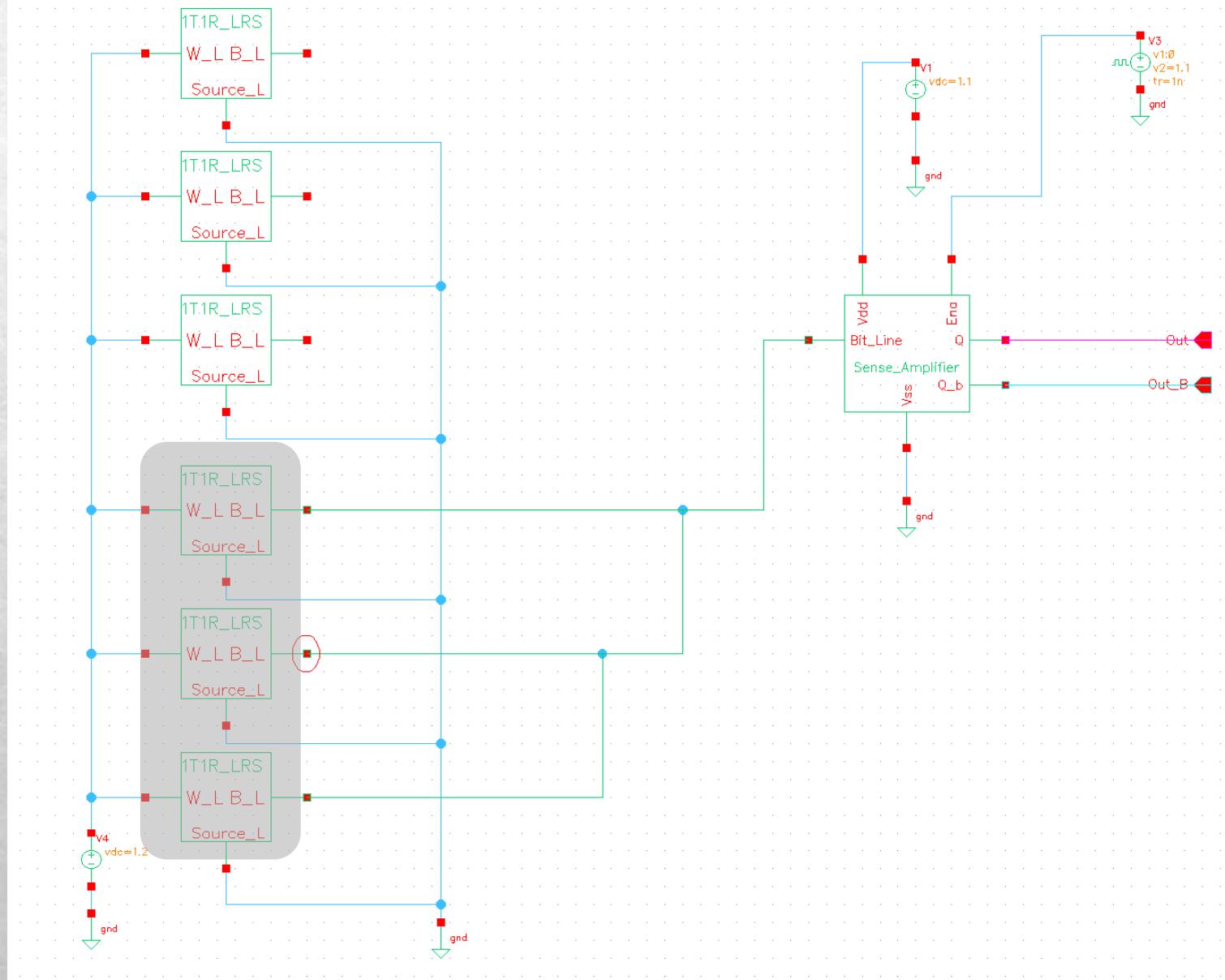


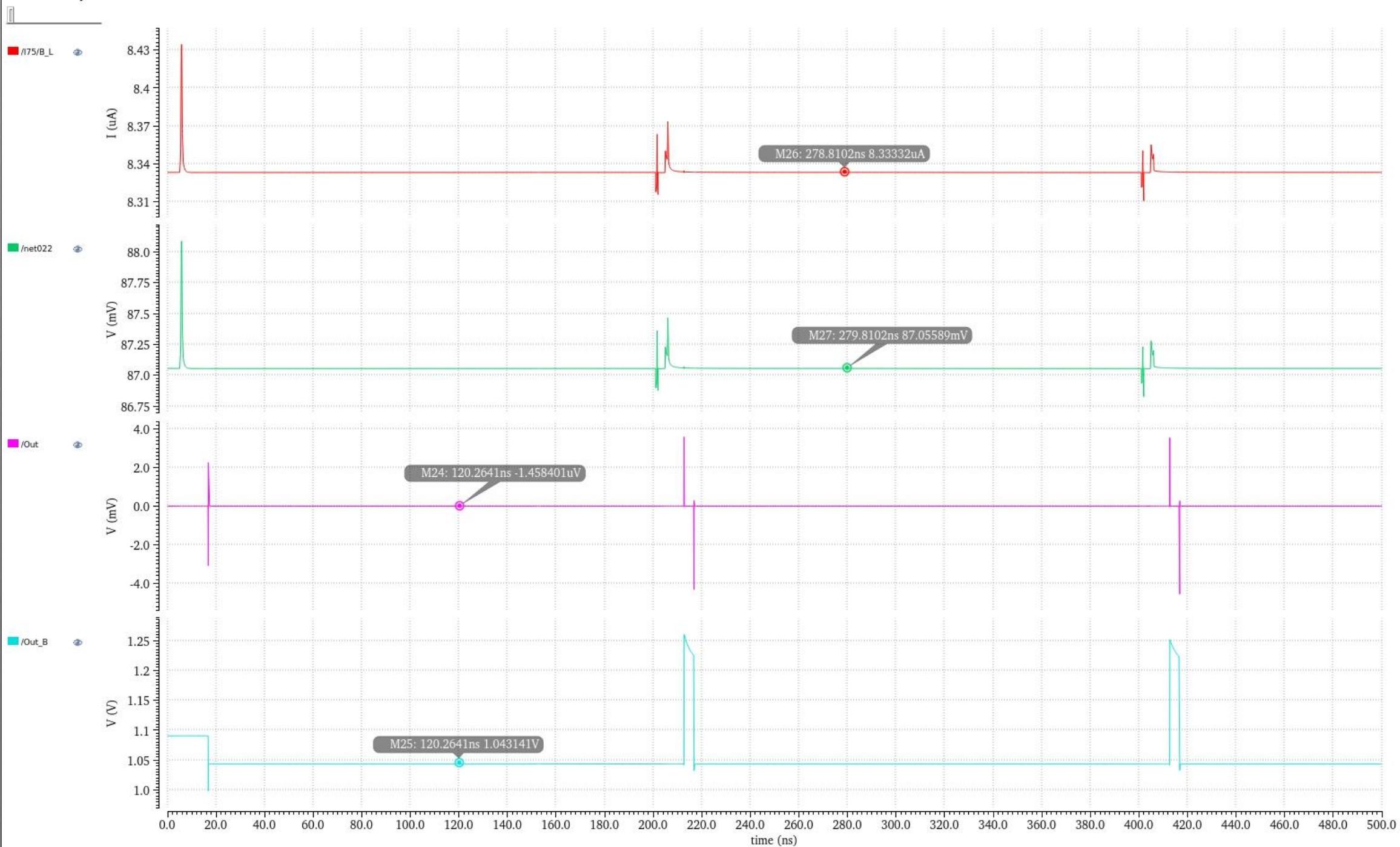
Step-5 : Making m1(6)=HRS



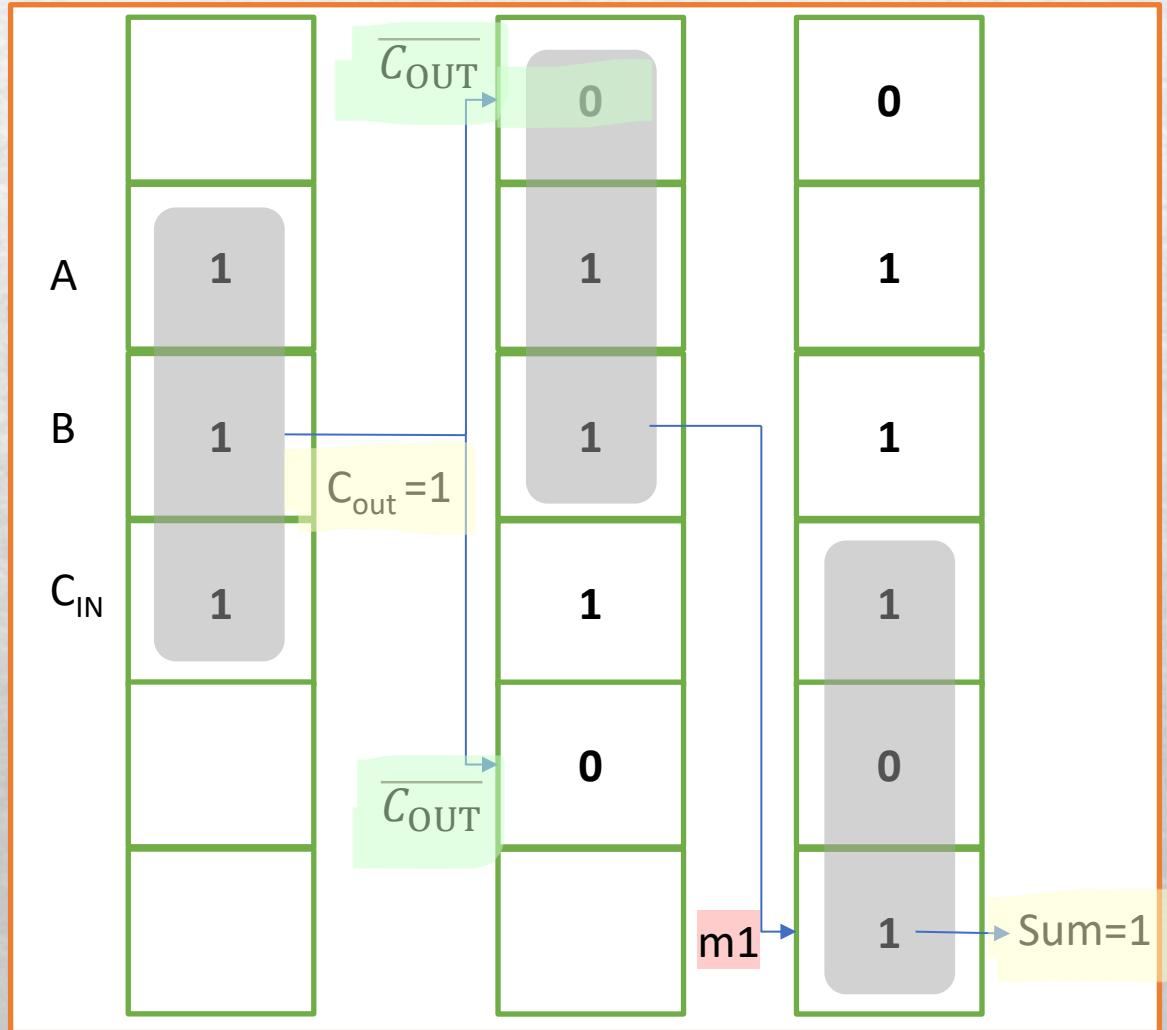
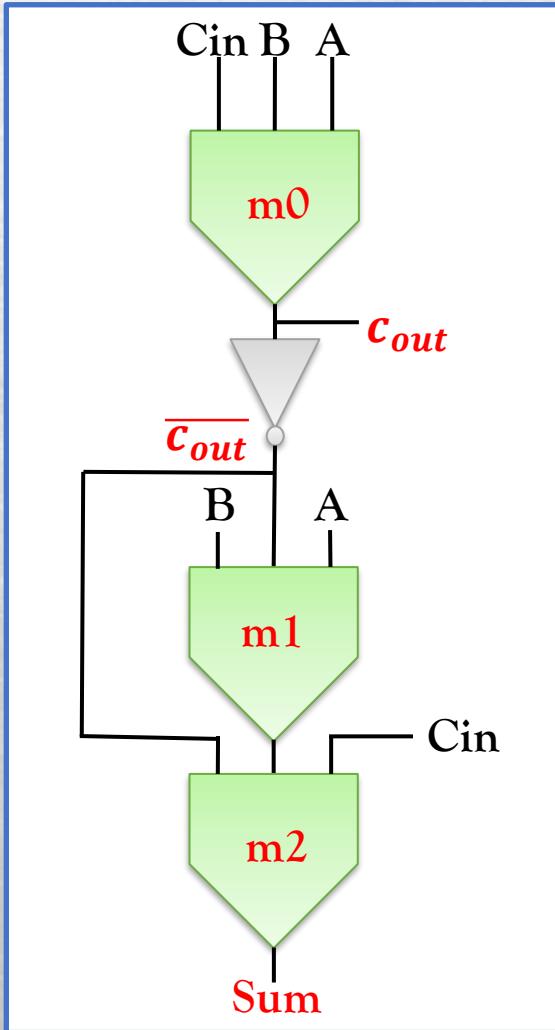


Step-6 : Reading $C_{OUT} = LRS$, m1=HRS, $C_{IN} = HRS$



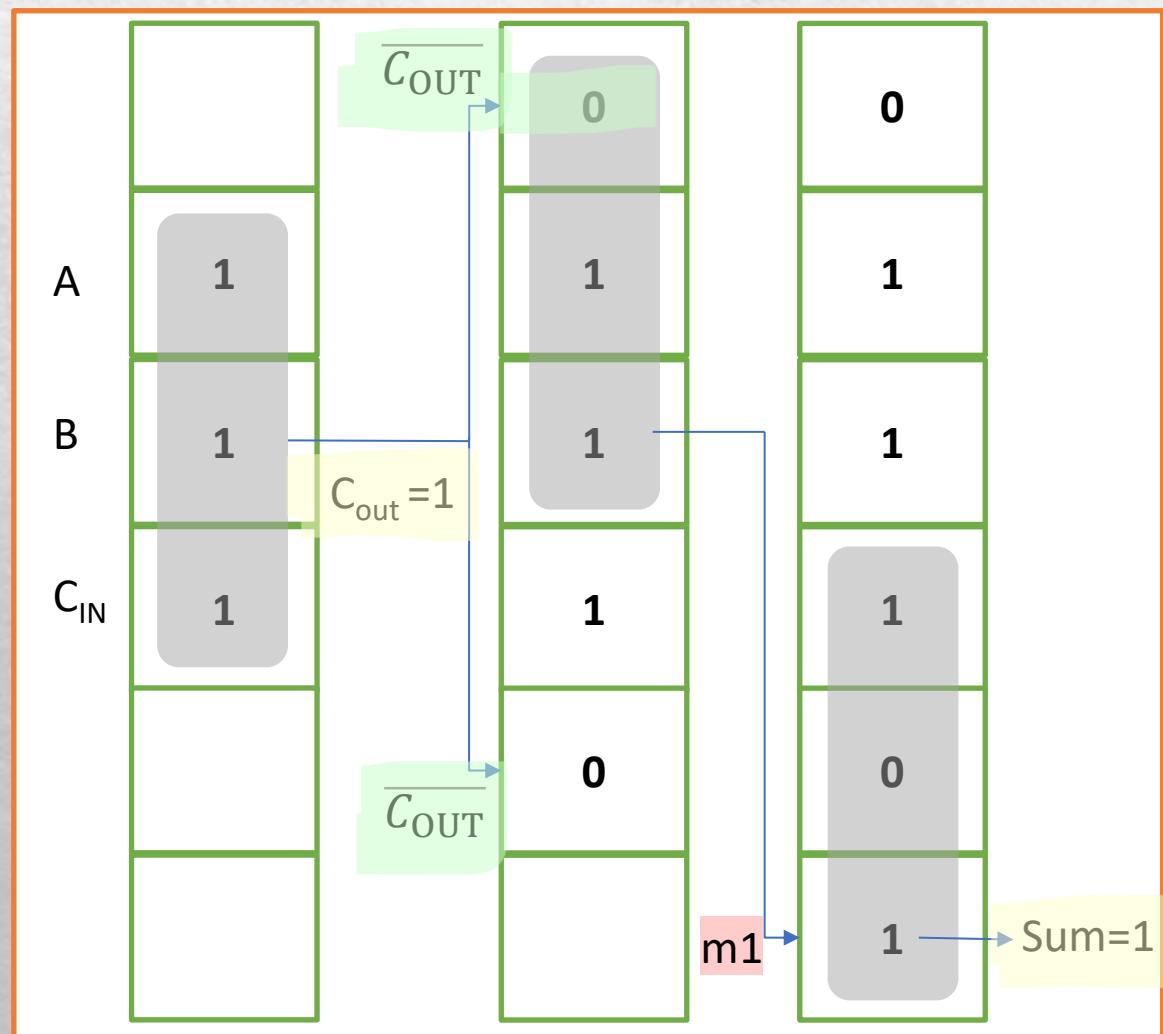


111



Step-1 : Reading
 $A=LRS$, $B=LRS$,
 $C_{IN}=LRS$

Step-2 : Making/Reading
 $\overline{C_{OUT}}(1)$ and $\overline{C_{OUT}}(5)$ as HRS

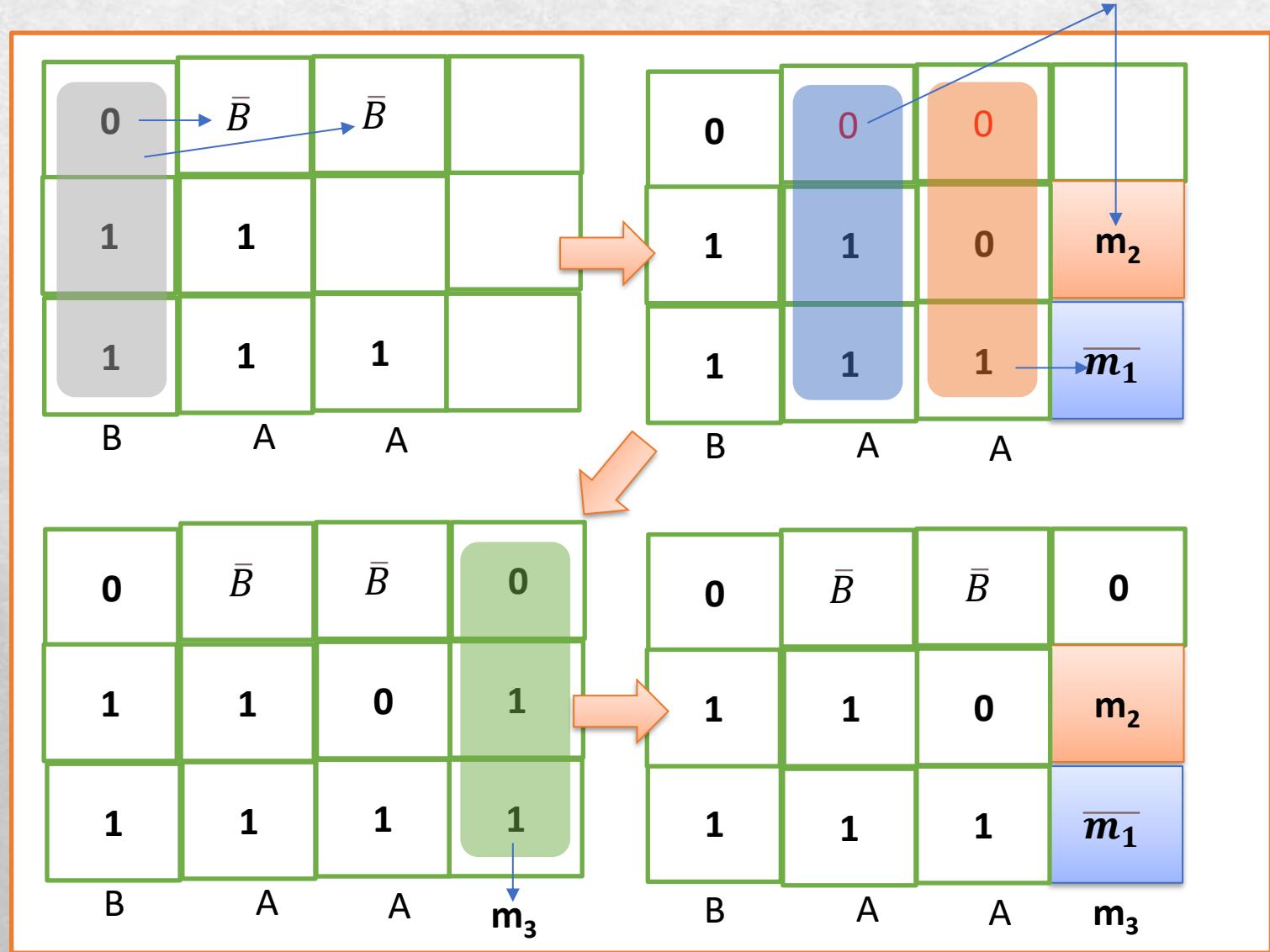
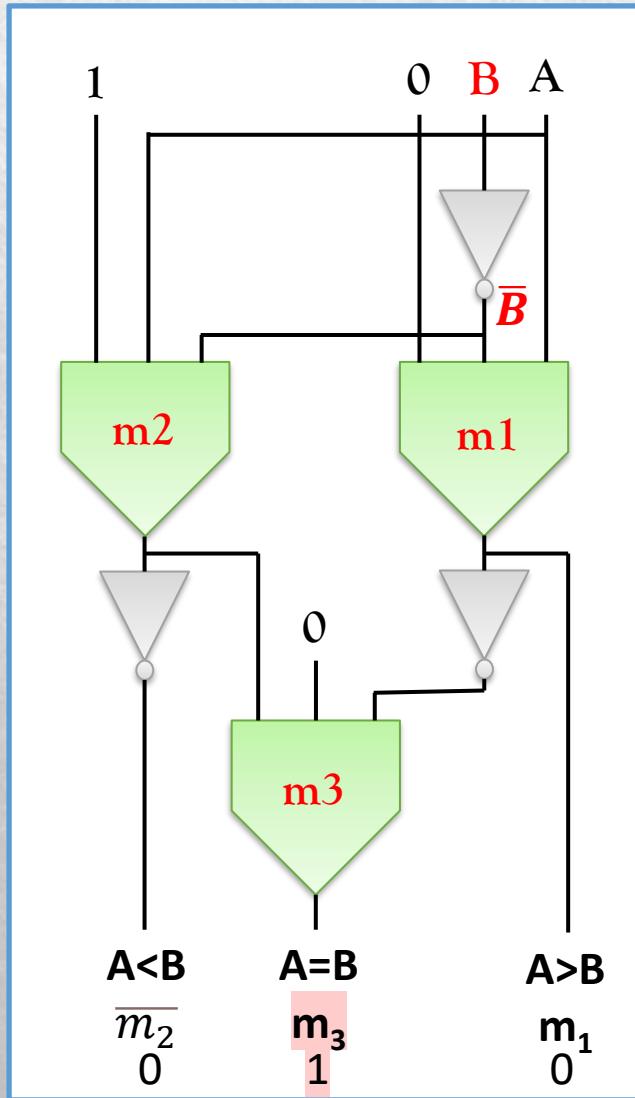


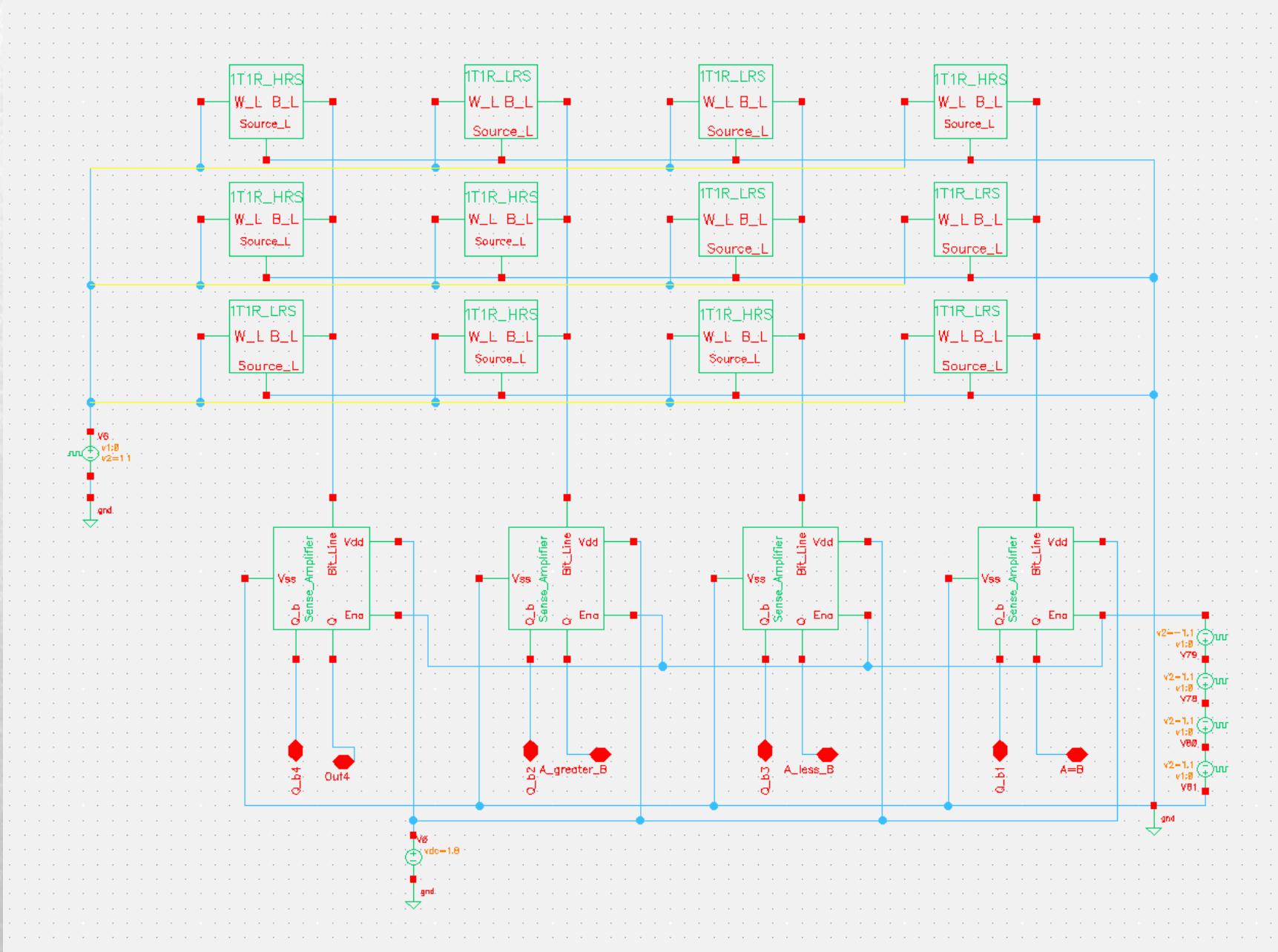
Step-3 : Reading
 $A=LRS$, $B=LRS$,
 $\overline{C_{OUT}} = HRS$

Step-4 : Making $m_1(6)$
 $=LRS$

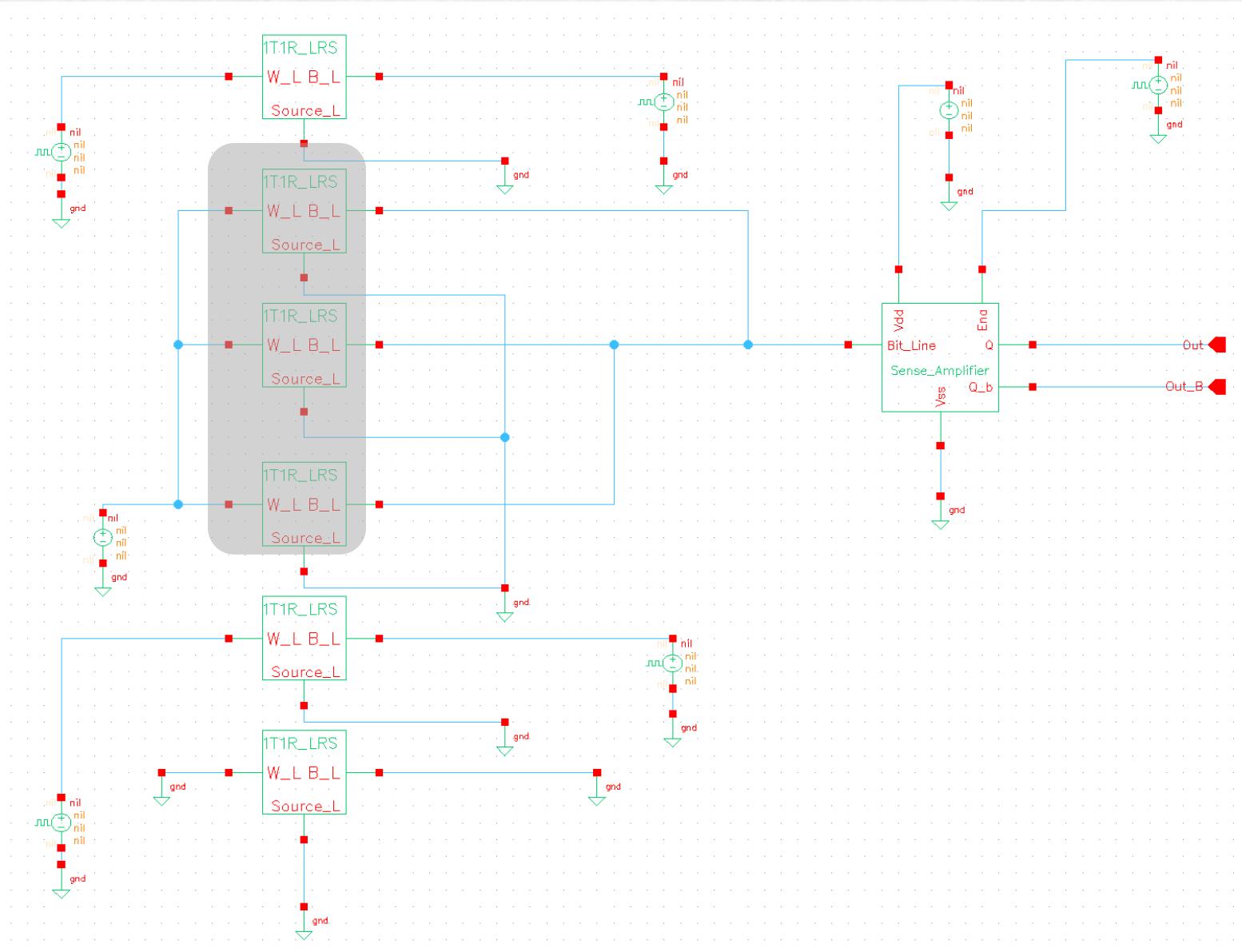
Step-5 : Reading $\overline{C_{OUT}}=HRS$,
 $m_1=LRS$, $C_{IN}=LRS$

1-bit Comparator using Majority Gate A = 1, B = 1





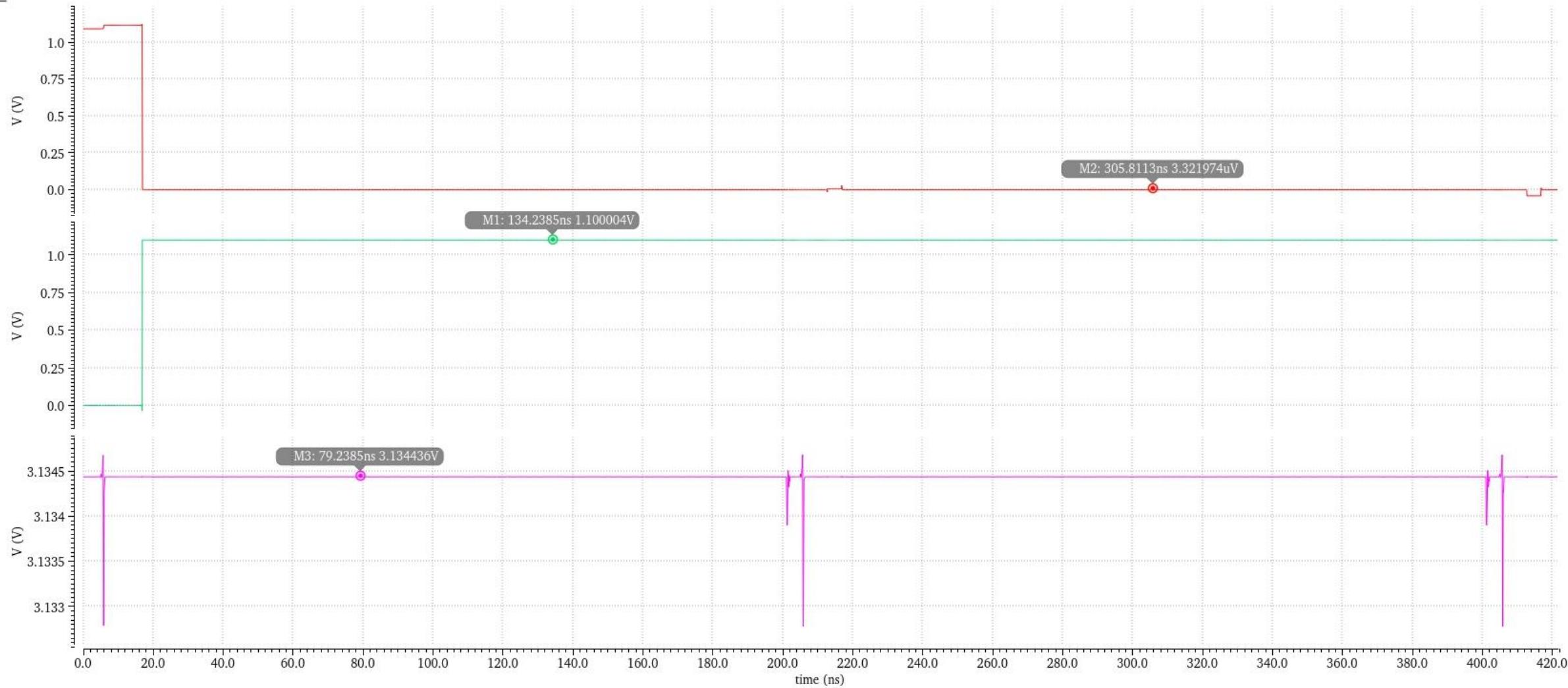
Step-1 : Reading A=LRS, B=LRS, C_{IN}=LRS



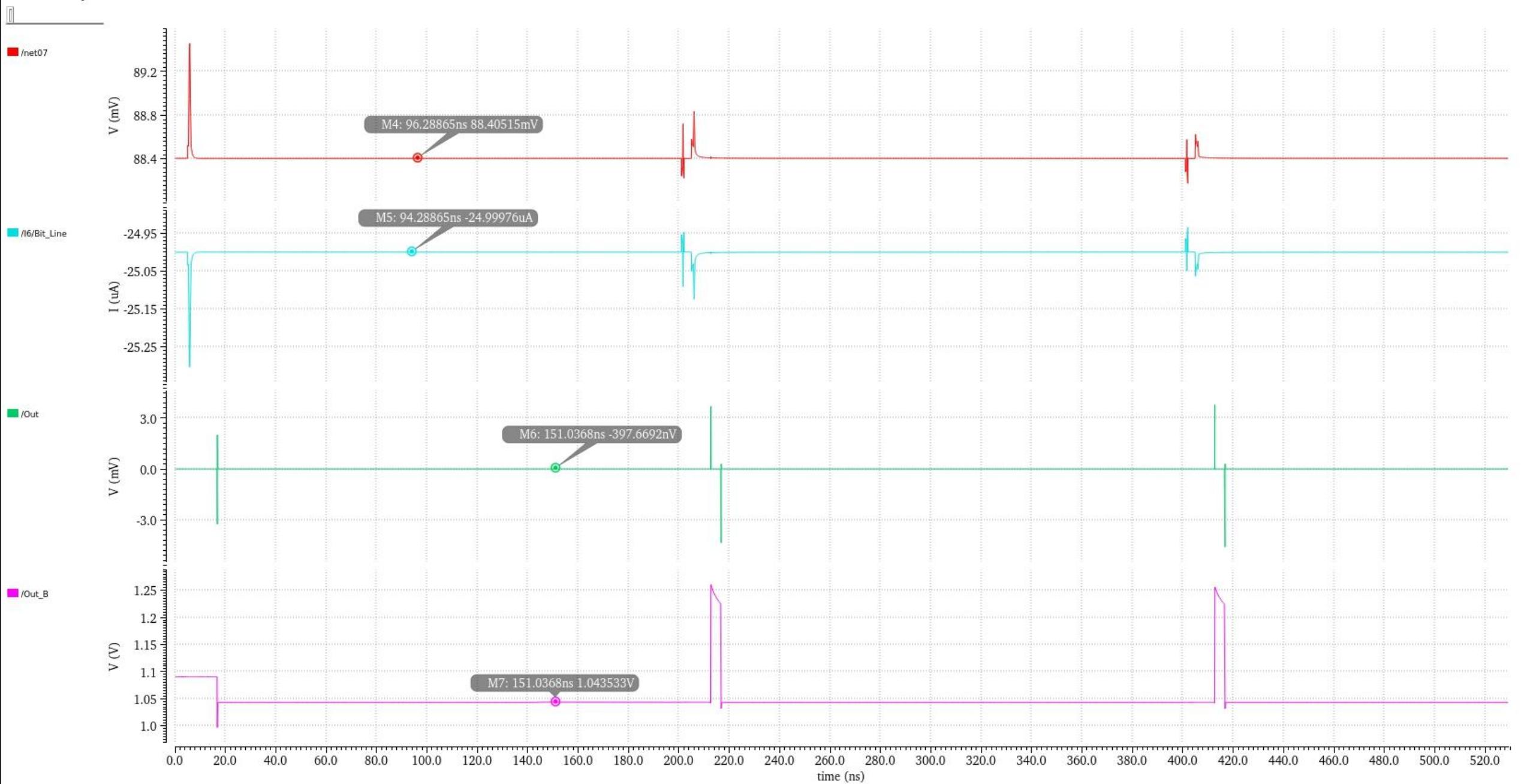
Transient Response

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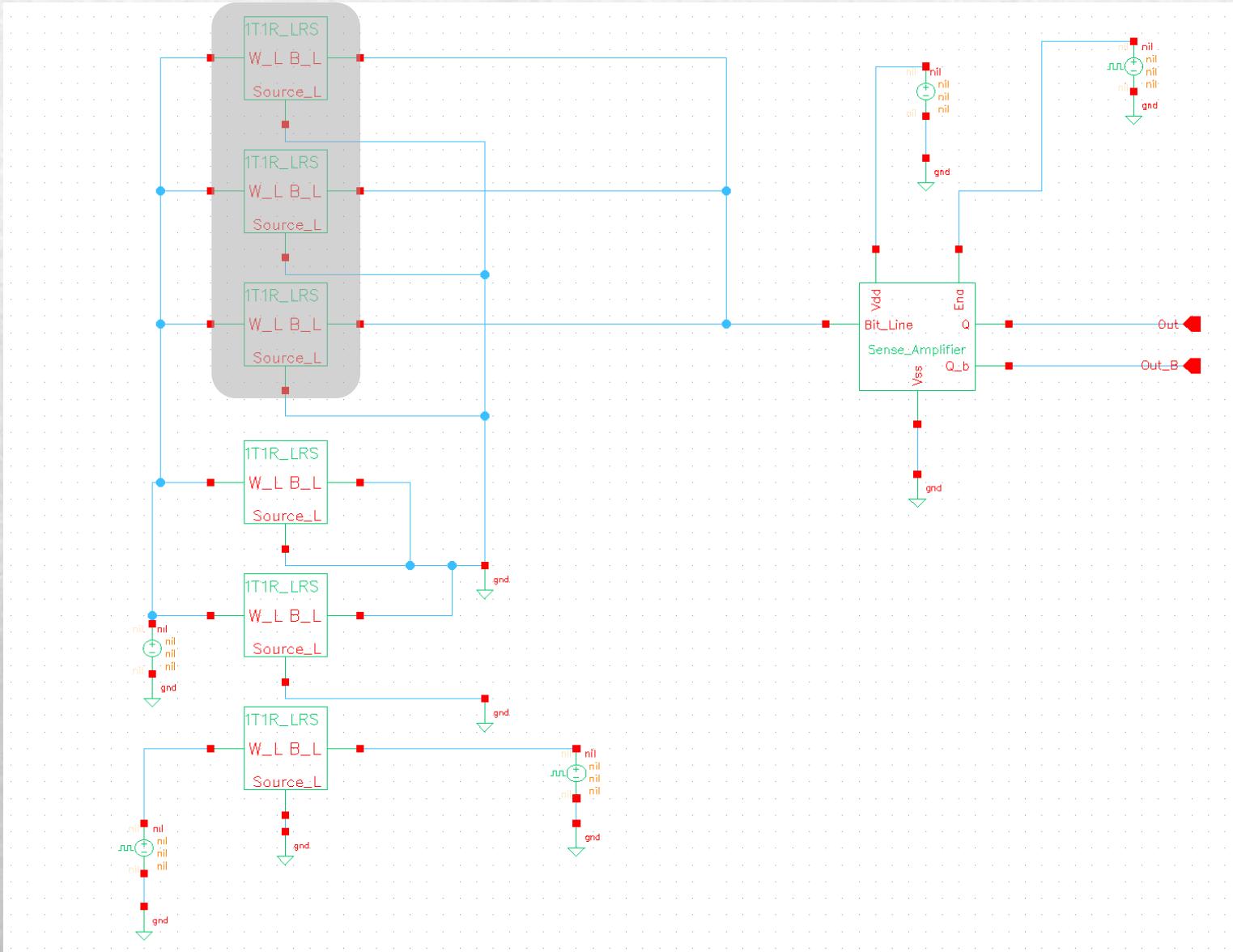
/Out_B

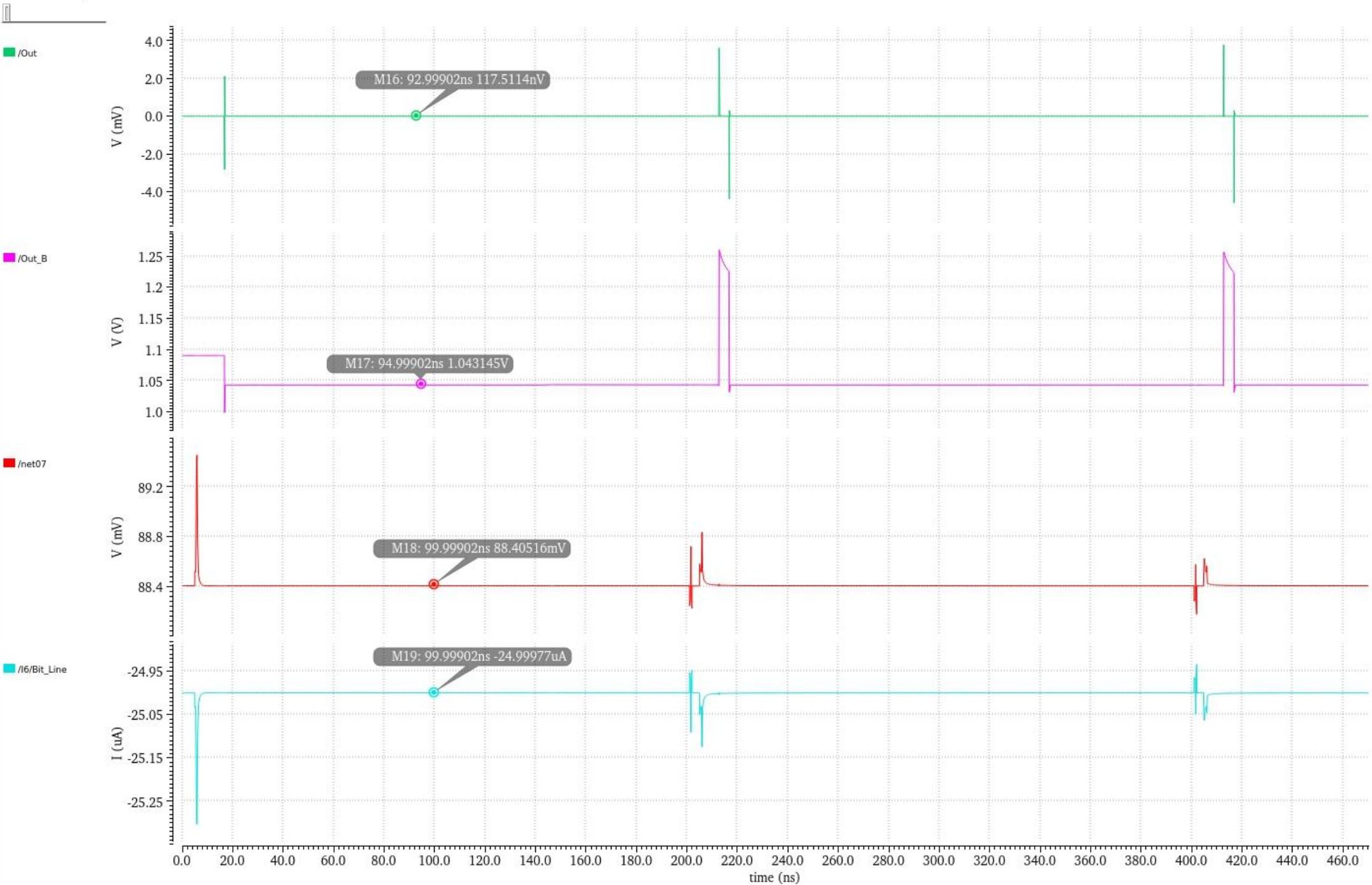


Step-2 : Making/Reading $\overline{C_{OUT}}(1)$ and $\overline{C_{OUT}}(5)$ as HRS

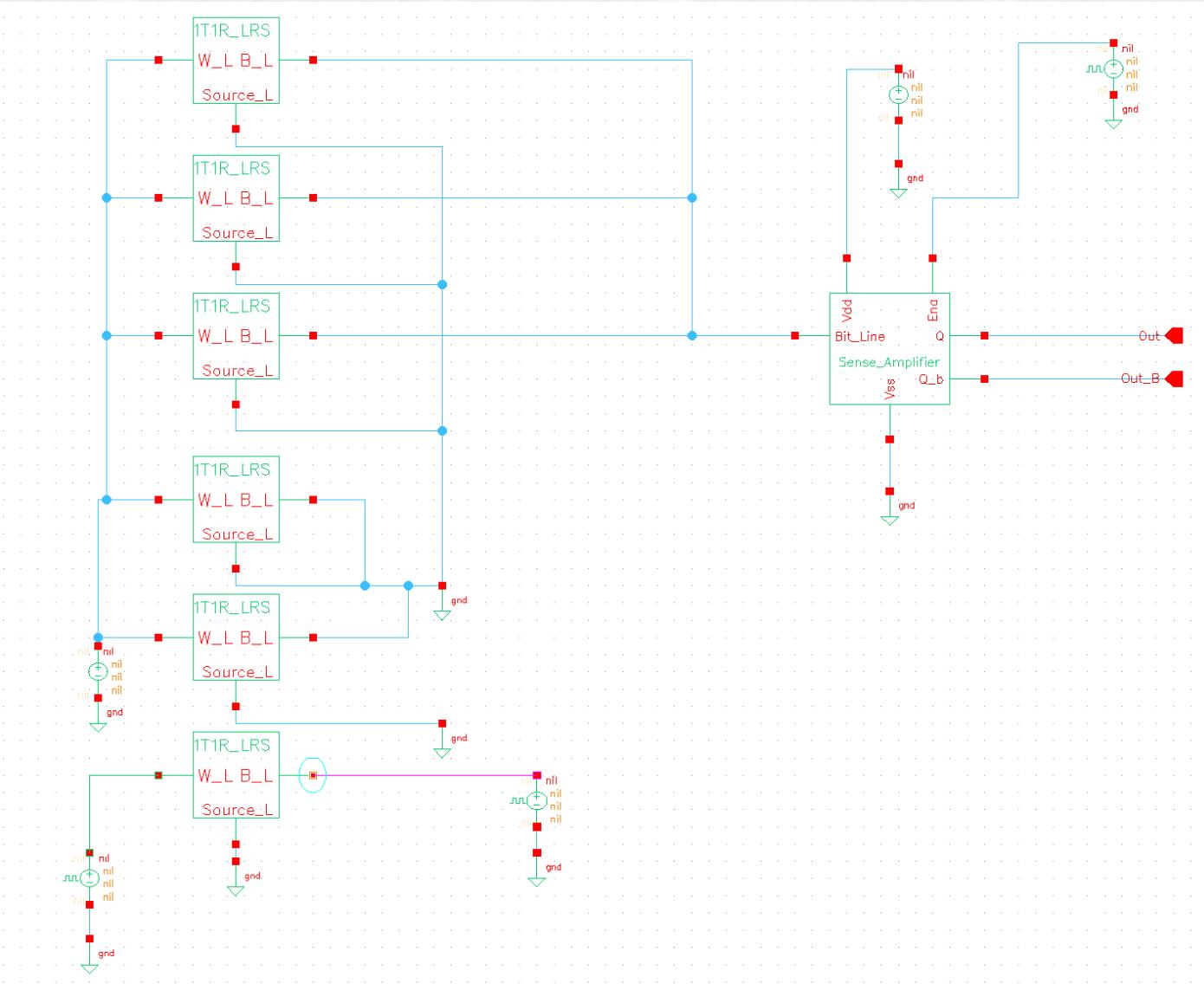


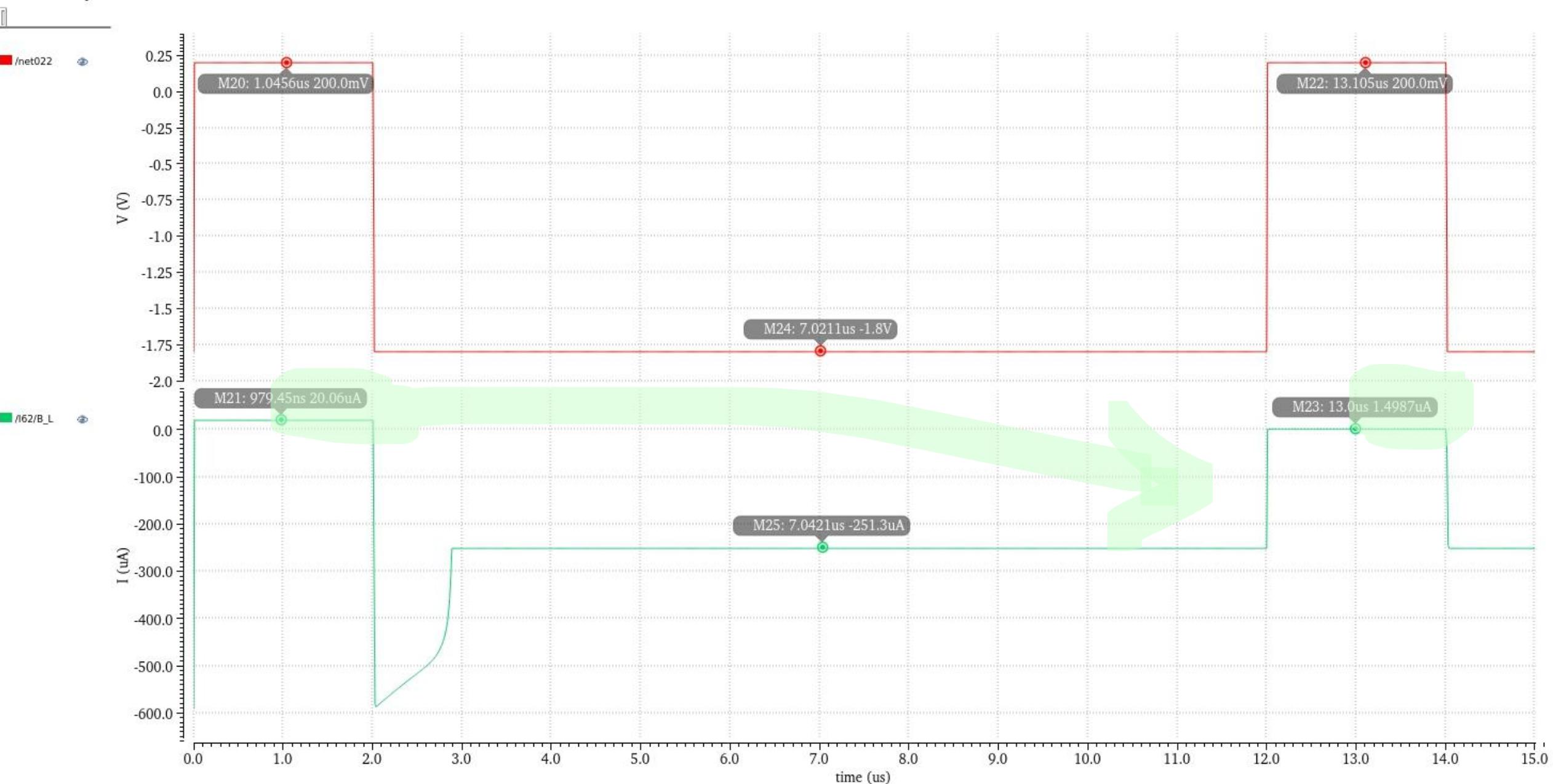
Step-3 : Reading A=LRS, B=LRS, $\overline{C_{OUT}}$ =HRS



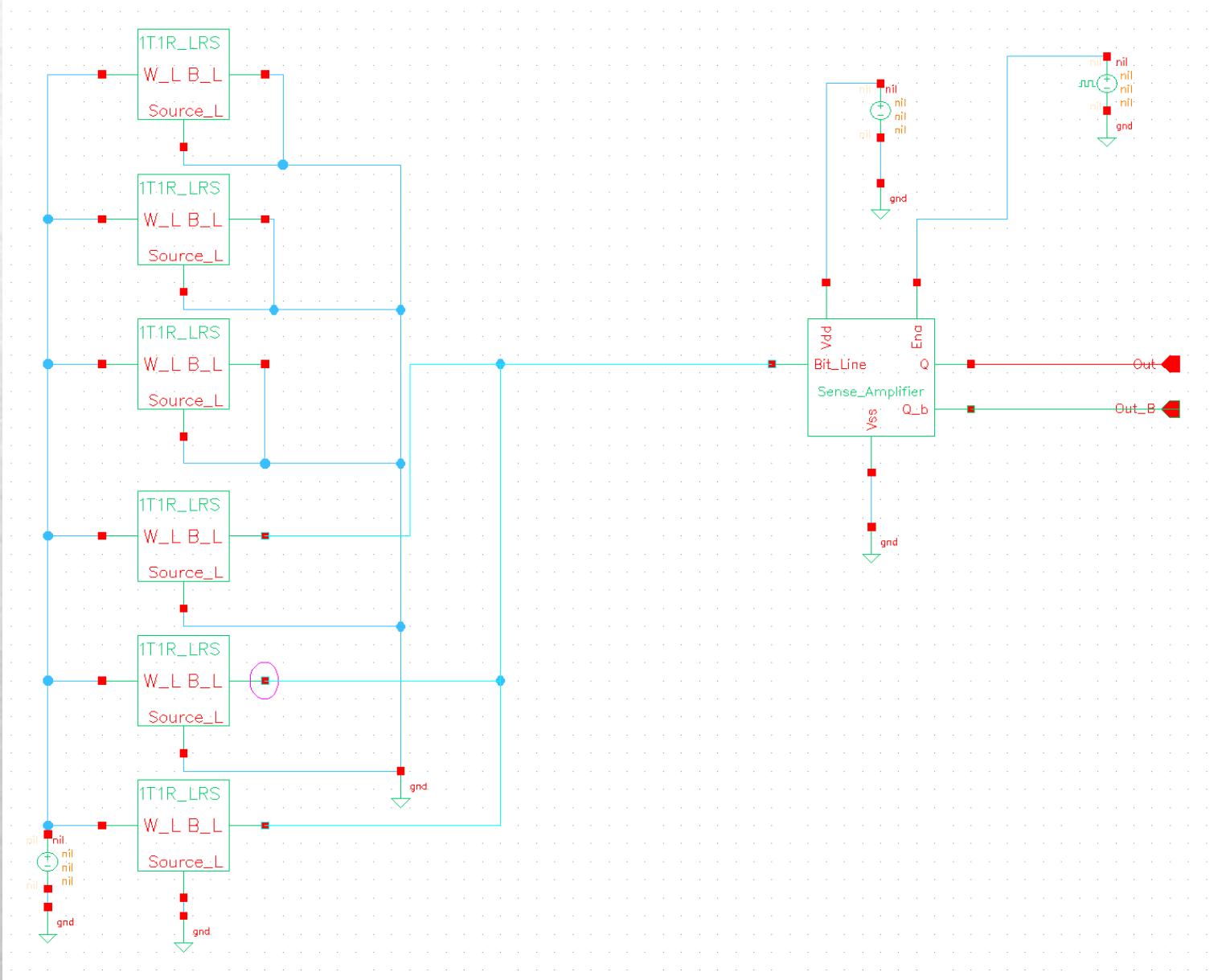


Step-4 : Reading/Making m1(6) =LRS





Step-5 : Reading C_{OUT} =HRS, m1=LRS, C_{IN} =LRS



Transient Response

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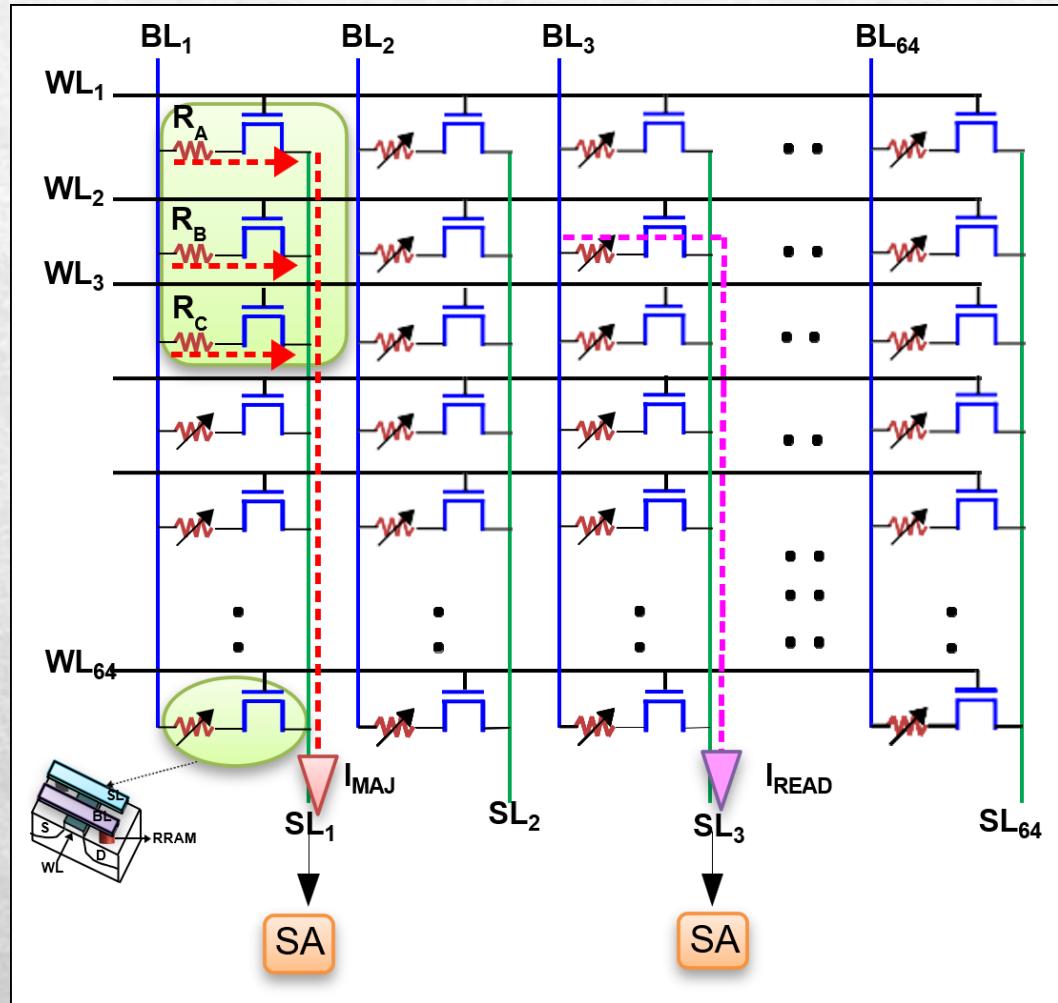
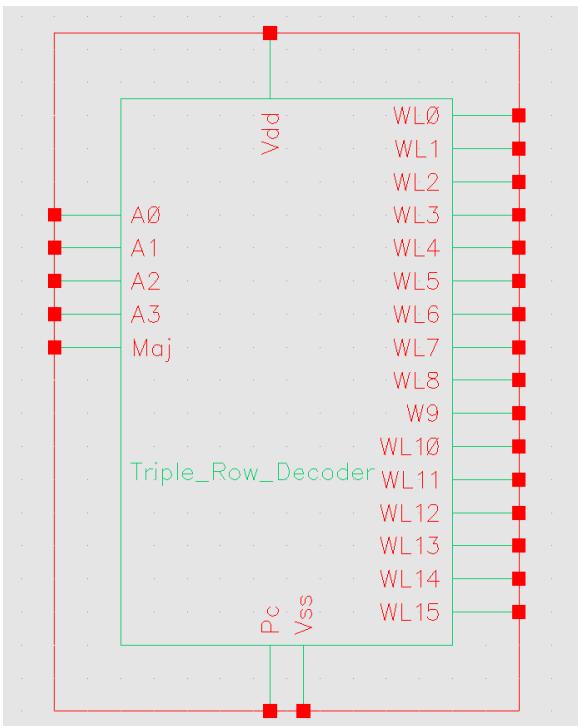
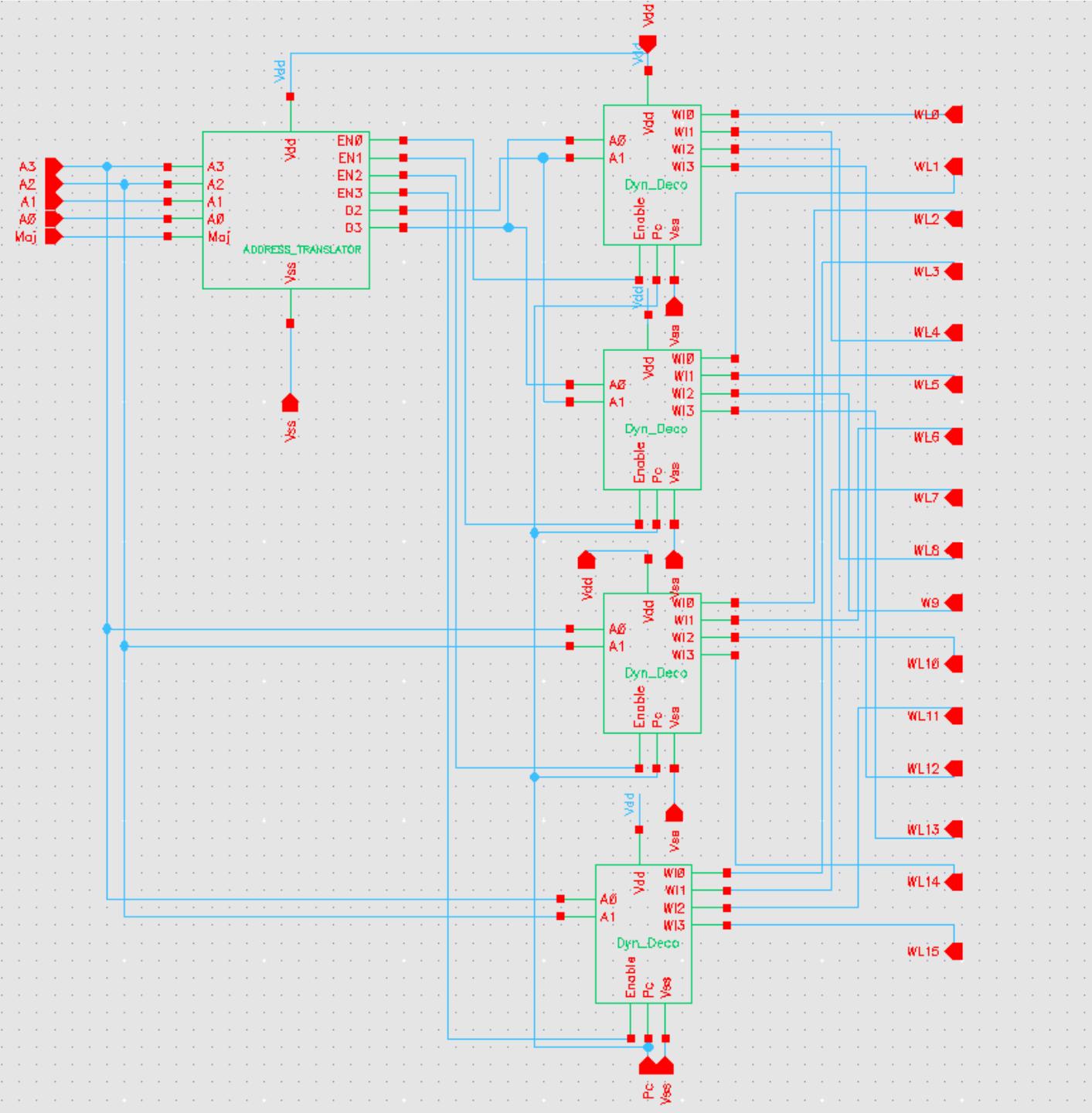


Figure . In a conventional memory, a single row is activated and V_R is applied across the cell to read from it (e.g., reading from cell at 2 depicted in pink). To compute majority, three Word Lines ($WL_{1,2,3}$) are activated simultaneously and $V_R/3$ is applied across cells in column 1 resulting in I_{MAJ} .

Row decoder



- **Purpose:** To select multiple rows of memory cells simultaneously for efficient majority operations.
- **Structure:** Interleaving of four 2:4 dynamic NAND decoders.
- **Operation:**
 - Pre-charge signal (Φ) drives all output lines (WL) to '0'.
 - Input address lines (A) determine which output lines should be activated.
 - NAND gates evaluate the address and activate the corresponding WLs.
- **Single-row vs. Multi-row:** A conventional 1T-1R memory selects one row at a time, while the proposed gate selects three rows simultaneously.



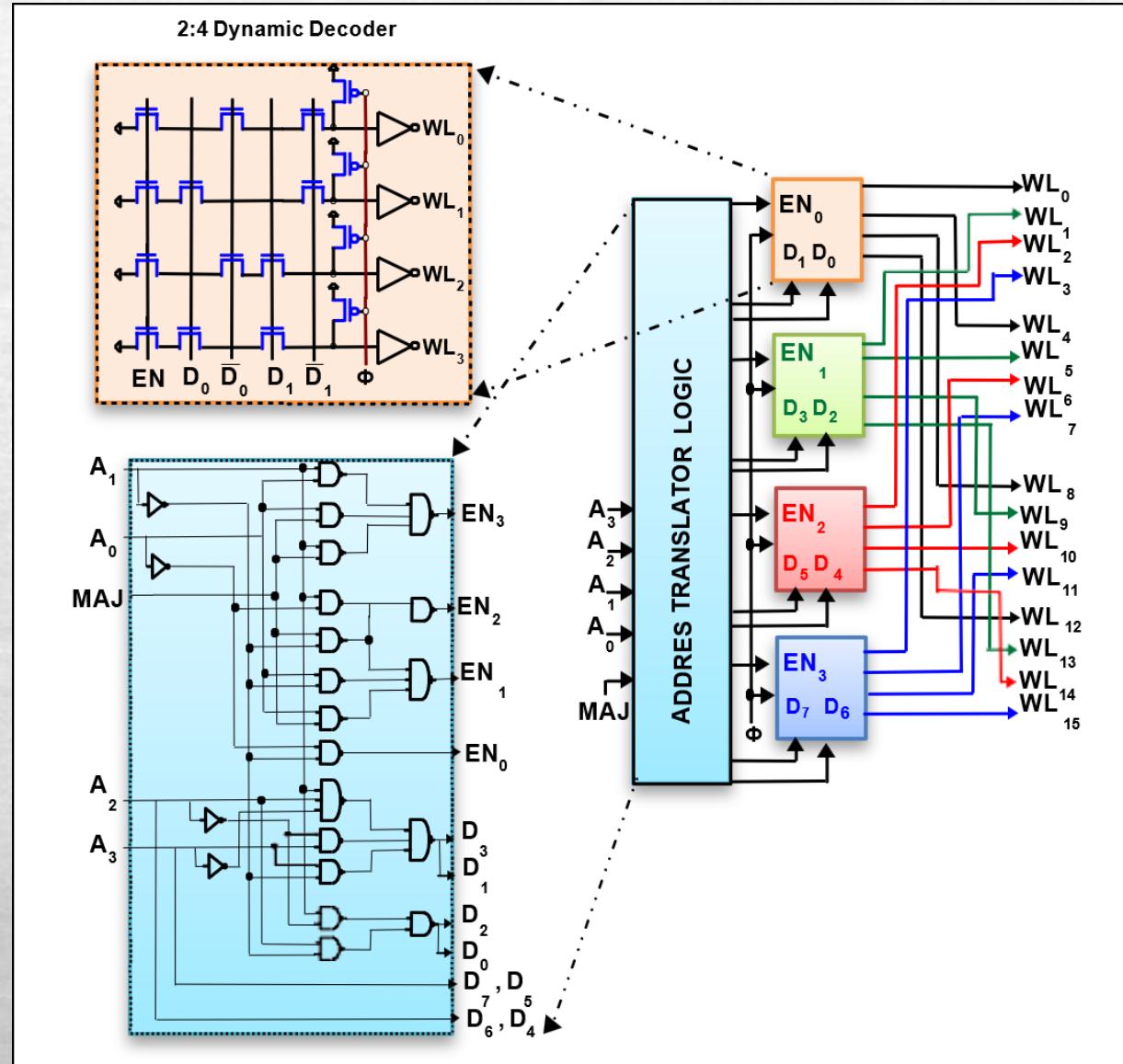
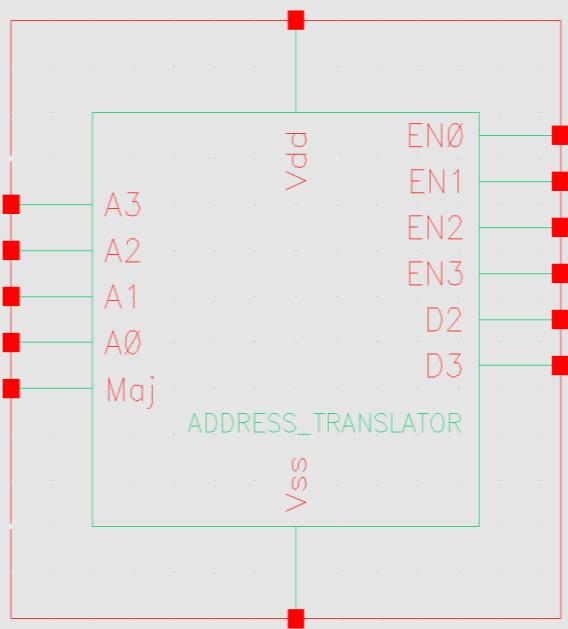
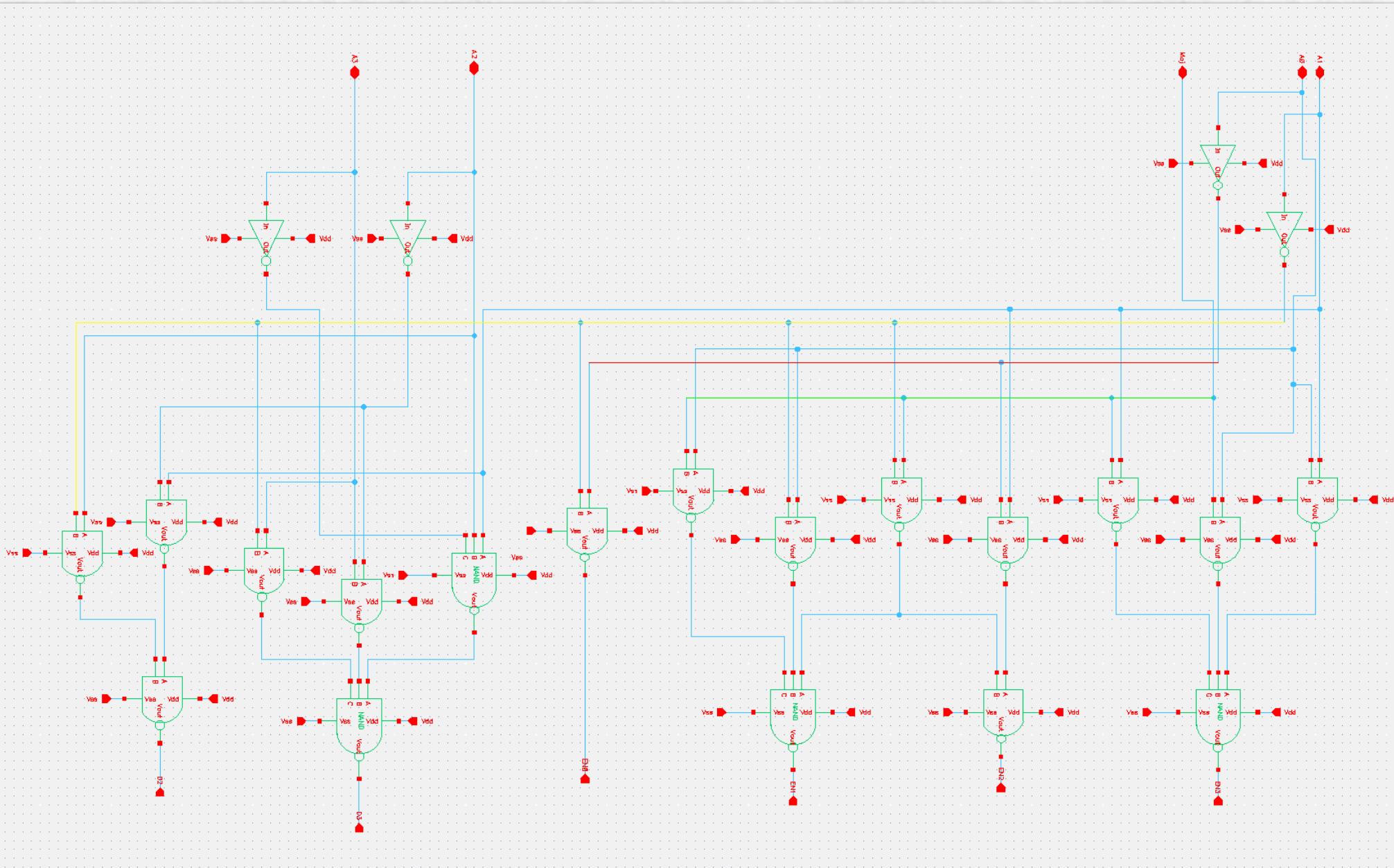


Fig. : Triple-row decoding is achieved by interleaving multiple single-row decoders. When control signal MAJ is logic ‘0’ (READ/WRITE/NOT), WL_i corresponding to row address A₃A₂A₁A₀ is selected. When MAJ is logic ‘1’ (majority), WL_i, WL_{i+1}, WL_{i+2} are selected.

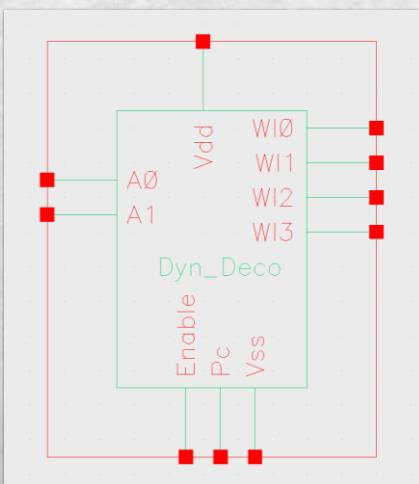
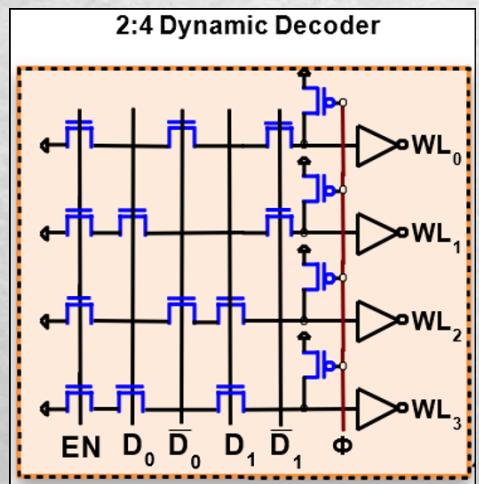
Address Transistor Logic



- **Purpose:** To switch between single-row and multi-row decoding modes.
- **Control Signal:** MAJ (Majority) signal determines the mode.
- **Functionality:**
 - Single-row mode: Enables one decoder and sets the corresponding D values.
 - Multi-row mode: Enables multiple decoders and sets the appropriate D values.
- **Address Translation:** Converts the input address ($A_3A_2A_1A_0$) into control signals ($D_7D_6D_5D_4D_3D_2D_1D_0$ and $EN_3EN_2EN_1EN_0$).



2:4 Dynamic decoders



Dynamic NAND decoders are called "dynamic" because their operation relies on a pre-charge signal (Φ) to determine the output state.

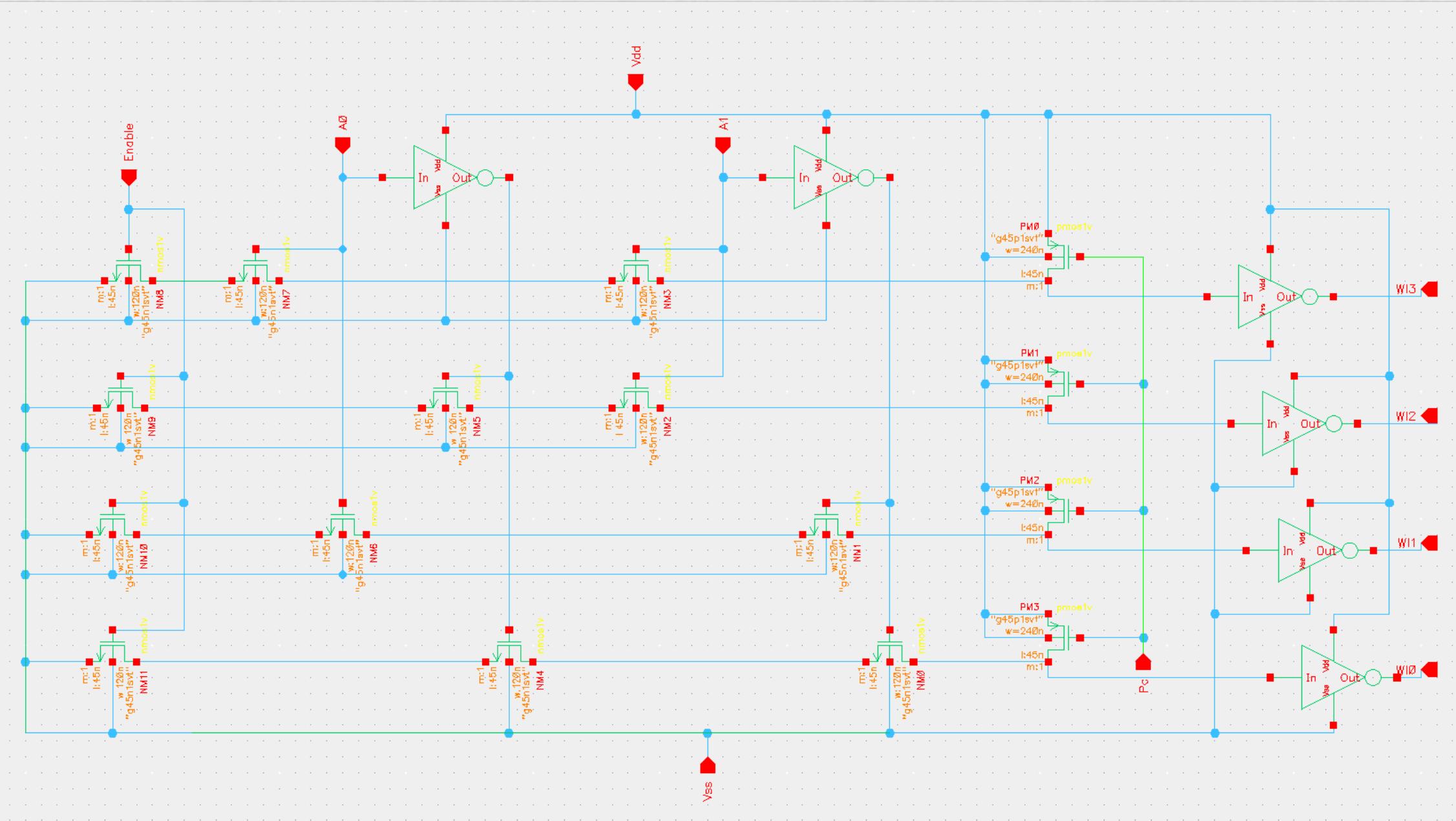
This pre-charge signal is periodically changed, allowing for faster operation and reduced power consumption compared to static decoders.

In contrast, static decoders maintain a constant output state based solely on the input address, without requiring a pre-charge signal. This leads to higher power consumption and potentially slower operation.

Dynamic NAND decoders are a type of digital circuit used to select specific output signals based on input address codes. They are commonly employed in memory systems to address individual memory cells.

Key Components and Operation:

- 1.Pre-charge Signal (Φ):** This signal is used to pre-charge all output lines (WL) to a specific voltage level (typically '0').
- 2.Input Address Lines (A):** These lines carry the address code that determines which output line should be activated.
- 3.NAND Gates:** The decoder consists of multiple NAND gates, each connected to a specific output line (WL).
- 4.Output Lines (WL):** These lines correspond to the selected memory cells or other circuit elements.



GENERAL STRUCTURE OF IN-MEMORY COMPUTING SYSTEM

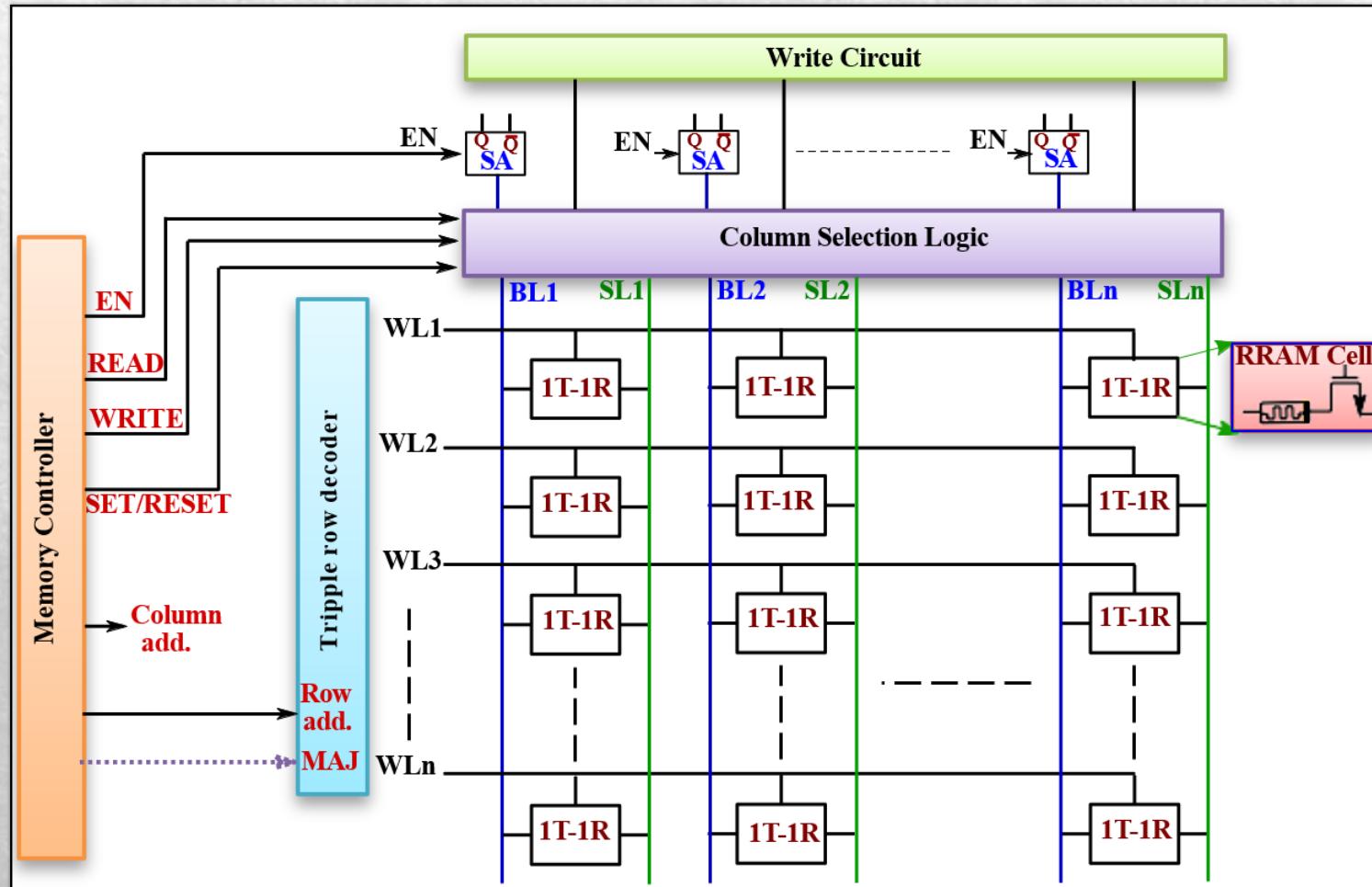
□ Memory Organization

- The memory array is arranged into **multiple segments**, each containing **8 columns**.
- Each segment has dedicated **Sense Amplifiers (SAs)** and **multiplexers (Mux)** for controlling and selecting columns within that segment.
- The rows are accessed by **Word Lines (WL1, WL2, WL3)**, while columns are accessed via **Bit Lines (BL1, BL2, BL3, etc.)**.
- The diagram shows various control signals that govern the operation of the memory cell, such as **WRITE, READ, EN, and SET/RESET**.
- The memory is organized into rows and columns, and a triple row decoder is used to select a specific row within the memory array.
- The diagram shows various control signals that govern the operation of the memory cell, such as **WRITE, READ, EN, and SET/RESET**.

- Each segment has dedicated Sense Amplifiers (SAs) and multiplexers (Mux) for controlling and selecting columns within that segment.
- The **Transmission Gates (TG)** are key components controlling data flow for both read and write operations.
- TGs are responsible for isolating or connecting the **Bit Line (BL)** and **Source Line (SL)**.
- These gates are toggled by control signals like READ and WRITE.
- There are **two sets of TGs**, one for each operation, ensuring that only the required lines are active during memory access.
- The memory cells operate with **SET and RESET operations**, controlled by a **SET/RESET switch**:
- **SET Operation (HRS → LRS):**
 - The memory cell is changed from a **High Resistance State (HRS)** to a **Low Resistance State (LRS)**.
 - Triggered by setting the **SET/RESET signal to '1'**.
- **RESET Operation (LRS → HRS):**
 - The memory cell is changed back to **High Resistance State (HRS)** from **Low Resistance State (LRS)**.
 - Triggered by setting the **SET/RESET signal to '0'**.

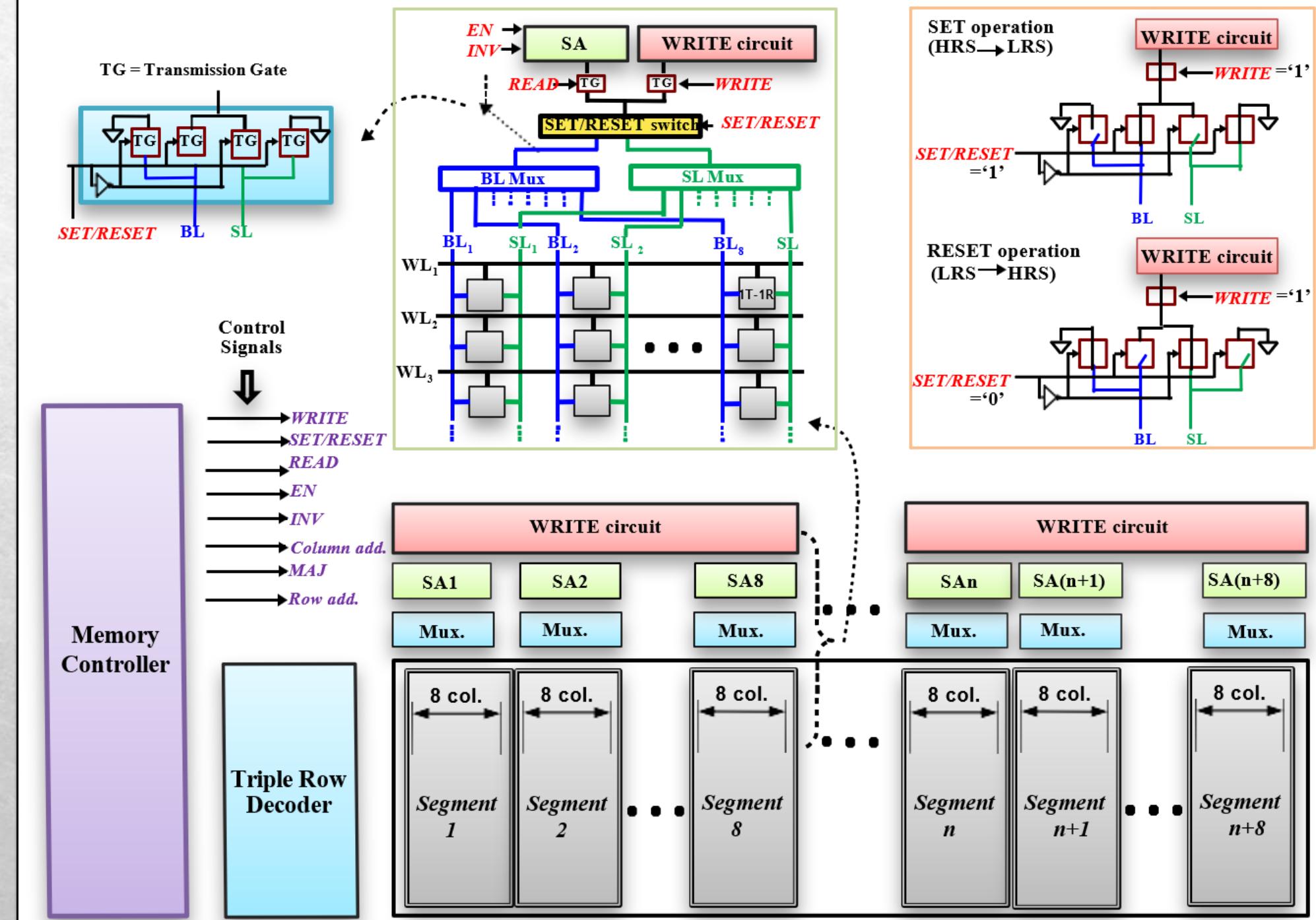
Fig. : Architecture of the in-memory computing system.

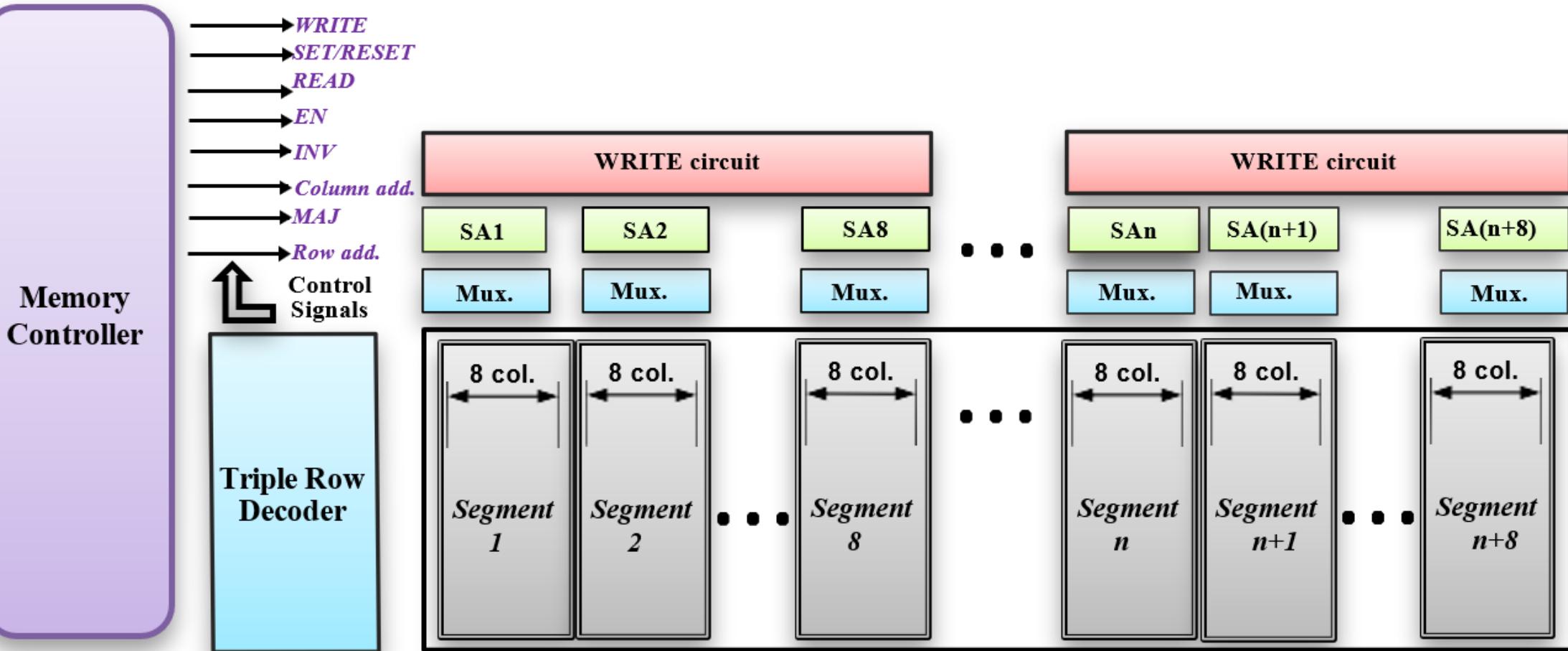
- Each column has a dedicated SA for READ operation.
- Eight columns of the array share a WRITE circuit.
- A triple-row decoder is used which uses MAJ as control signal to switch between majority operation (three rows selected) and normal READ/WRITE operation (single row is selected).



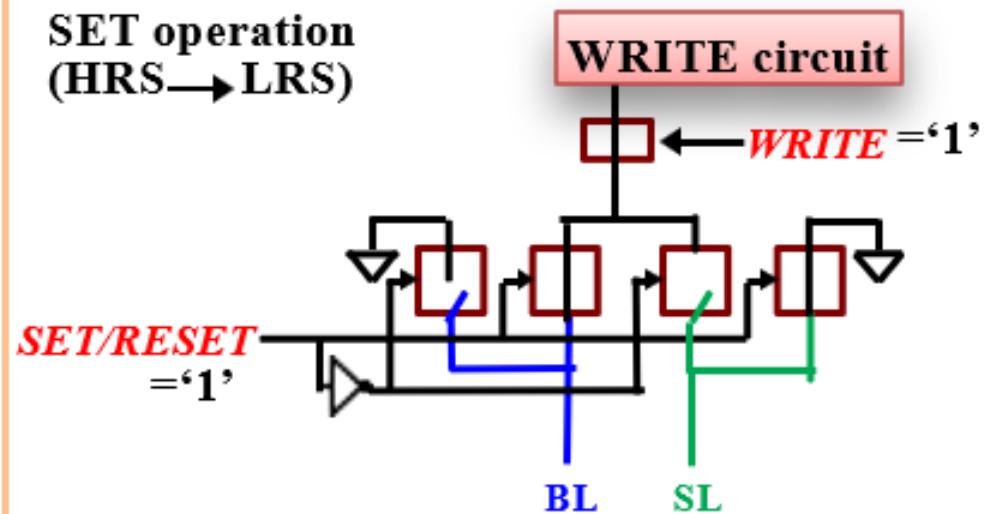
Detailed Architecture of the in-memory computing system.

The memory array augmented with computing capability. Since the area occupied by the SA corresponds to 8 columns, the array is partitioned into segments (8 columns form a segment) and each segment has a dedicated SA. 8 segments share a WRITE circuit.

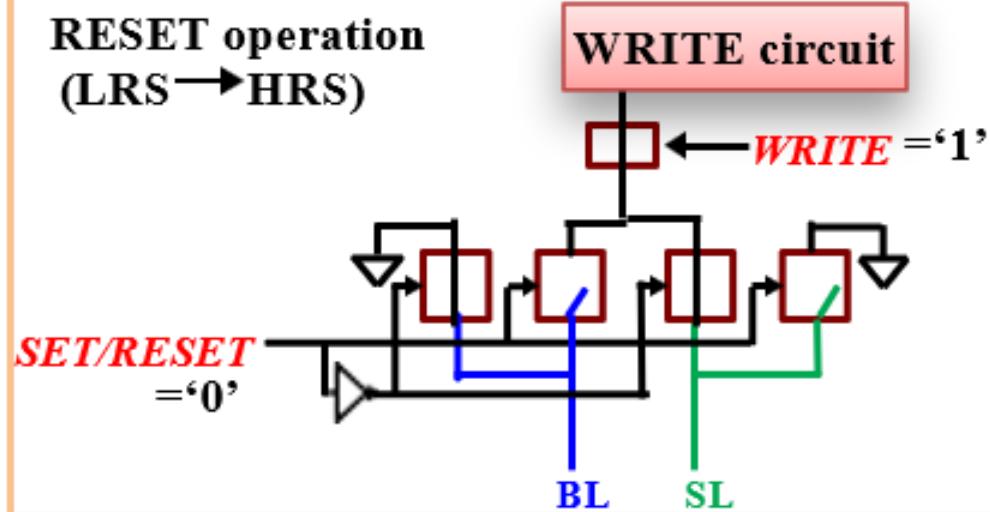


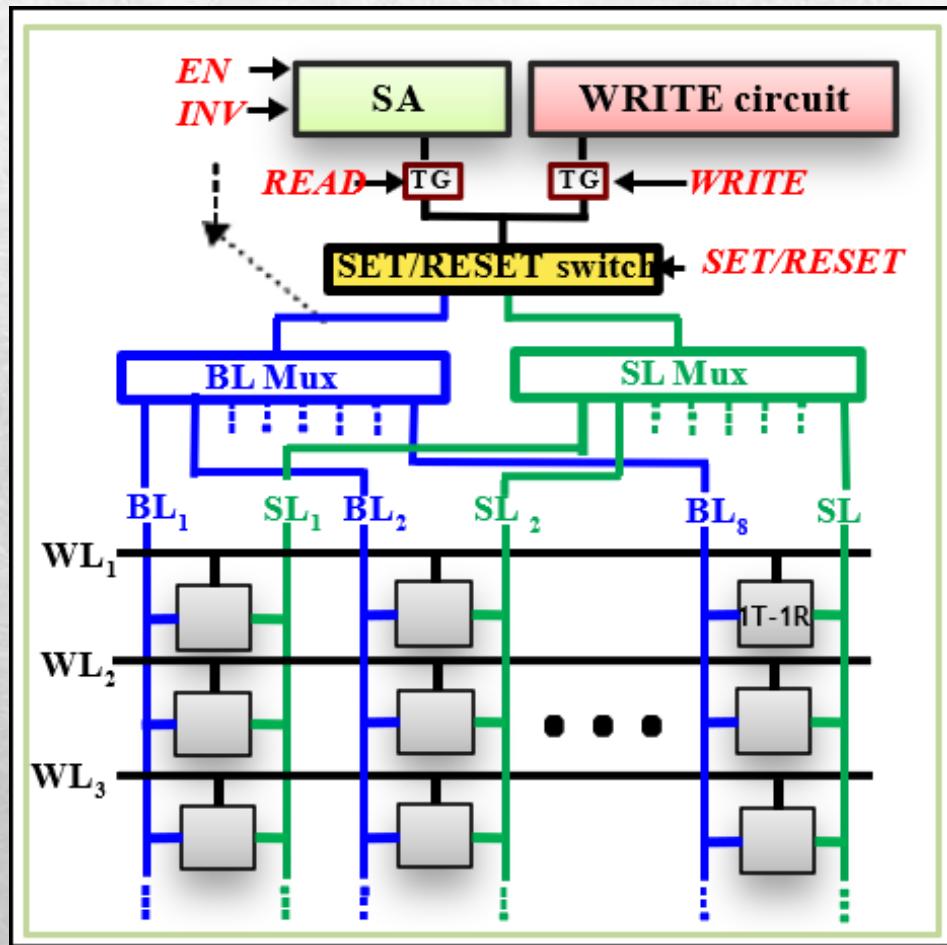


SET operation
 $(HRS \rightarrow LRS)$

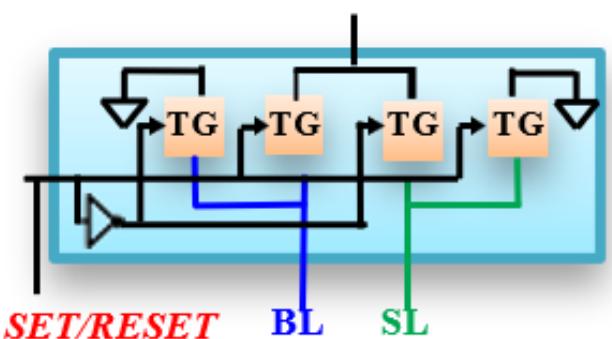


RESET operation
 $(LRS \rightarrow HRS)$





TG = Transmission Gate



Write circuit



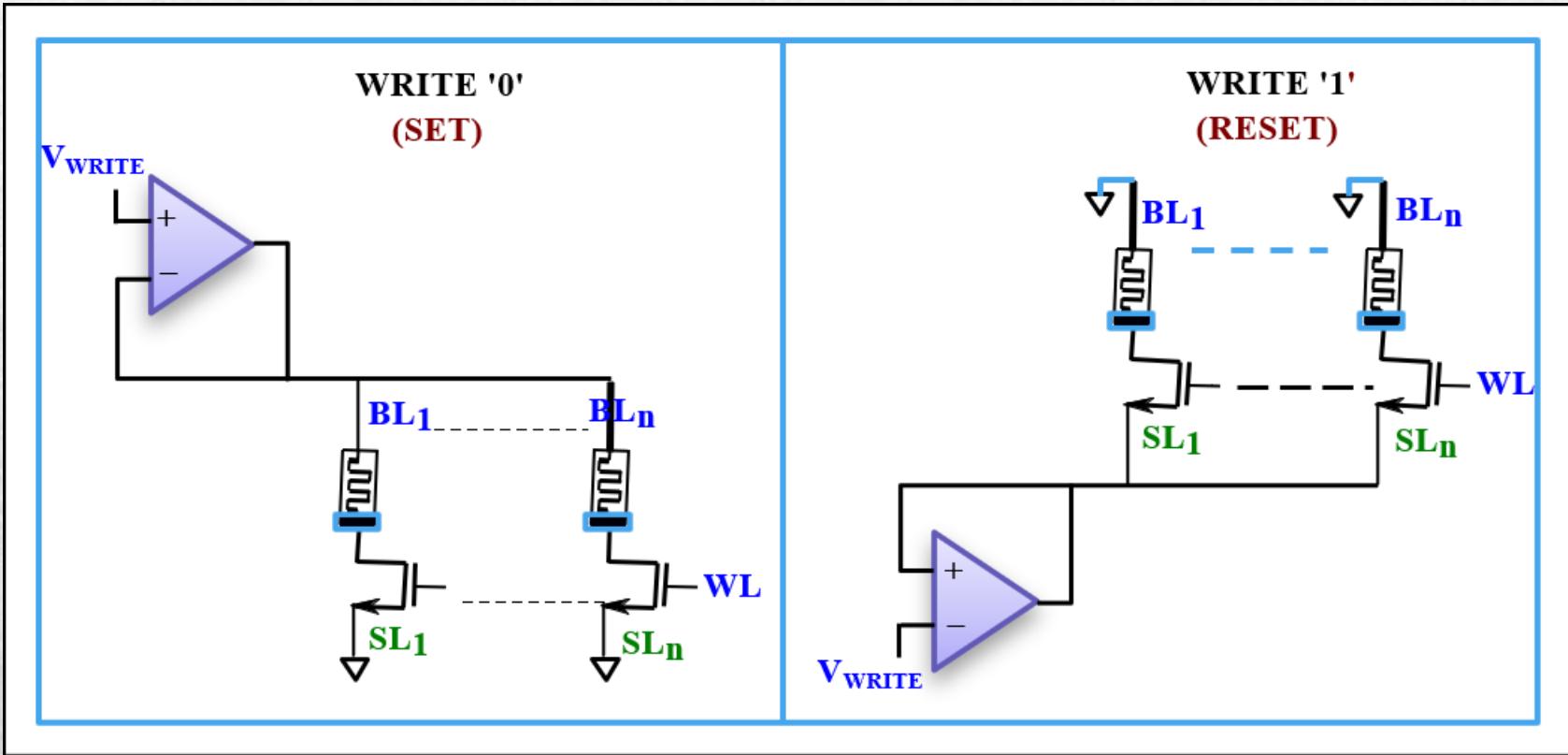
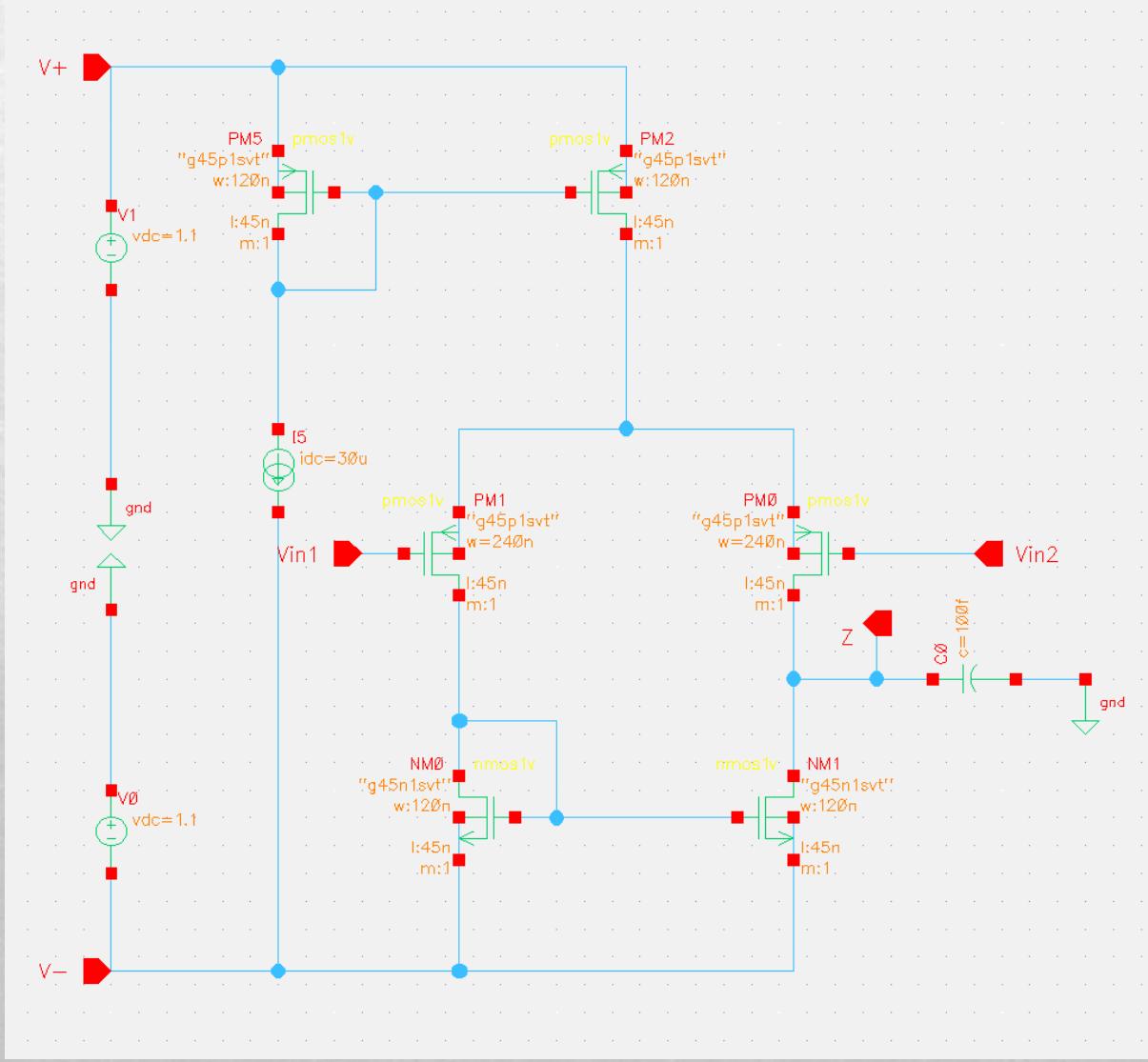
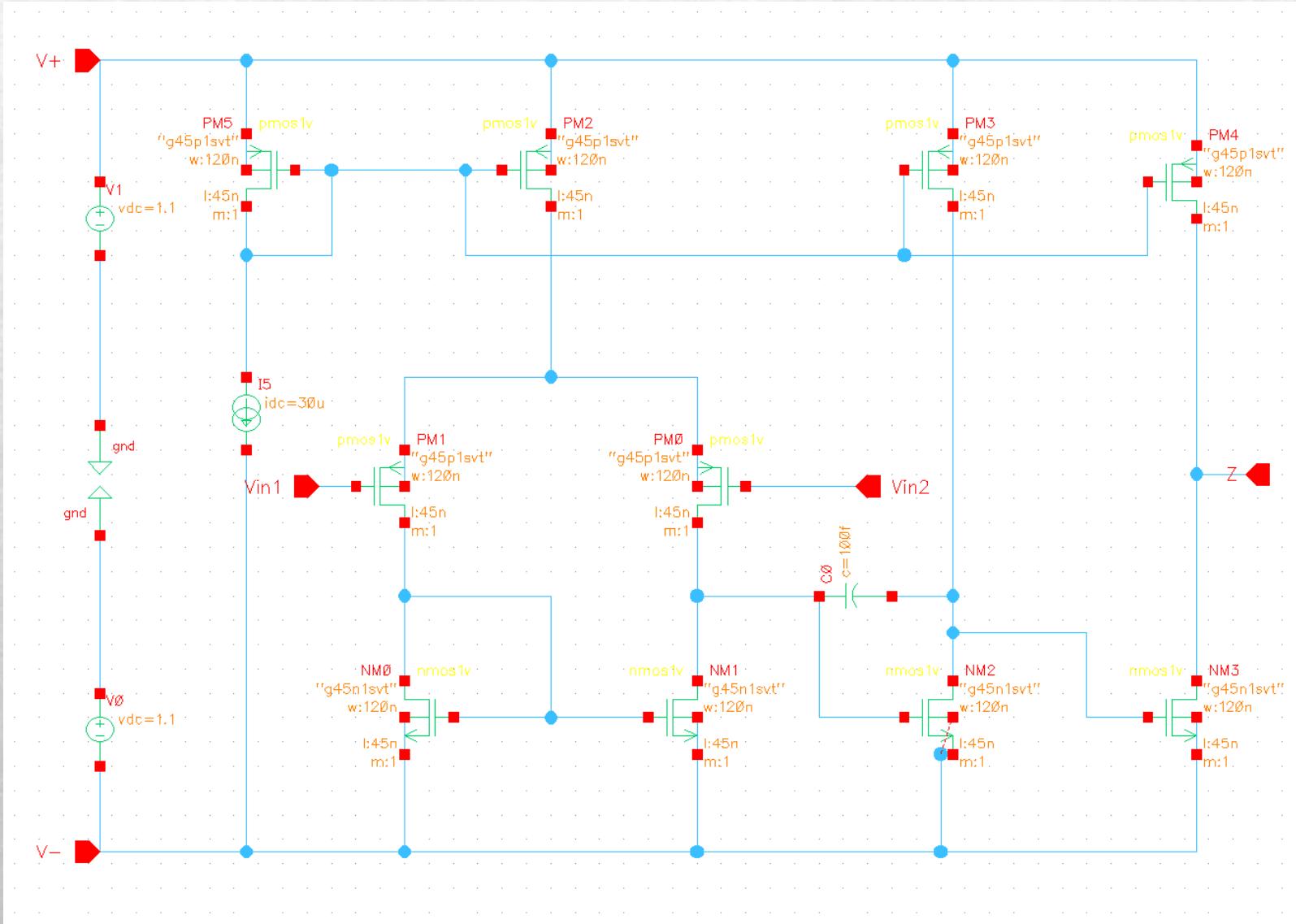


Fig. 6: The operational amplifier regulates the voltage while driving enough current to switch the cell. The op-amp is connected to BL/SL of the ReRAM cells and SL/BL is grounded for WRITE '0'/'1' operation.

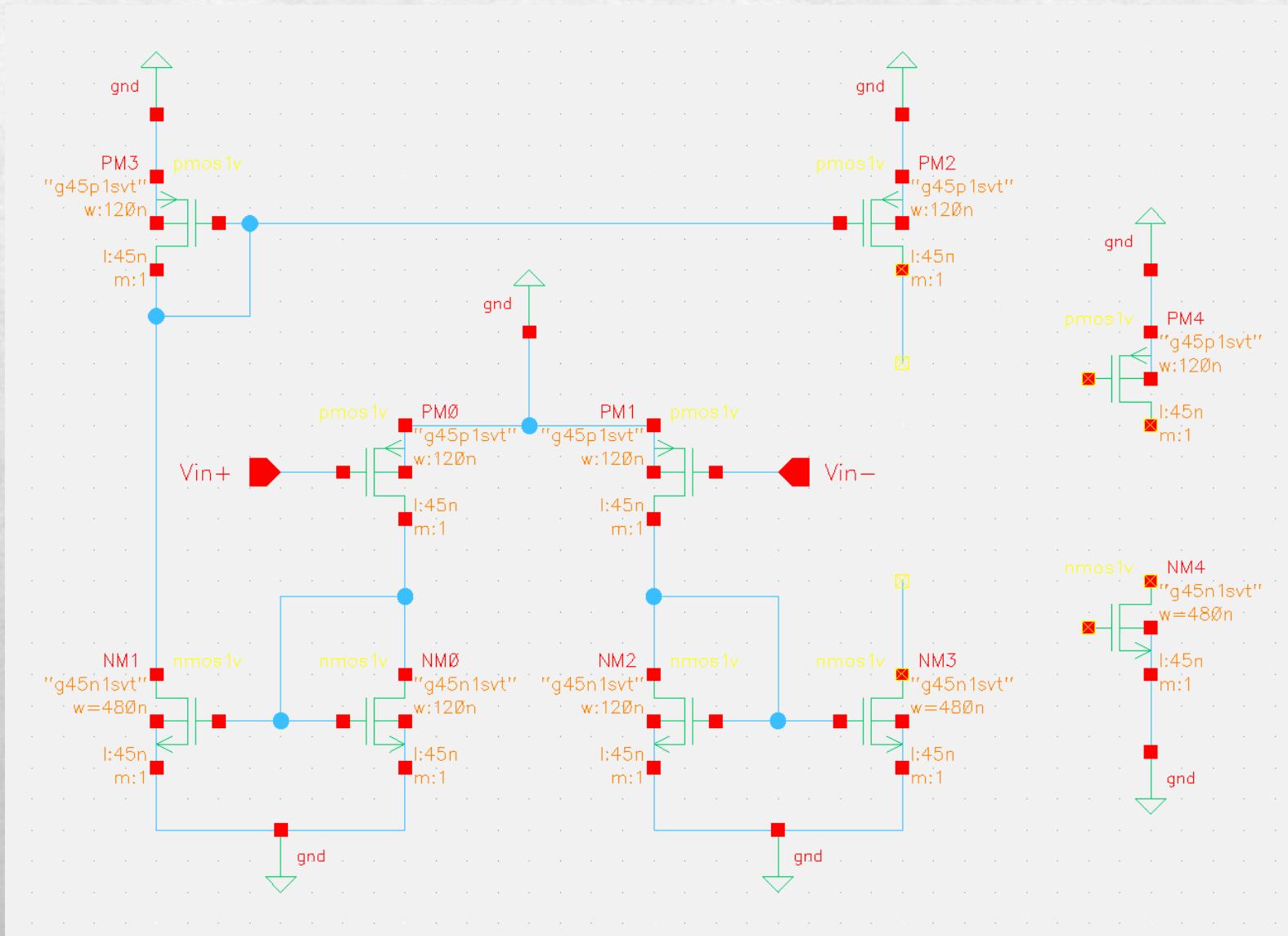
Op.Amp. Single Stage



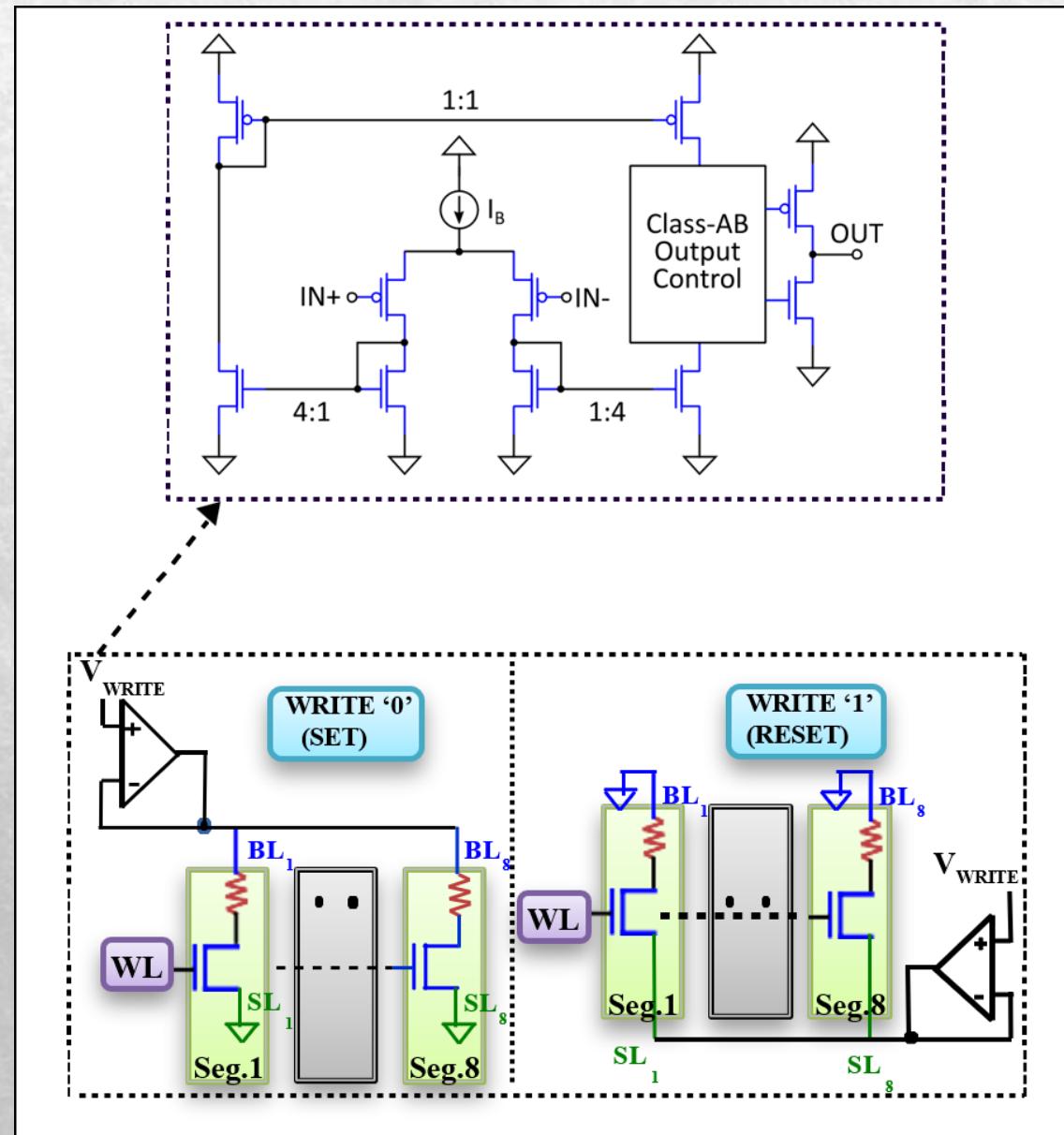
Op.Amp. Double Stage

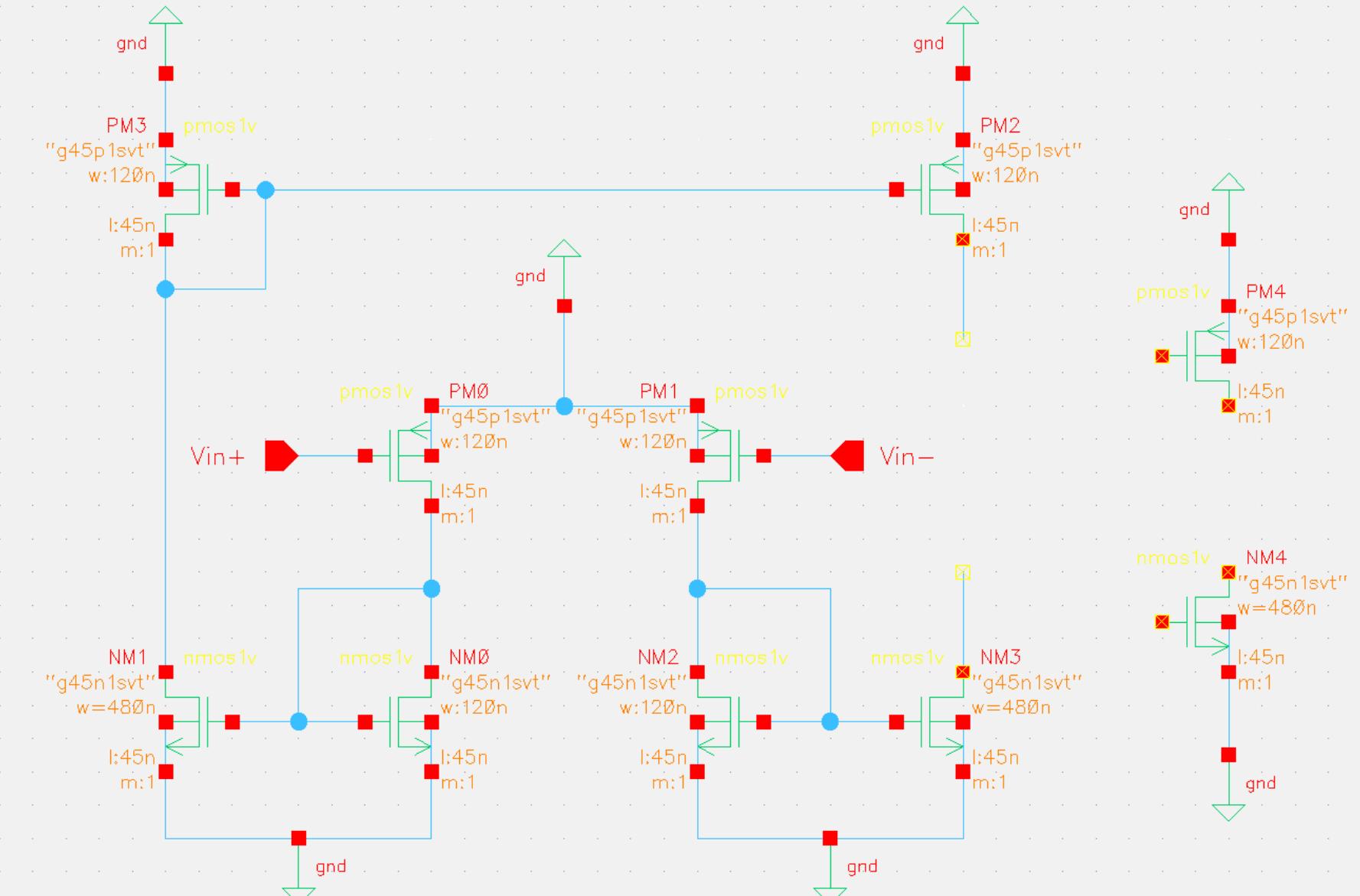


Op.Amp. Class-AM Amp.



Write circuit: Op-amp regulates the voltage while driving enough current to write into the cell.

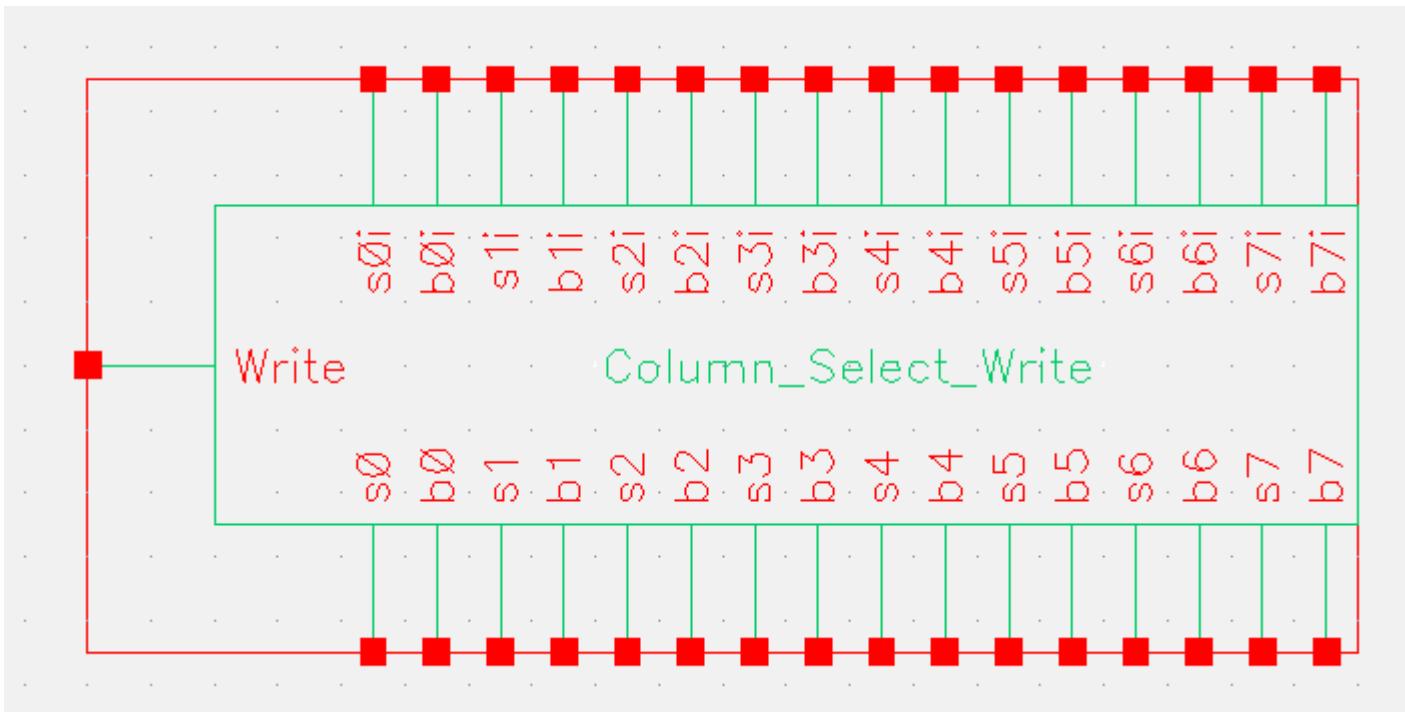


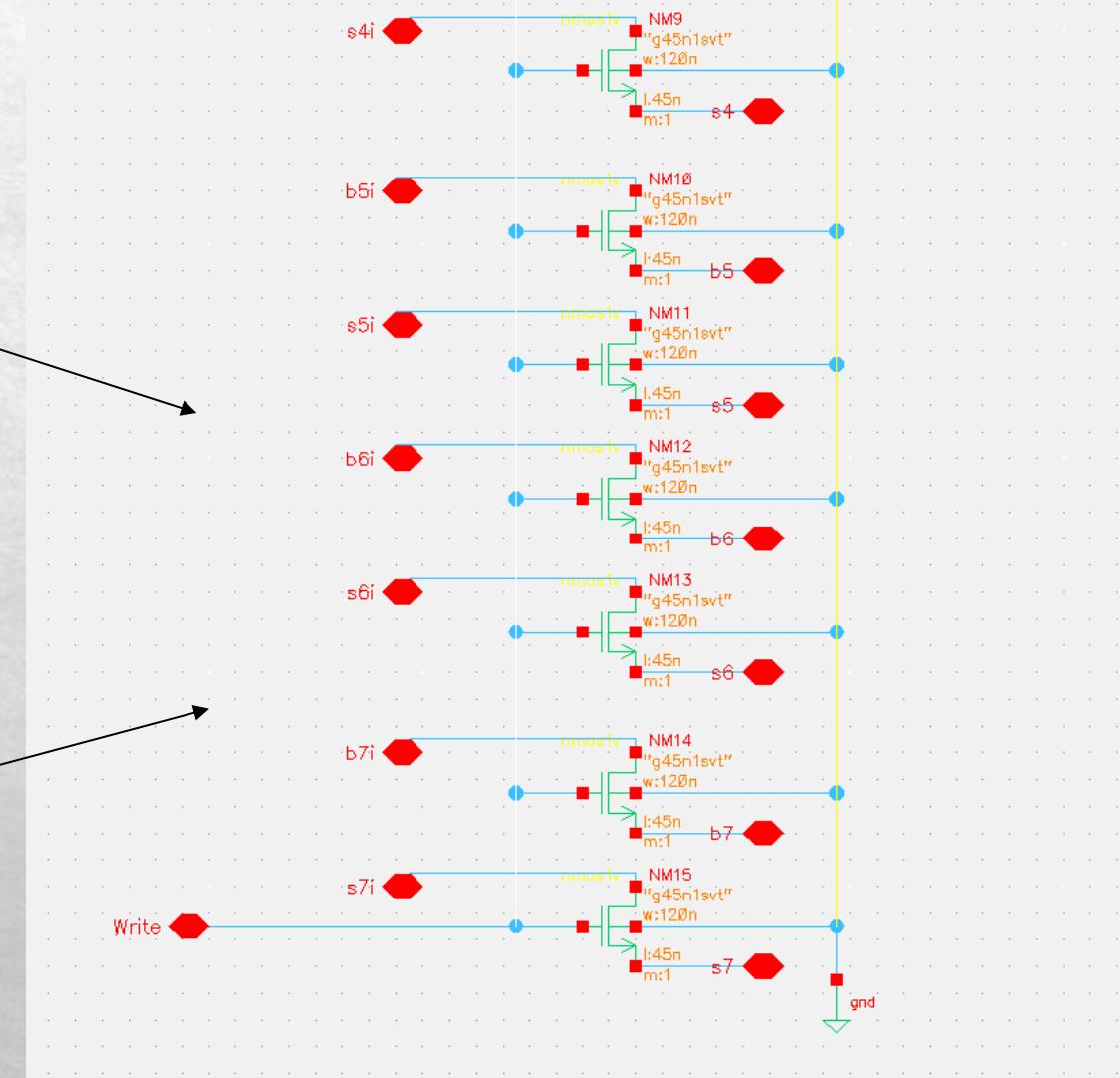
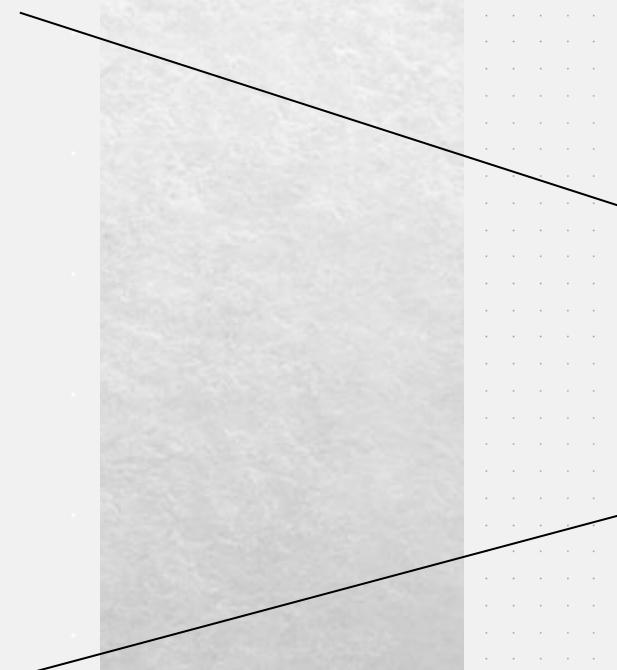
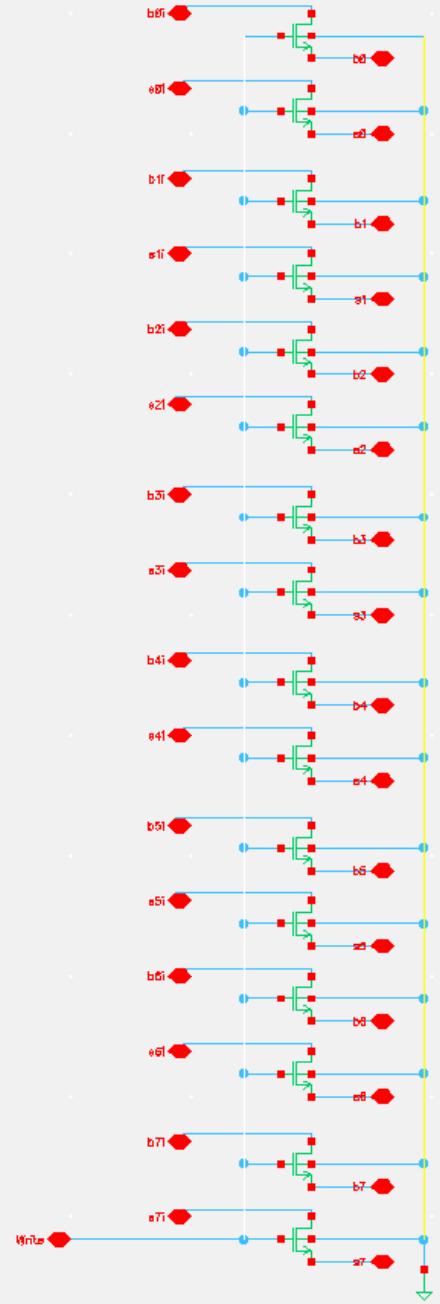


Class-AB OUTPUT Control

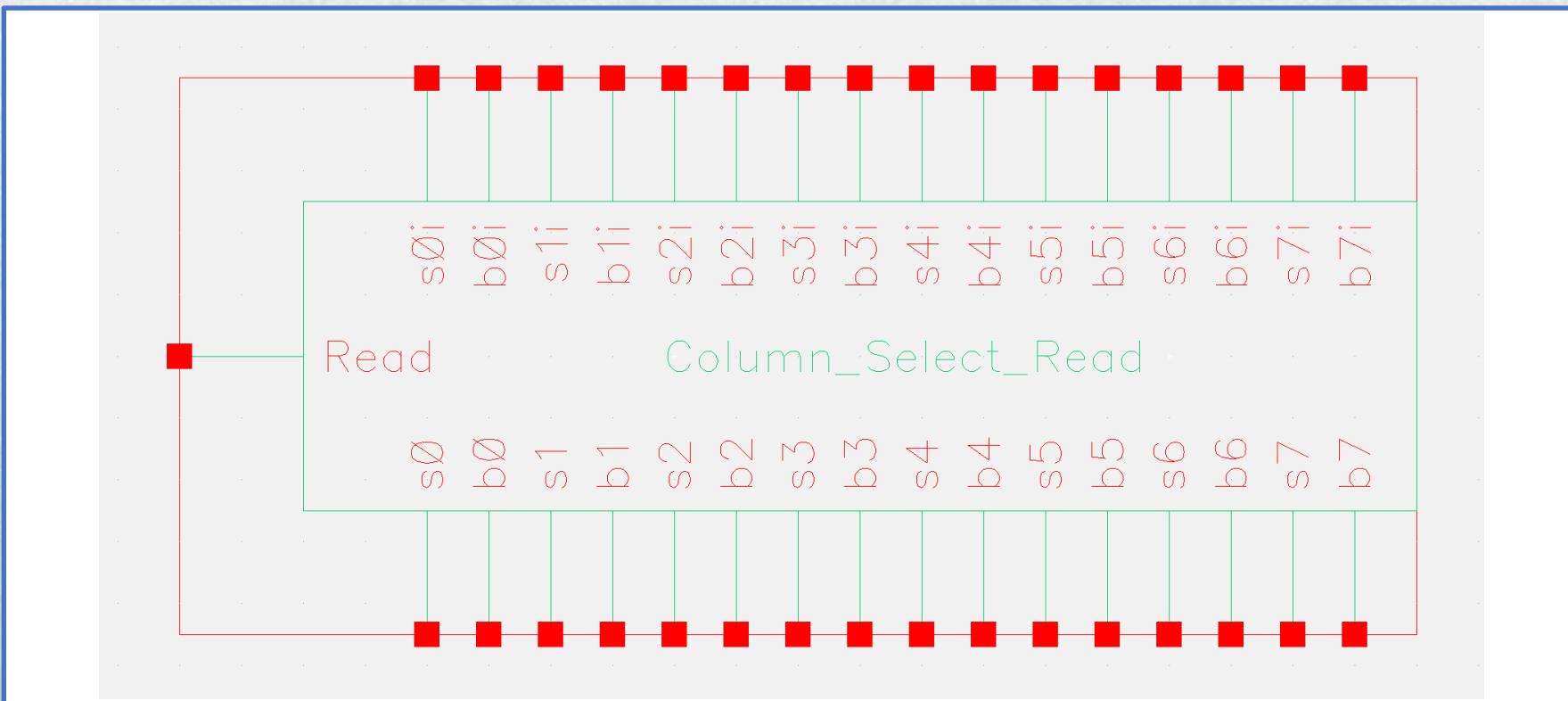


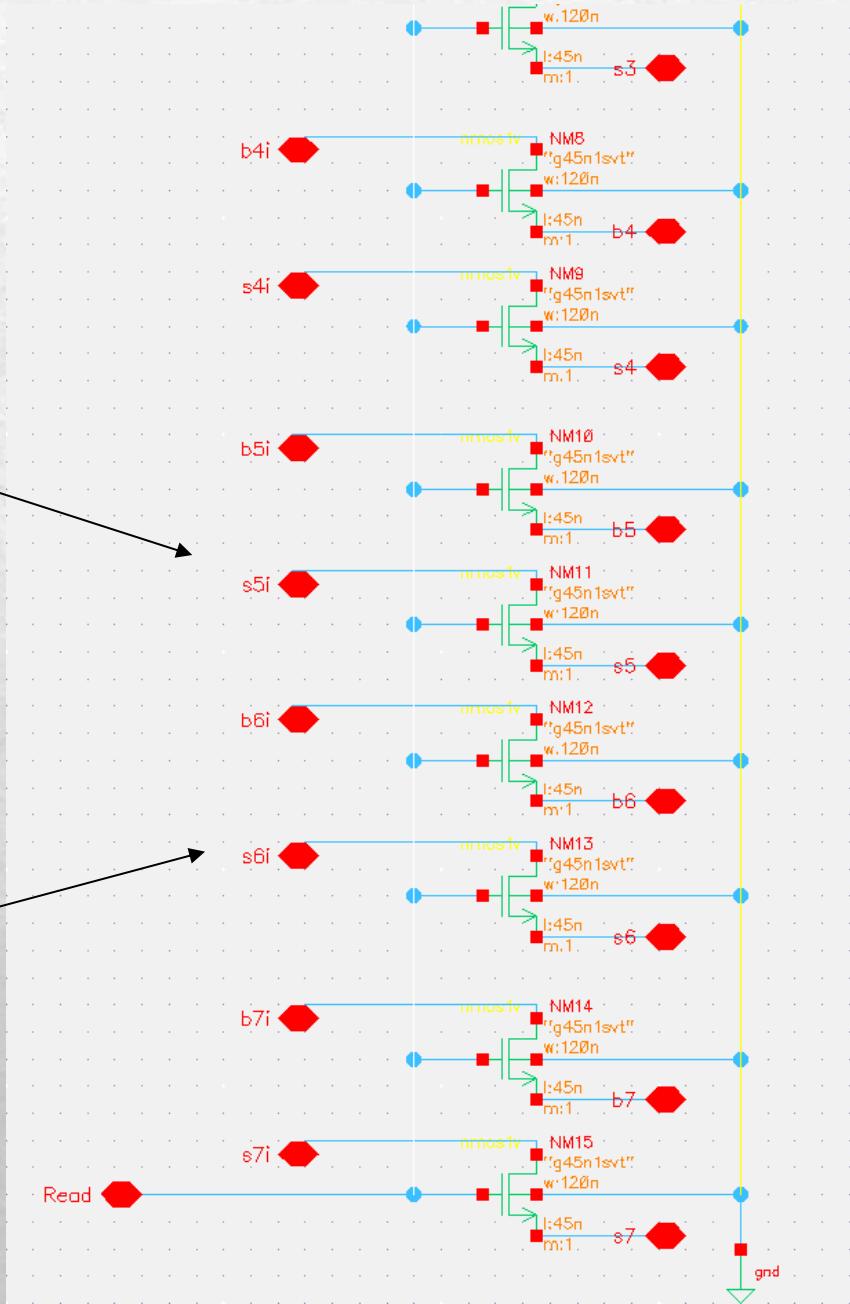
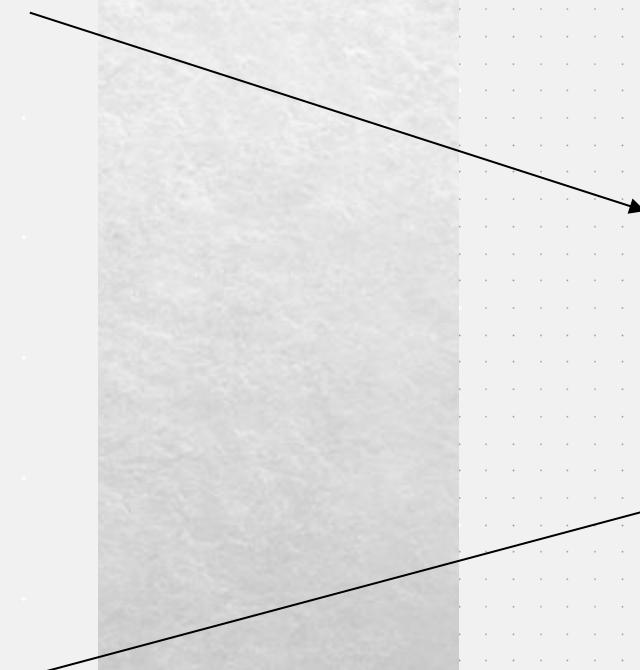
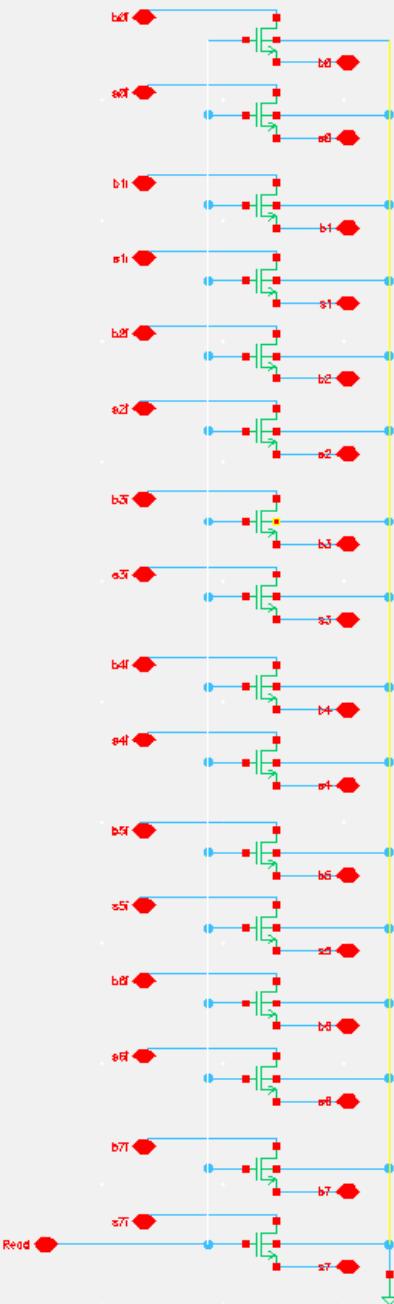
Column selection logic(Write)



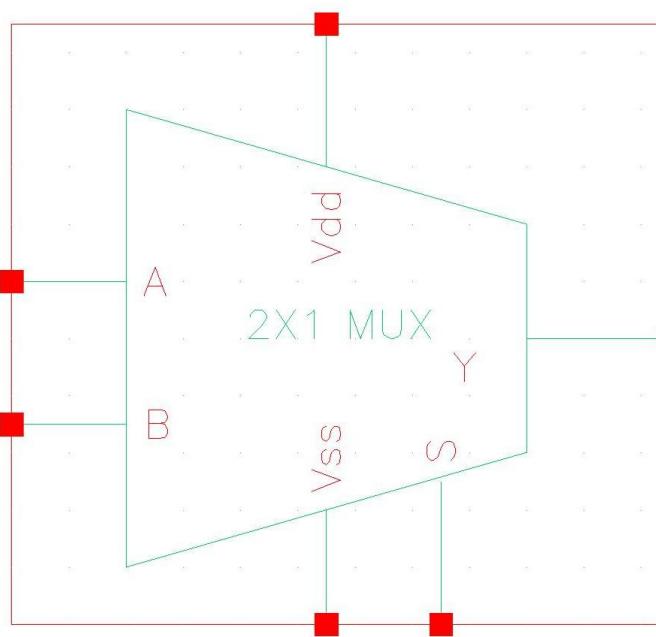


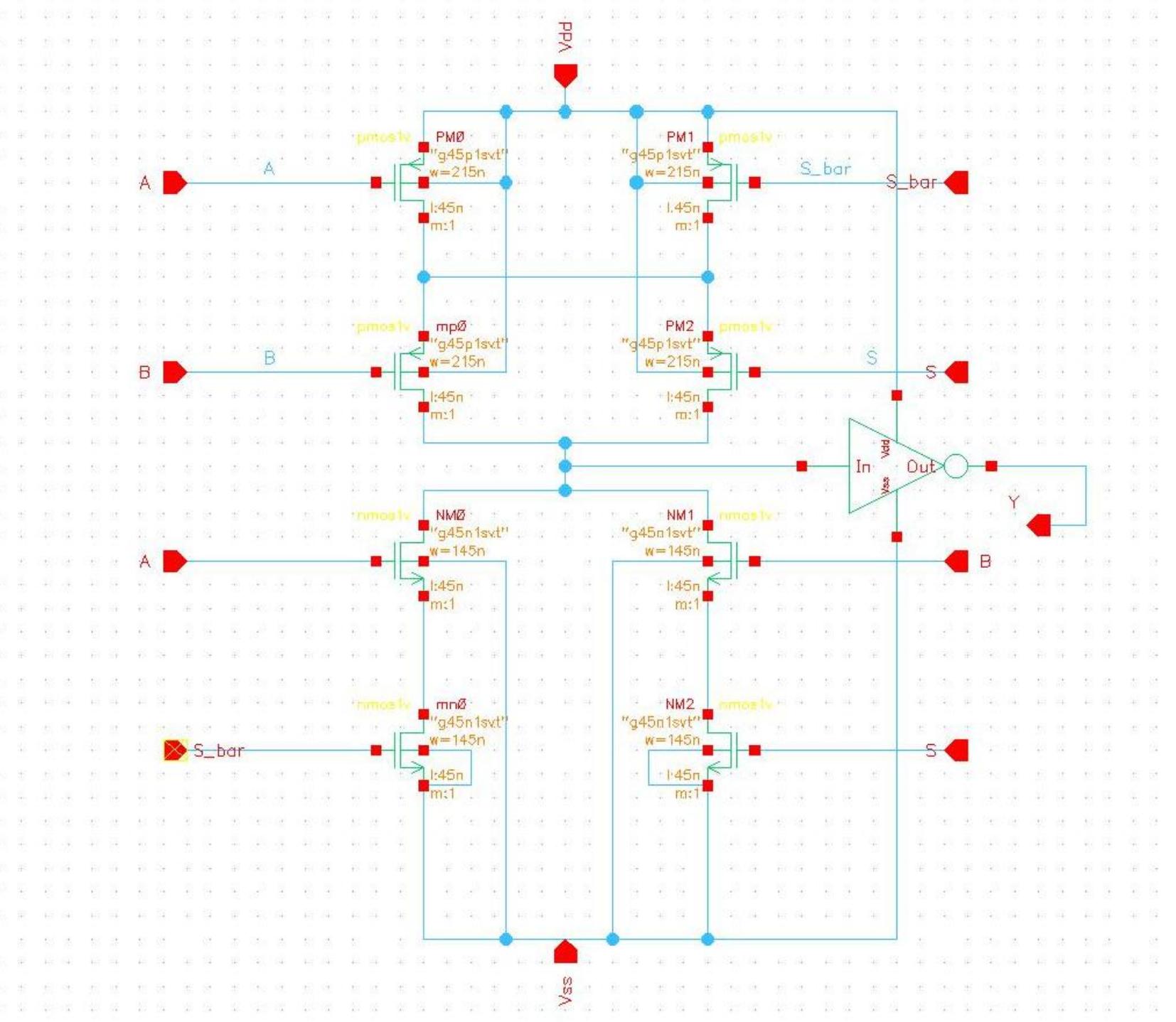
Column selection logic(Read)



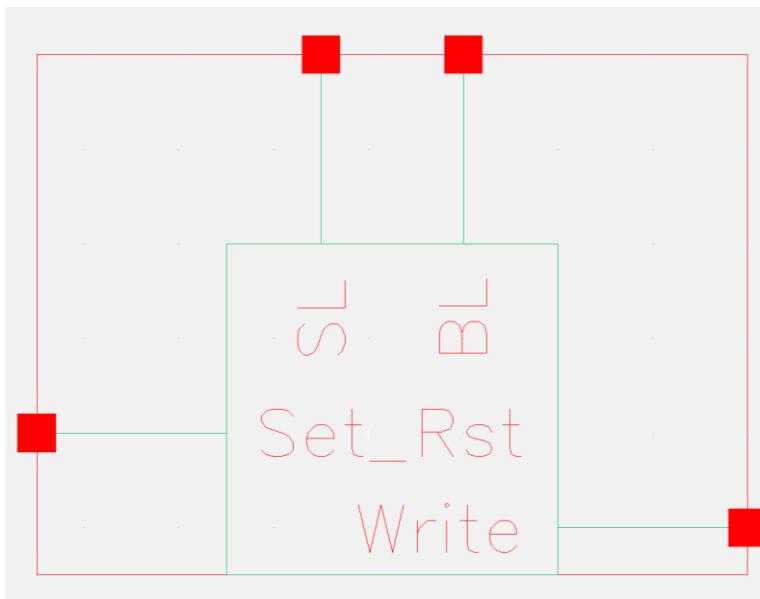


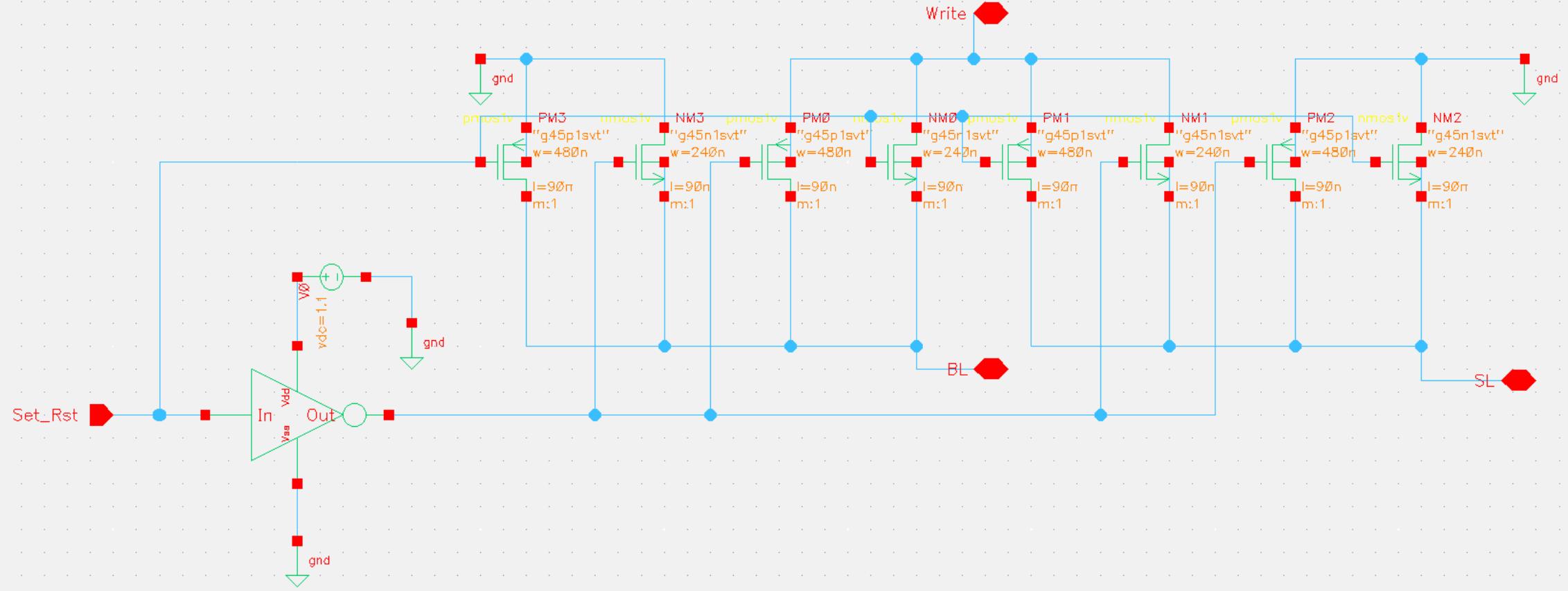
Mux



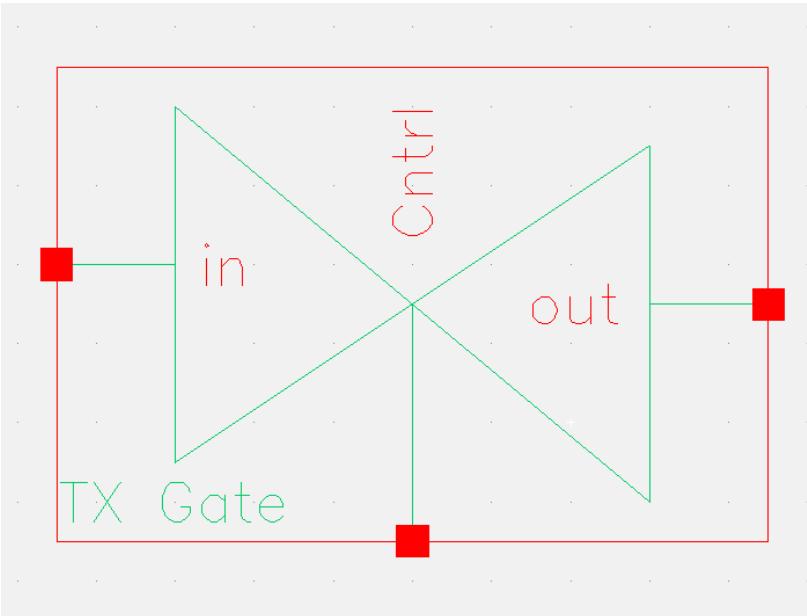


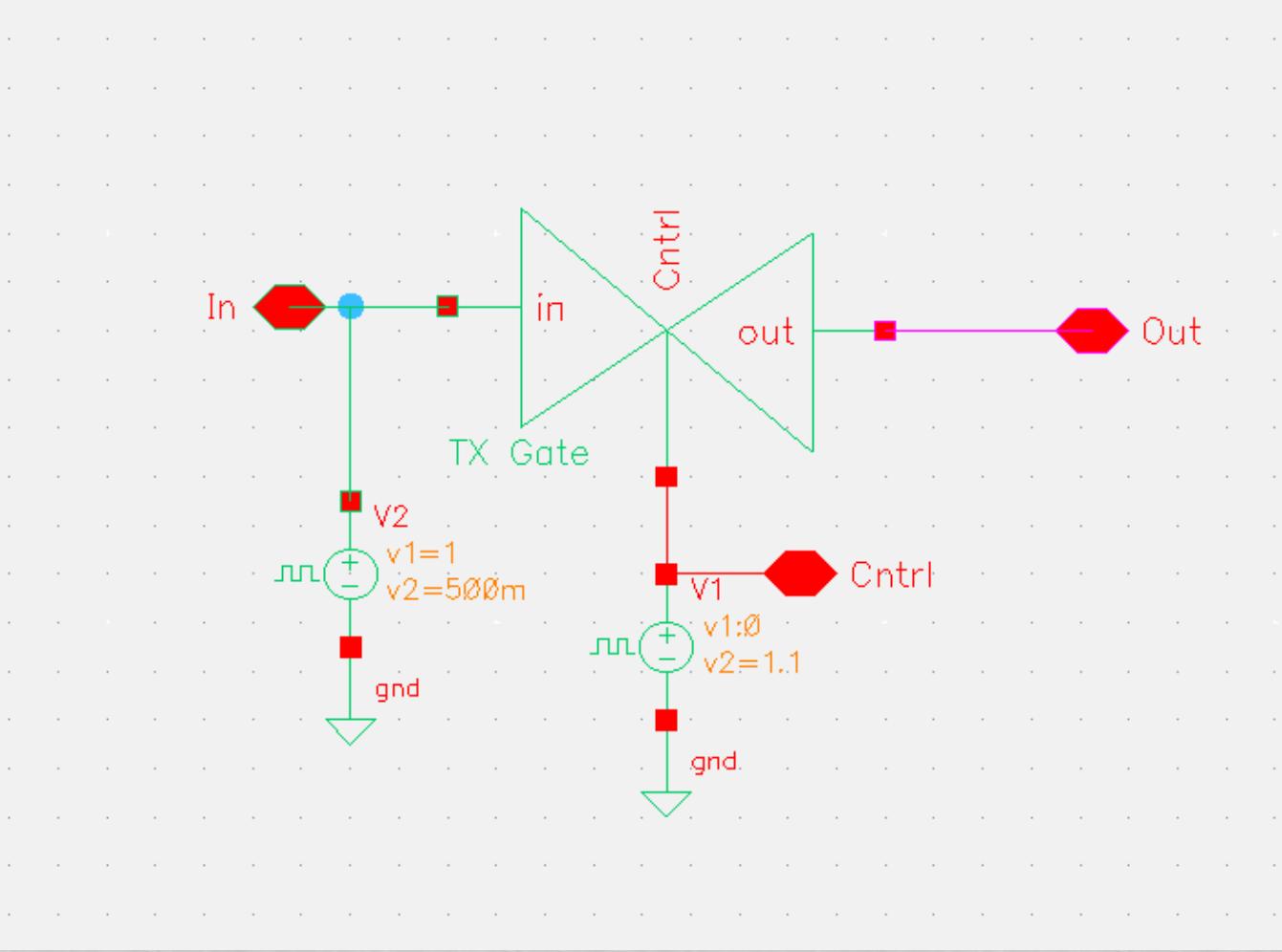
Set/reset switch





Transmission Gate





Transient Response

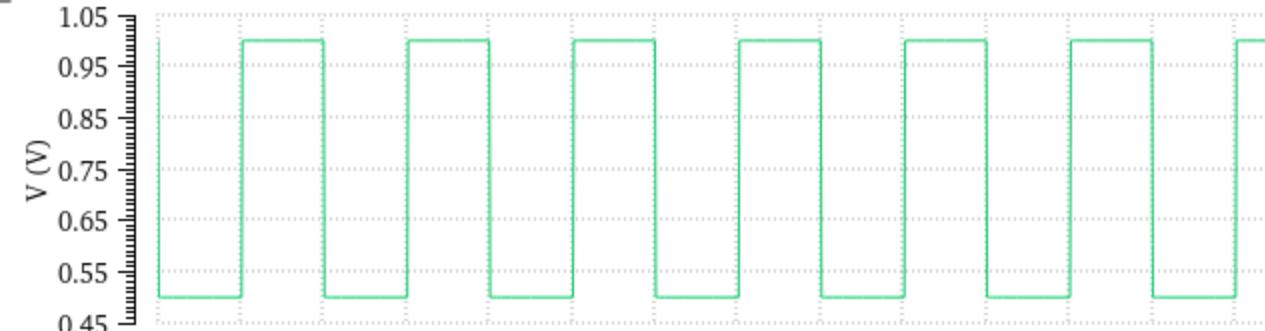
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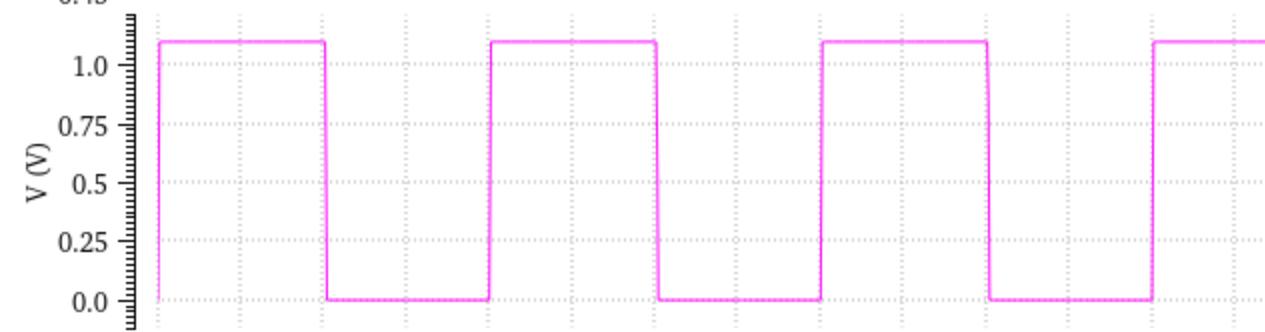
1



/In



/Cntrl



/Out



Memory controller



This table outlines the control signals required for different memory and logic operations, including READ, NOT, Majority, SET, and RESET operations. The columns represent the binary control signals associated with each operation.

Operation	READ	WRITE	SET/RESET EN	INV	MAJ
READ	1	0	1	1	0
NOT	1	0	1	1	0
Majority	1	0	1	0	1
SET (WRITE '0')	0	1	1	0	0
RESET (WRITE '1')	0	1	0	0	0

Conclusions



Thank You