

Contents

- What is clock Jitter?
- Max. timing analysis (Setup check) with Clock Jitter
- Min. timing analysis (Hold Check) with Clock Jitter
- Sources of Clock skew and Jitter

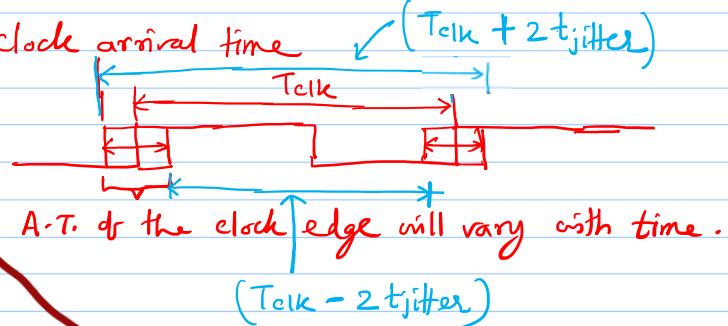
Clock Jitter

SKEW

A large, handwritten-style purple text "Clock Jitter" is centered at the bottom. Below it, a wavy teal line underlines the entire word. To the right, the word "SKEW" is written in a green, handwritten-style font. A green curved arrow points from the top of the "K" in "SKEW" towards the "J" in "Clock Jitter". Below "SKEW", there are two parallel red lines.

What is clock jitter?

- ① Clock jitter is basically a random variation of clock arrival time $(T_{clk} + 2t_{jitter})$ and $(T_{clk} - 2t_{jitter})$.
- clk ↑ or ↓ w.r.t. to time
- ② Clock period will increase or decrease with time.
- ③ Cycle-to-cycle jitter \Rightarrow Timing varying deviation of a single clock period.
- ④ It can be modelled using a zero mean random variable.

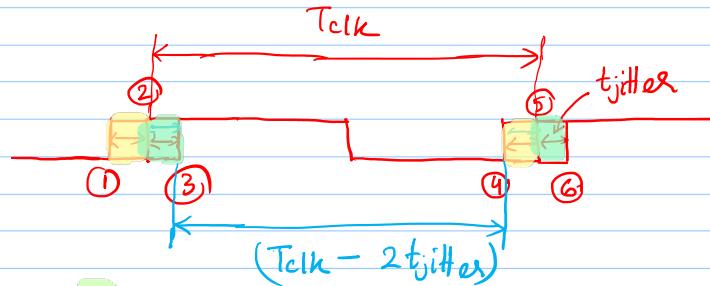


clk

but
Period Same
with Skew

Max timing Analysis with jitter

MAX ANALYSIS



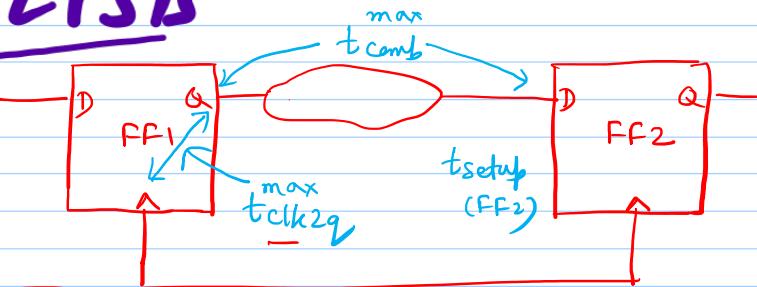
Case I (without jitter) \rightarrow FF1 samples at edge ②]
 FF2 " at edge ⑤] $\rightarrow T_{clk}$

$$T_{clk} \geq t_{clk2q}^{\max} + t_{\text{comb}}^{\max} + t_{\text{setup}} \quad \checkmark$$

Case II (with jitter) \rightarrow FF1 samples at edge ③ \leftarrow late]
 FF2 " " " ④ \leftarrow early] $T_{clk} - 2t_{jitter}$

$$T_{clk} - 2t_{jitter} > t_{clk2q}^{\max} + t_{\text{comb}}^{\max} + t_{\text{setup}}$$

$$T_{clk} > t_{clk2q}^{\max} + t_{\text{comb}}^{\max} + t_{\text{setup}} + 2t_{jitter} \quad \checkmark$$



Tclk will be increase by $2t_{jitter}$

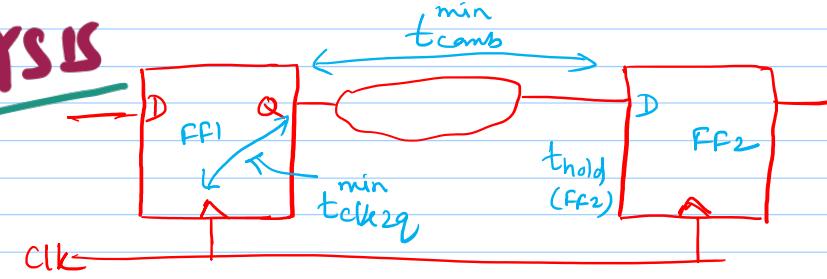
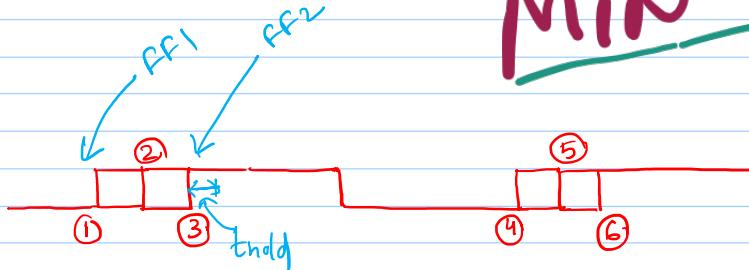
$$T_{clk} \uparrow \Rightarrow f_{clk} \downarrow$$



Subtract
2tjitter
from tclk

Min. Timing analysis with jitter

MIN ANALYSIS



Case I (without jitter) : Edge ② is considered by FF1 and FF2

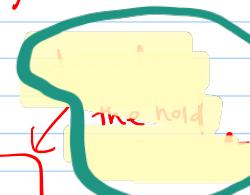
$$thold \leq t_{clk2q}^{\min} + t_{comb}^{\min}$$

Case II (with jitter) : FF1 should sample at edge ① } Worst case
FF2 " " " " " ③ } condition

$$thold \rightarrow (thold + 2t_{jitter})$$

$$thold \leq t_{clk2q}^{\min} + t_{comb}^{\min}$$

$$thold \leq t_{clk2q}^{\min} + t_{comb}^{\min} - 2t_{jitter}$$



Add with
THOLD
What it do?

Sources of skew and jitter :

Clock jitter

① Clock generation \rightarrow PLL \rightarrow VCO \rightarrow clock jitter

crystal

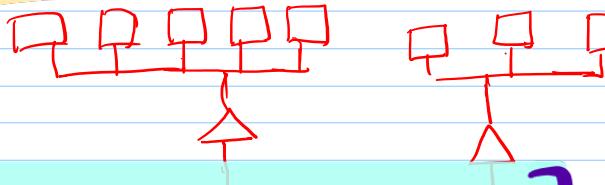
② Power Supply variation \rightarrow Clock generation circuit \rightarrow clock jitter

③ Coupling to Adjacent lines — Clock jitter

SOURCES

JITTER

$$\frac{1}{f}$$



① Frequency variation.

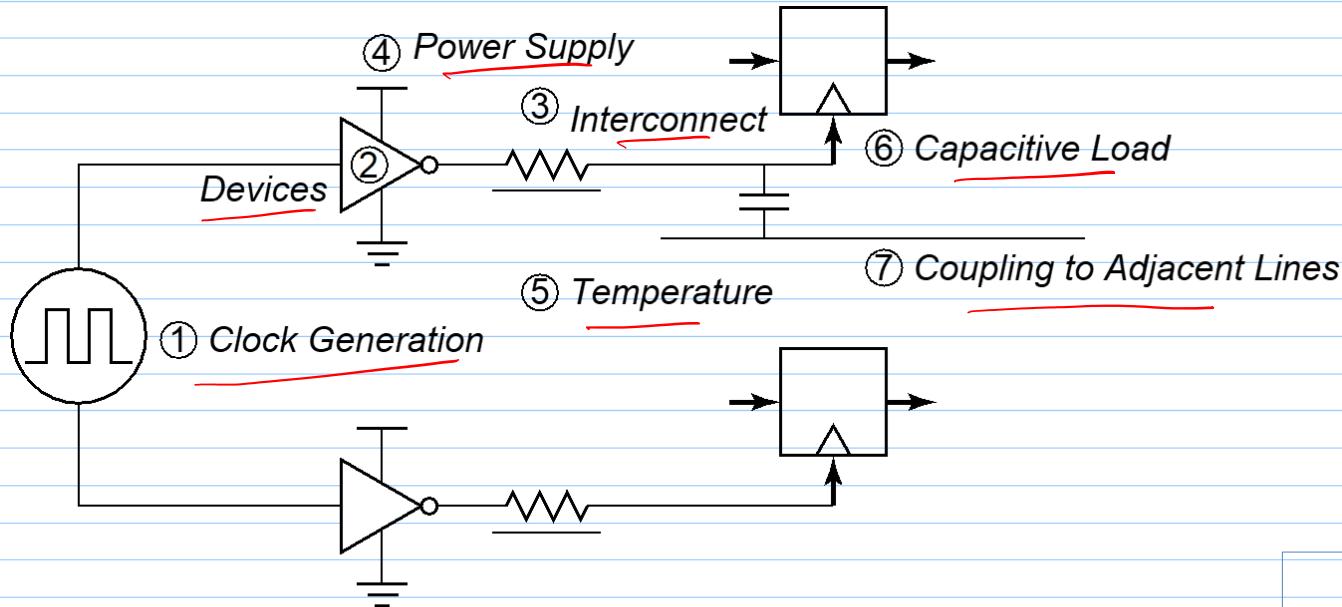
② Device or Process Variation (Within die) — (i) RDP (ii) LER (iii) OTV

③ Capacitive load variation.

④ Temperature variation (clock jitter and skew)

Both

SKEW



Sources of clock uncertainty

Source : Digital Integrated Circuits: A Design Perspective by Jan Rabaey, Anantha Chandrakasan, Borivoje Nikolic

New FORMULAE'S:

$$\text{Data req. time} = \text{Launch clk path} + \frac{\text{Max data path}}{\text{clock period}}$$
$$\text{Data arrival time} = \text{Capture clk path} + \text{clock period} - t_{\text{setup}} (\text{FF}_2)$$

For setup time check

Data arrival time \leq Data required time

For Hold time check

\geq

Contents

- Launch FF and Capture FF
- Max. timing analysis (Setup check) without variation
- Max. timing analysis (Setup check) ~~with on-chip variation (OCV)~~
- Max. timing analysis (Setup check) ~~with OCV~~ + CRPR

SETUP
CHECK

MAX
ANALYSIS :

LAUNCH

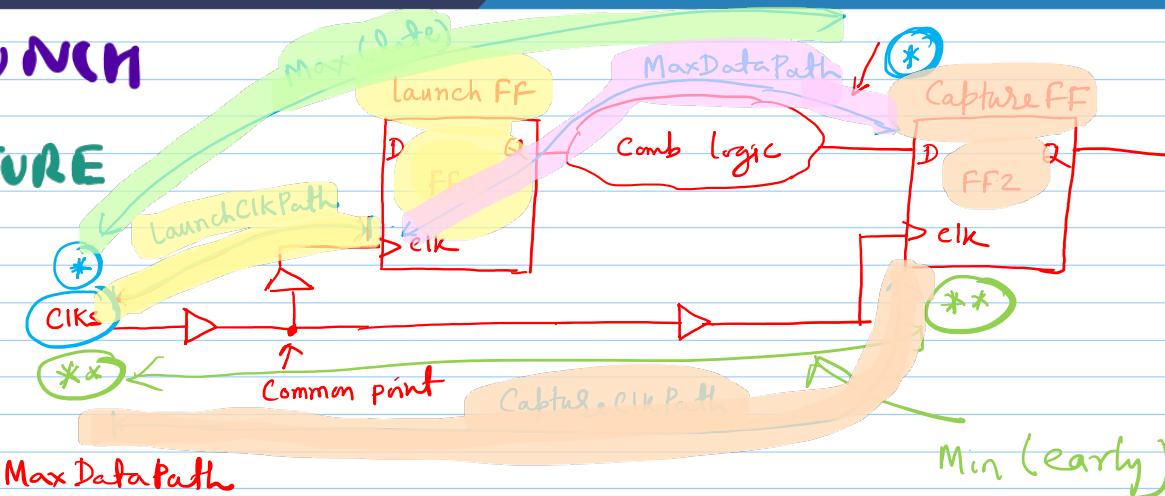
CAPTURE

FF1 - launch FF

FF2 - Capture FF

①

②



$$\text{Data Arrival time} = \text{Launch Clk Path} + \text{Max Data Path}$$

$$\text{Data Required time} = \text{Clock Period} + \text{Capture Clock Path} - t_{\text{setup}}(\text{FF2})$$

For Setup time check

$$\text{Data arrival time} \leq \text{Data Required time}$$

for good Setup check

$$\boxed{\text{DRT} \geq \text{DAT}} \\ (\text{Setup component})$$

In general case (with clock buffer in clock tree)

$$DAT \leq DRT$$

$$\text{Launch ClkPath} + \text{Max Data Path} \leq \text{Clock Period} + \text{Capture Clock Path} - t_{\text{setup}}$$

Special Case (No buffer in clock tree) \leftarrow "Ideal case"

$$\text{Launch ClkPath} = 0$$

$$\text{Capture ClkPath} = 0$$

$$\text{Max Data Path} \leq \text{Clock Period} - t_{\text{setup}}$$

$$\Rightarrow t_{\text{clk2g}}^{\max} + t_{\text{comb}}^{\max} \leq T_{\text{clk}} - t_{\text{setup}}$$

$$\Rightarrow t_{\text{clk2g}}^{\max} + t_{\text{comb}}^{\max} + t_{\text{setup}} \leq T_{\text{clk}}$$

COMBINE
Both H
formulas

if only 3 terms

MAX
Data
path

$$\leq T_{\text{clk}} - t_{\text{setup}}$$

IDEAL

$$t_{\text{clk2g}}^{\max} + t_{\text{comb}}^{\max} + t_{\text{setup}} \leq T_{\text{clk}}$$

SLACK

HOW MUCH
DELAY MARGIN
WE HAVE?



$$DRT - DAT$$

as

$$DRT \geq DAT$$

↳ Slack = 0 $DRT = DAT \rightarrow$ min clock period

↳ +ve slack \Rightarrow $DRT \geq DAT$ is what we require
so, extra margin

↳ -ve slack \Rightarrow $DAT \geq DRT$ we have
 \times → Setup Violation

3 Cases :

Numerical⁸:

on Slack

Case ① w/o OCV

Ex-1

GIVEN

$$T_{CKL} = 7.2 \text{ ns}; t_{setup} = 0.5 \text{ ns}$$

①

Case I (without variation)

$$\text{Launch Clock Path} = 1.5 \text{ ns} + 0.9 \text{ ns} = 2.4 \text{ ns}$$

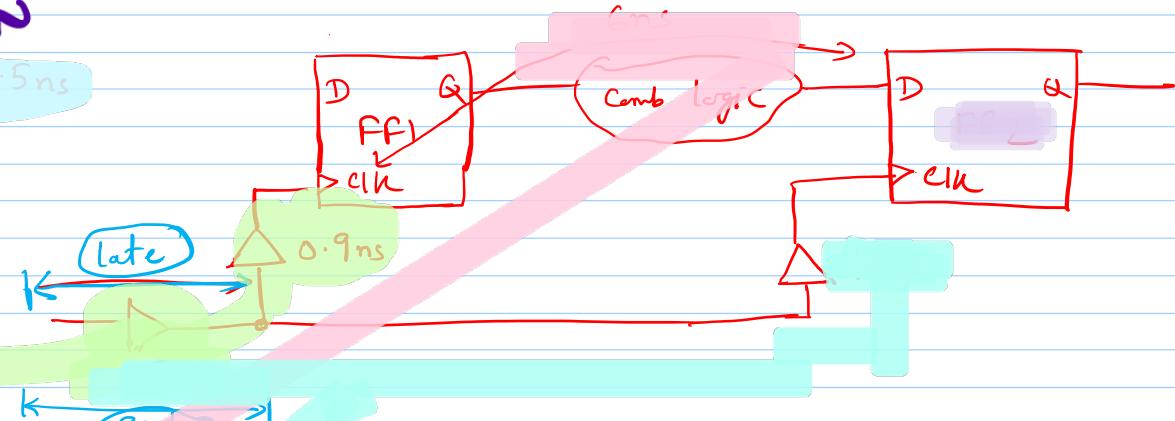
$$\text{Setup Data Path} = 0.5 \text{ ns}$$

$$\text{Launch DkPath} = 1.5 \text{ ns} + 1.1 \text{ ns} = 2.6 \text{ ns}$$

$$t_{clock} = 0.5 \text{ ns}$$

$$DAT = 2.4 + 0.5 = 8.4 \text{ ns}$$

$$DRT = 7.2 + 0.5 - 0.5 = 9.3 \text{ ns}$$



$$\text{Slack} = DRT - DAT$$

$$= 9.3 - 8.4 = 0.9 \text{ ns}$$

Check
Slack

and setup requirement

is satisfied



Case ②:

Slack With OCV

Set-timing-decide - early
- late

- late \rightarrow Cell check

Applicable for setup & hold times

with OCV

Worst Case Analysis	Nature	Multiply with
Capture clock path	Early (Min.)	Set-timing-decide - early
Launch "	Late (Max)	" " " - late
Max Data "		" " " - late
Setup time of ff ₂	Late (Max)	" " " - late * Cell Check
# Now again find	Slack =	DRT-DAT

Case II (with OCV) -  local variation (inside the same die)

Case

#



2

OCV

Launch Clk Path = $2.4 \text{ ns} \times 1.1 = 2.64 \text{ ns}$

lat

Max Datapath = $6 \text{ ns} \times 1.1 = 6.6 \text{ ns}$

Capture Clock Path = $2.6 \text{ ns} \times 0.85 = 2.21 \text{ ns}$] early

$t_{\text{setup}} = 0.5 \text{ ns} > 1.05 = 0.525 \text{ ns}$]

all check

DAT = $2.64 + 6.6 = 9.24 \text{ ns}$

NEW

DRT = $2.21 \text{ ns} - 0.525 \text{ ns} + 7.2 \text{ ns} = 8.885 \text{ ns}$

Slack = DRT - DAT = -0.355 ns ← Setup violation

-ve Slack coming
S.V. ↙

Case ③ : Slack With OCV & CRPR



delay difference along this common position of the clock tree due to diff. derating for
① Launch —
② Capture clock paths

Latest A.T @
Common Point

— Earliest A.T @
Common Point

Add this error in Prev. Case ② Slack

& then Check Slack Again.

Case III (with OCV + CRPR)

CRPR = Clock Recovery and Precharge Recovery

CPP = is the delay

Duration of the clock tree due to the

for launch and capture clock paths

CPP = latest A.T @ common point - Earliest A.T @ common point

$$= (1.5 \text{ ns} \times 1.1 - 1.5 \text{ ns} \times 0.85) = 0.375 \text{ ns}$$

$$\text{Slack} = -0.355 \text{ ns} + 0.375 \text{ ns} = 0.02 \text{ ns} = 20 \text{ ps}$$

Now Slack is +ve. \Rightarrow No setup violation

$$\text{Slack} = \text{DRT} - \text{DAT}$$

$$\text{Slack} (\text{OCV} + \text{CRPR})$$

$$= \text{Slack} (\text{OCV}) + \boxed{\text{CPP}}$$

Case ③



Contents

- Launch FF and Capture FF
- Min. timing analysis (hold check) without variation
- Min. timing analysis (hold check) with on-chip variation (OCV)
- Min. timing analysis (hold check) with OCV + CRPR

DAT \geq DRT
OPP.

Same as Previous Max. \rightarrow Min Case

STA

Timing Analysis

Hold check

For Hold check

Data arrival time (DAT) = launch Clock Path +

Path taken by data

Data Required time (DRT) = Capture Clock Path + t_{hold}

For Hold check:

DATA \geq DRT

opp. DATA \geq DRT

Slack = Data arrival time - Data Required time

Case I :

$\Rightarrow \text{DAT} > \text{DRT} \Rightarrow \text{No hold violation}$

Case II :

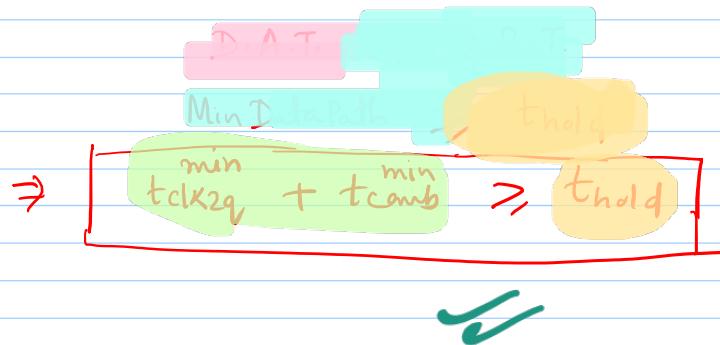
Slack is -ve $\Rightarrow \text{DAT} < \text{DRT} \Rightarrow \text{hold violation}$

Slack = $\text{DAT} - \text{DRT}$

Special Case! (No buffer in the clk tree)

Launch CLK Path = 0

Capture CLK Path = 0

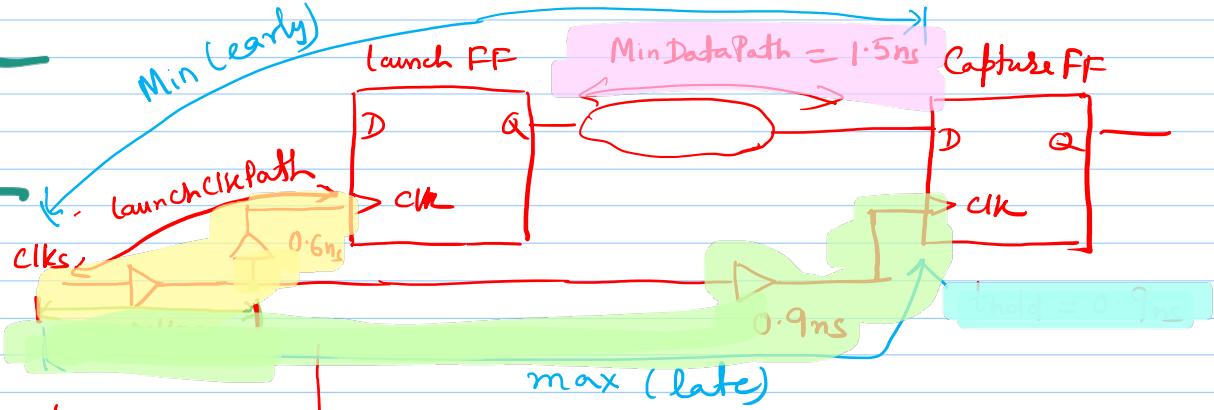


Case ①

I DEAL

Ex:1

EXAMPLE



Case I (without variation)

$$\text{Launch CLK Path} = 0.4 + 0.6 = 1\text{ns}$$

$$\text{MinDataPath} = 1.5\text{ ns}$$

$$\text{Capture Clock Path} = 0.4 + 0.9 = 1.3\text{ ns}$$

$$\text{DAT} = 1\text{ns} + 1.5\text{ ns} = 2.5\text{ ns}$$

$$\text{DRT} = 1.3\text{ ns} + 0.7\text{ ns} = 2.2\text{ ns}$$

$$\text{Slack} = \text{DAT} - \text{DRT} = 2.5 - 2.2 = 0.3\text{ ns}$$

Slack is +ve

hold requirement is met

Just check like
this

Case II (with OCV) — local variation inside the same die

set-timing-degrade

- early

0.85

set-timing-degrade

- late

1.1

set-timing-degrade

- early

0.9

- cell-check
hold

$$\text{Launch Clk Path} = 1\text{ns} \times 0.85 = 0.85\text{ns}$$

$$\text{Min Data Path} = 1.5\text{ns} \times 0.85 = 1.275\text{ns}$$

$$\text{Capture Clk Path} = 1.3\text{ns} \times 1.1 = 1.43\text{ns}$$

$$\text{DAT} = 2.125\text{ns} ; \text{DRT} = 2.24\text{ns}$$

$$\text{Slack} = \text{DAT} - \text{DRT} = -0.115\text{ns}$$

Slack =

?

hold v' " "

Case ②

With OCV

-ve slack

Case III

(with OCV + CRPR)

?

$$CPP = 0.4 \times 1.1 - 0.4 \times 0.85 = 0.1\text{ns}$$

$$\text{Slack} = -0.115 + CPP = -0.015$$

Add \downarrow $= -15\text{ps}$

Hold violation exists



Buffer insertion in the datapath

Note! Hold check is independent of the time period of the clk.



Case 3

$$\text{Slack} = DAT - DRT$$

Case II (OCV)

$$\text{Slack (OCV)} = DAT - DRT$$

Case III (OCV + CRPR)

$$\text{Slack (OCV + CRPR)} = DAT - DRT$$

$$= (DAT - \text{extra}) - DRT$$

New

extra

STA for Combinational Chks

- Types of Path
- Arrival time and Required time
- Output Arrival time for (1) Inverting gate and (2) Non-inverting gate
- Input Required time for (1) Inverting gate and (2) Non-inverting gate

①

②

Types of Paths in

Combinational Circuits

- ① Critical Path or longest path in a design (setup check) ✓
- ② Short Path or Min data path in a design/circuit (Hold check)
- ③ False Path

Path
Critical
Short
False

• Arrival time: Actual rise and fall times at different nodes due to the rise and fall delay of the logic gates

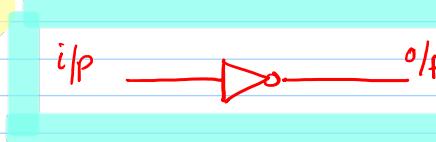
Actual time

• Required time: Rise and fall arrival time required or needed due to the time constraints specified by the circuit designer

Required time

Inverting-type of gates:

① Single-input gates!



$$O/P \text{ A.T. (rise)} = t_2 + t_{rise}$$

$$= i/p A.T. + t_{rise}$$

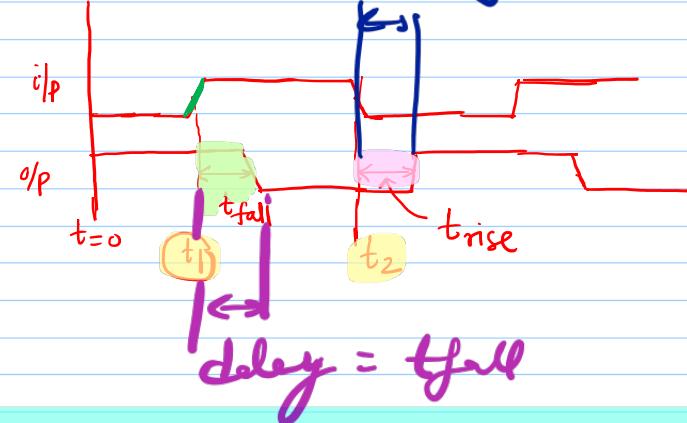
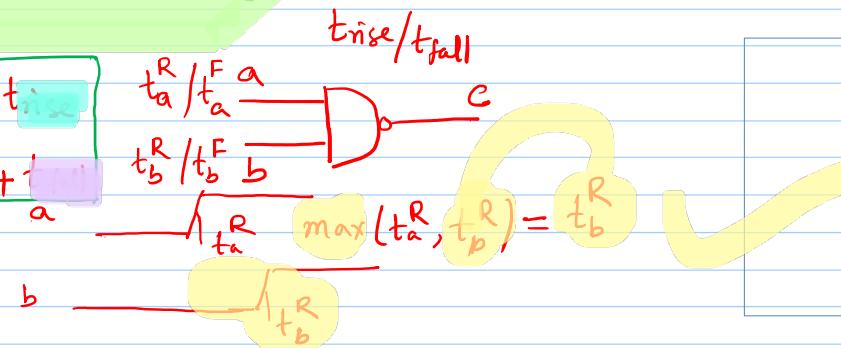
$$O/P \text{ A.T. (fall)} = t_1 + t_{fall}$$

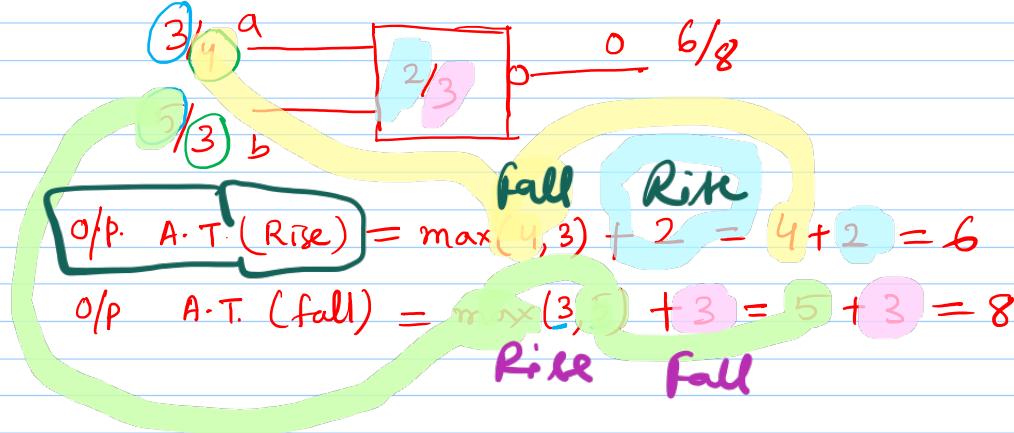
$$= i/p A.T. + t_{fall}$$

② multiple input gates:

$$O/P \text{ A.T. (rise)} = \max(\text{input rise A.T.}) + t_{rise}$$

$$O/P \text{ A.T. (fall)} = \max(\text{input fall A.T.}) + t_{fall}$$





✓

Opk

Non-inverting type ↴

$$\begin{aligned}
 \text{Rise} &= \text{Fall} + \text{Rise} \\
 \text{Fall} &= \text{Rise} + \text{Fall}
 \end{aligned}$$

Non-Inverting type of gates



I/P → O/P

$$O/P \text{ A.T. (Rise)} = t_1 + t_{rise}$$

$$O/P \text{ A.T.} = \text{input Rise A.T.} + \text{Rise delay}$$

$$O/P \text{ A.T. (fall)} = t_2 + t_{fall}$$

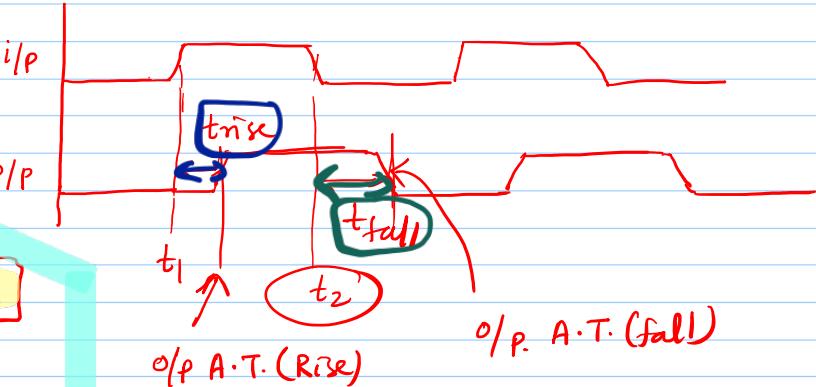
$$O/P \text{ fall A.T.} = \text{input fall A.T.} + \text{fall delay}$$



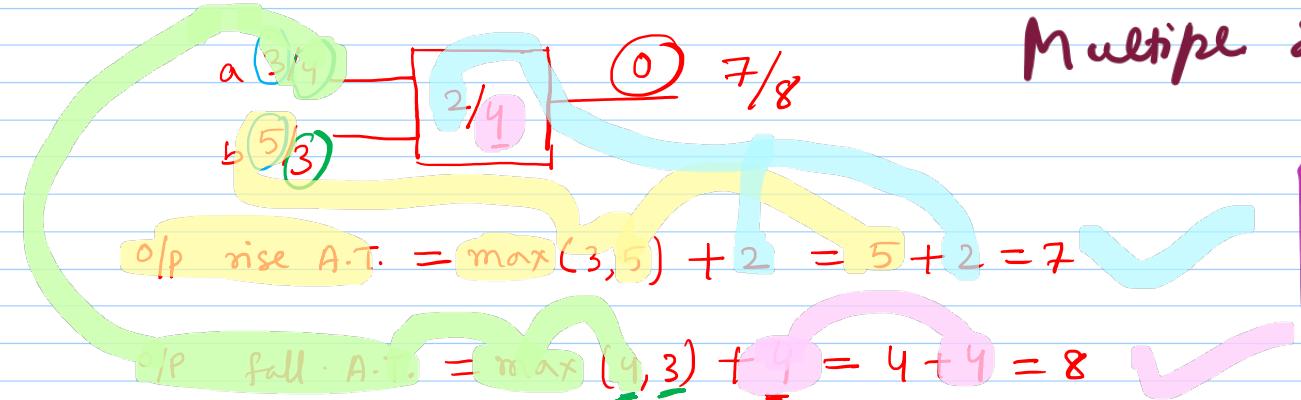
Just Max.

$$O/P \text{ A.T. (rise)} = \max(\text{input rise A.T.}) + \text{Rise delay}$$

$$O/P \text{ A.T. (fall)} = \max(\text{input fall A.T.}) + \text{fall delay}$$



Here $t_{rise} = t_{r1} + t_{rise}$
(same) & $t_{fall} = t_{f1} + t_{fall}$



Multiple J/P

*

Non-inverting
type of gate.

For J/P



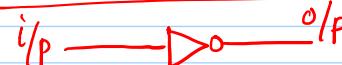
Input A-T. (Rise/fall)

Given Parameters (1) Output A-T (Rise/Fall) (2)

Rise delay / Fall delay

① Inverting - $t_1 = t_{fall}$

(i) Single-input and Single-output

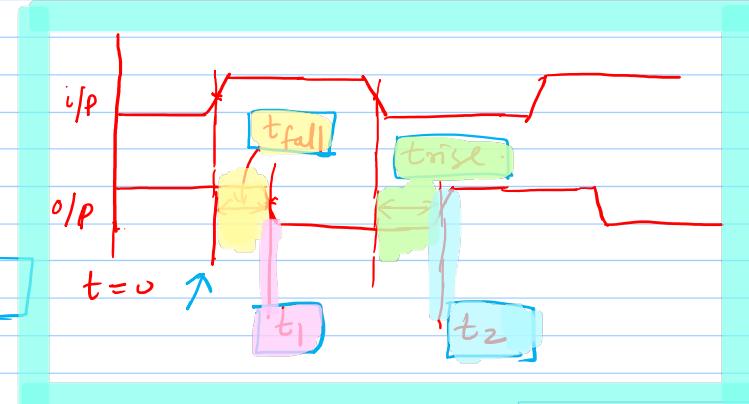


$$\text{input rise A.T.} = t_1 - t_{fall}$$

$$\text{input fall A.T.} = \text{output fall A.T.} - \text{fall delay}$$

$$\text{input fall A.T.} = t_2 - t_{rise}$$

$$\text{input fall A.T.} = \text{output rise A.T.} - \text{Rise delay}$$



Totally opposite

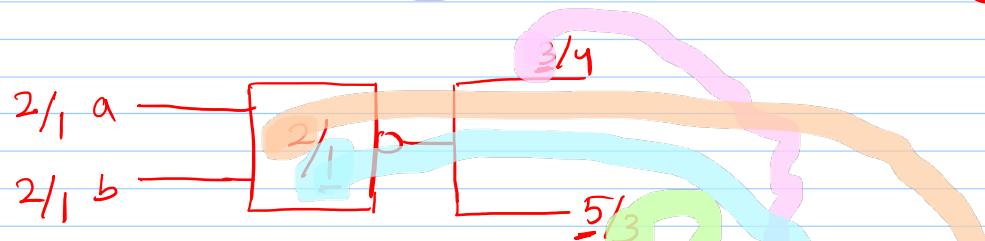
$$\begin{cases} \text{Rise} = \text{fall} - \text{fall delay} \\ \text{Fall} = \text{Rise} - \text{Rise delay} \end{cases}$$

(ii) Multiplexer
Fan-out connected to o/p pin of the gates

$$\text{input rise A.T.} = \text{Min}(\text{output fall A.T.}) - \underline{\text{fall delay}}$$

$$\text{input fall A.T.} = \text{Min}(\text{Output rise A.T.}) - \text{Rise delay}$$

Ex:-



$$\text{input rise A.T. (a or b)} = \text{min}(4, 3) - \underline{1} = 3 - 1 = 2$$

$$\text{input fall A.T. (a or b)} = \text{min}(3, 5) - 2 = 3 - 2 = 1$$

Taking Min.

8

net
max

I/P Total max 21

O/P diff Value min =

Non-Inverting →

Non-Inverting gates :

(1) Single-input and Single-output :



$$\text{rise A.T.} = t_1 - t_{\text{rise}}$$

$$\text{rise A.T.} = \text{o/p Rise A.T.} - \text{Rise delay}$$

$$\text{fall A.T.} = t_2 - t_{\text{fall}}$$

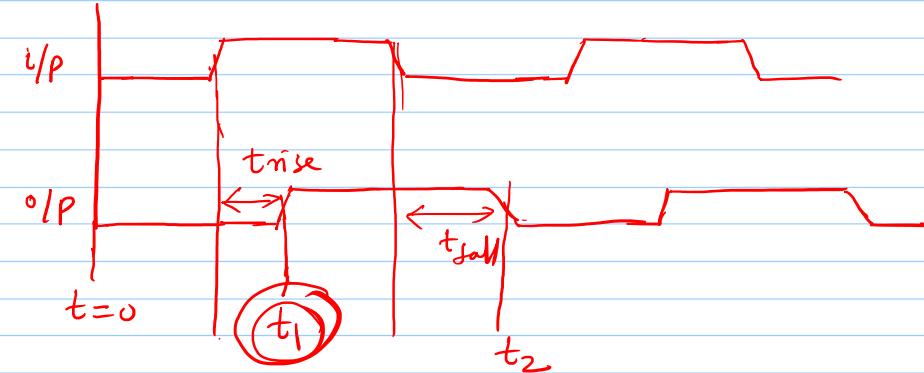
$$\text{fall A.T.} = \text{o/p fall A.T.} - \text{fall delay}$$

2) Multiple Inputs



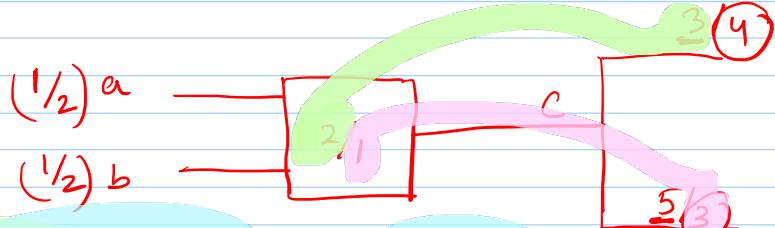
$$\text{i/p. rise A.T.} = \min(\text{o/p. Rise A.T.}) - \text{Rise delay}$$

$$\text{i/p. fall A.T.} = \min(\text{o/p fall A.T.}) - \text{fall delay}$$



} Taking \min

Ex



Take Max

Multiply

O/P \rightarrow Max

I/P \rightarrow Min

$$i/p \text{ Rise A.T.} = \text{Min}(o/p. \text{ Rise A.T.}) - \text{Rise delay}$$

$$= \text{Min}(\underline{3}, \underline{5}) - 2 = \underline{3-2} = 1$$

$$\begin{aligned} i/p. \text{ Fall A.T.} &= \text{Min}(o/p. \text{ Fall A.T.}) - \text{Fall delay} \\ &= \text{Min}(4, 3) - 1 = \underline{3-1} = 2 \end{aligned}$$

$$i/p (\text{Rise / fall}) \text{ A.T.} = (\frac{1}{2})$$

Invert. Non Inv.

O/P opp
I/P opp

Same
Same

Critical Path finding:

Inverting

type of gates



① Output rise A.T. = max (input fall A.T.) + Rise delay

② Output fall A.T. = max (input rise A.T.) + fall delay

③ input rise A.T. =

input rise R.T. = min (output fall R.T.) - fall delay

④ input fall A.T.

input fall R.T. = min (output rise A.T.) - rise delay

} off. + sum

} off. + off

Ex:

Given $\left(\frac{\text{Rise delay}}{\text{fall delay}} \right)$ for each gate

$$\frac{\text{rise}}{\text{fall}} \text{ A.T. node } "a" = \frac{0}{0}$$

$$", ", ", "b" = \frac{0}{0}$$

$$", ", ", "c" = \frac{0}{0}$$

Req. time

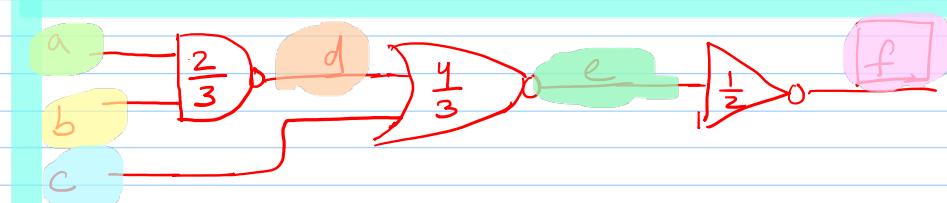
$$\boxed{\text{R.T. at node } "f" = \frac{5}{11}}$$

(i) Find the R.T. at each node

(ii) Find the slack at each node

(iii) Critical path in the circuit

FIND :



$$\text{A.T.} = \frac{0}{0} \quad \begin{matrix} \text{Rise A.T.} \\ \text{Fall A.T.} \end{matrix}$$

$$\text{R.T.} = \frac{2}{-1}$$

$$\text{Slack} = \frac{2}{-1}$$

$$\boxed{\text{Node } b \quad \text{A.T.} = \frac{0}{0}}$$

$$\text{R.T.} = \frac{5-3}{1-2} = \frac{2}{-1}$$

$$\boxed{\text{Slack} = \frac{2}{-1}}$$

$$\text{o/p. R.T. fall} = 5 ; \text{fall delay(NAND)} = 3$$

$$\text{o/p. R.T. rise} = 1 ; \text{rise delay(NAND)} = 2$$

Remember

Node C: $A.T. = \frac{0}{0}$

$$R.T. = \frac{1}{5}$$

$$\text{Slack} = \frac{1-0}{5-0} = \frac{1}{5}$$

Node d:

$$A.T. = \frac{2}{3}$$

i/p fall $A.T. = 0$;
i/p rise $A.T. = 0$;

Rise delay = 2 ;
fall delay = 3

$$R.T. = \frac{4-3}{9-4} = \frac{1}{5}$$

$$\text{Slack.} = -\frac{1}{2}$$

OPP.

o/p. fall $R.T. = 4$; fall delay (NOR) = 3
o/p. rise $R.T. = 9$; rise delay (NOR) = 4

Node e

$$A.T. = \frac{3+4}{2+3} = \frac{7}{5}$$

i/p fall $A.T. = 3$; Rise delay = 4
i/p rise $A.T. = 2$; Fall delay = 3

$$R.T. = \frac{11-2}{5-1} = \frac{9}{4}$$

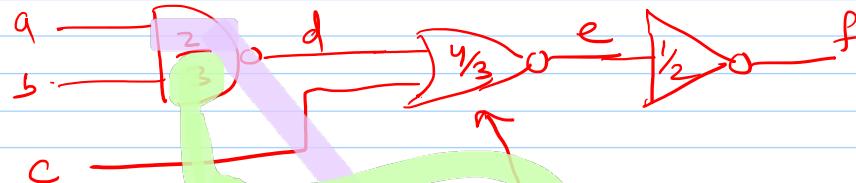
o/p. fall $R.T. = 11$; fall delay = 2
o/p. rise $R.T. = 5$; rise delay = 1

$$\text{Slack} = R.T. - A.T.$$

$$= \frac{9-7}{4-5} = \frac{2}{-1}$$

$$\text{Slack} = \frac{2}{-1}$$

Using them



Node f

$$A.T. = \frac{5+1}{7+2} = \frac{6}{9}$$

{ i/p A.T. fall = 5, Rise delay = 1
i/p A.T. rise = 7, fall delay = 2 }

Using

T/S from
Previous

Given $R.T. = \frac{5}{11}$

$$\text{slack} = R.T. - A.T. = \frac{R.T.(\text{rise}) - A.T.(\text{rise})}{R.T.(\text{fall}) - A.T.(\text{fall})} = \frac{5-6}{11-9} = \frac{-1}{2}$$

Get ΣH at
given ΣI

are Reg - Have ^{up}

*
↑ go
back
do this

with
every
Node

$$A.T. = \frac{0}{0}$$

$$R.T. = \frac{2}{1}$$

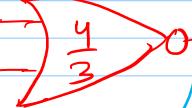
$$\text{Slack} = \frac{2}{-1}$$

$$A.T. = \frac{2}{3}$$

$$R.T. = \frac{1}{5}$$

$$\text{Slack} = \frac{-1}{2}$$

a
b



$$A.T. = \frac{7}{5}$$

$$R.T. = \frac{9}{9}$$

$$\text{Slack} = \frac{2}{-1}$$

c

$$A.T. = \frac{0}{0}$$

$$R.T. = \frac{1}{5}$$

$$\text{Slack} = \frac{1}{5}$$

$$A.T. = \frac{6}{9}$$

$$R.T. = \frac{5}{11}$$

$$\text{Slack} = \frac{-1}{2}$$

f

"f" rising \rightarrow "e" falling \rightarrow "d" rising \rightarrow "a/b" falling