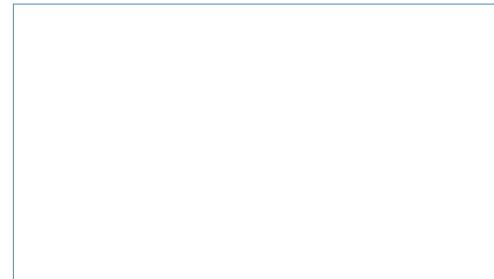


Contents

- Timing Analysis
- Significance of Static Timing Analysis
- STA in VLSI Physical Design
- Static Timing Analysis
- Dynamic Timing Analysis
- Timing Paths

STA



Timing Analysis

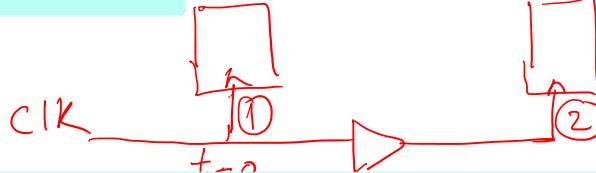
- Timing Analysis assesses and ensures that the designed circuit meets timing and performance requirements.
- Timing parameters of the circuit or chip, such as setup and hold times, clock-to-Q delays, and critical paths are evaluated and optimized.

Significance of Static Timing Analysis

- Determines the **critical path** of the design, which in turn determines the performance of the design.
- Determines the **shortest path** in the design (To avoid hold violation).
- Impact of **clock skew** and **clock jitter** on the timing of the design.
- Impact of **process variations** on the timing of the design.

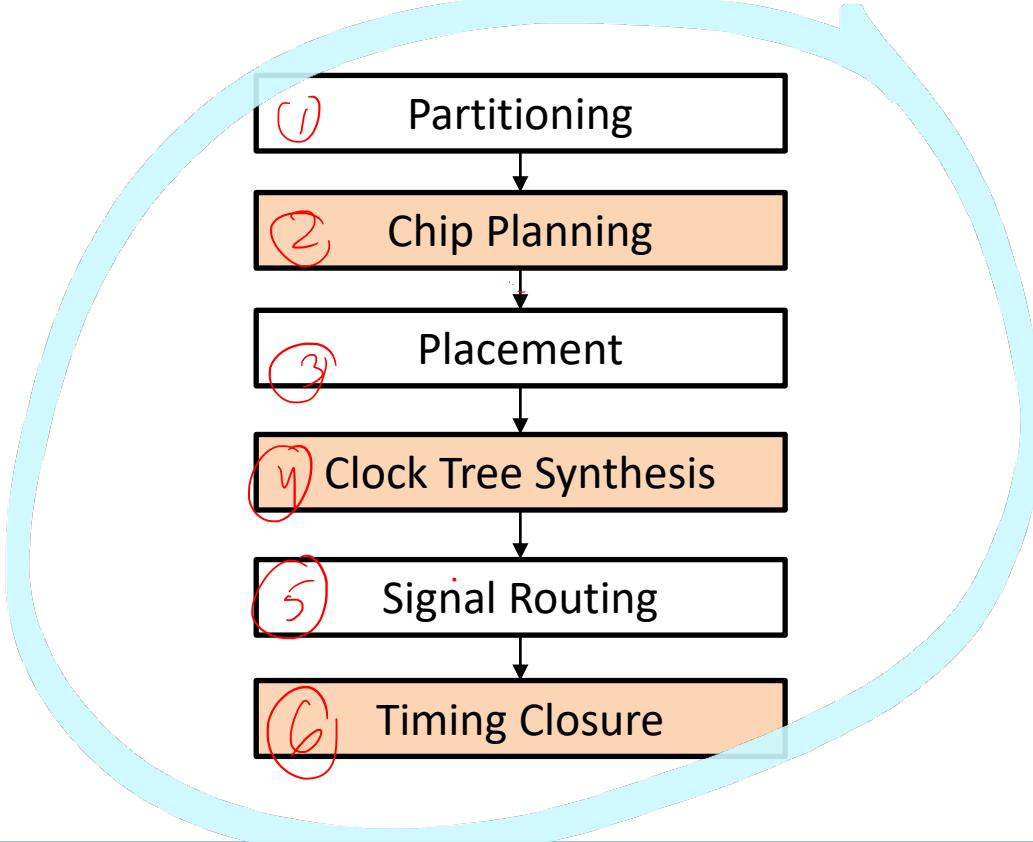


Also imp.



STA in VLSI Physical Design

gmp.



We've to check timing analysis after each step of FLOW.

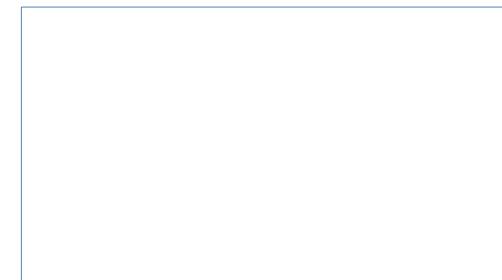
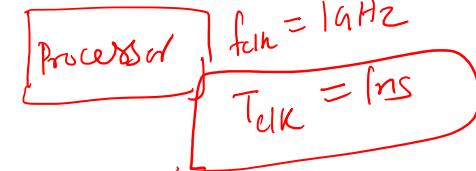
Timing Analysis

- Timing constraints for a chip are tested at a specified clock rate by employing either
 - Static Timing Analysis(STA) or
 - Dynamic Timing Analysis(DTA).



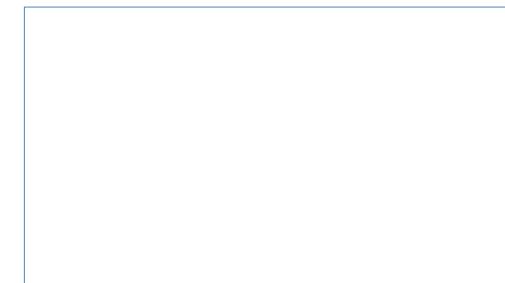
Static Timing Analysis(STA)

- Checks static delay requirements of the circuit without applying input vectors or monitoring output vectors.
- Process of Static Timing Analysis:
 1. Break a design down into timing paths.
 2. Calculate the signal propagation delay along each path.
 3. Check for violations of timing constraints inside the design and at the input/output interface.

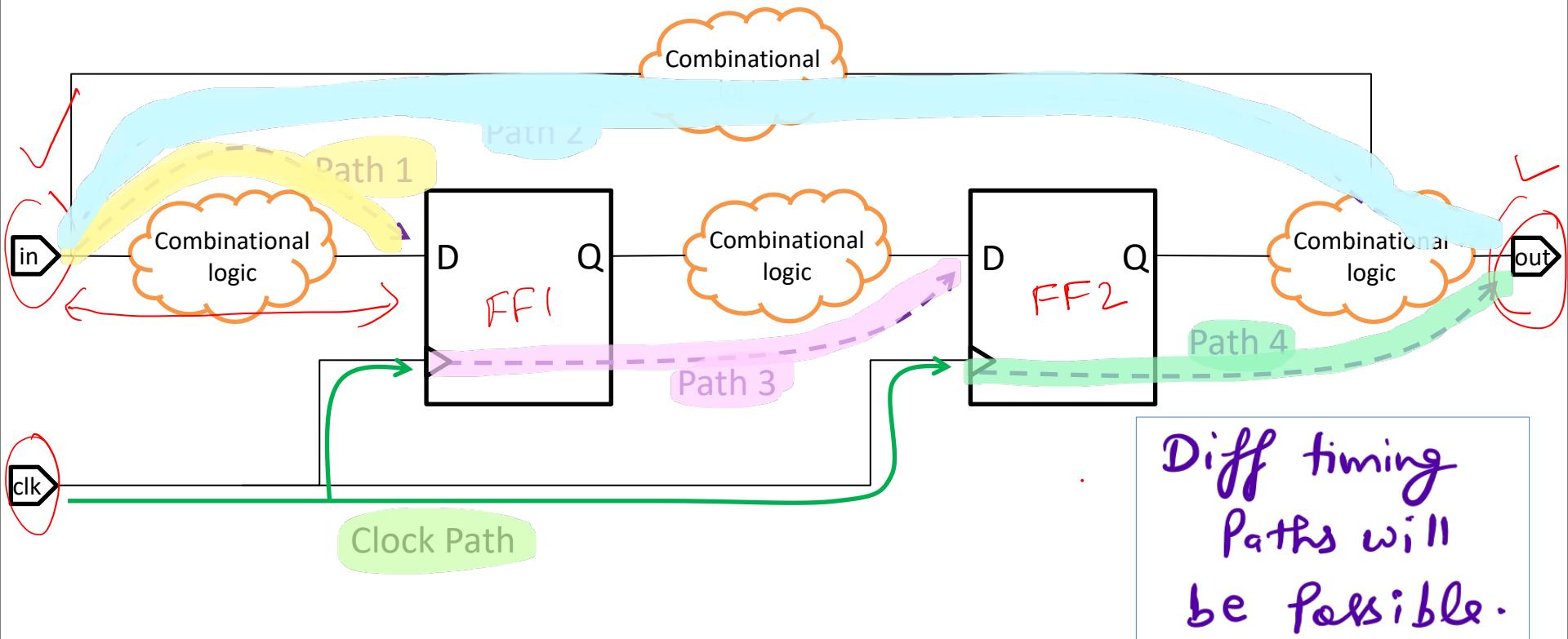


Dynamic Timing Analysis(DTA)

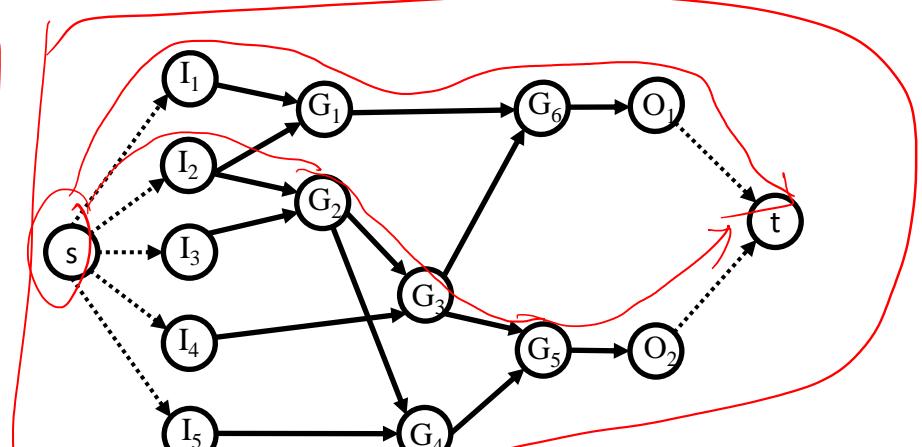
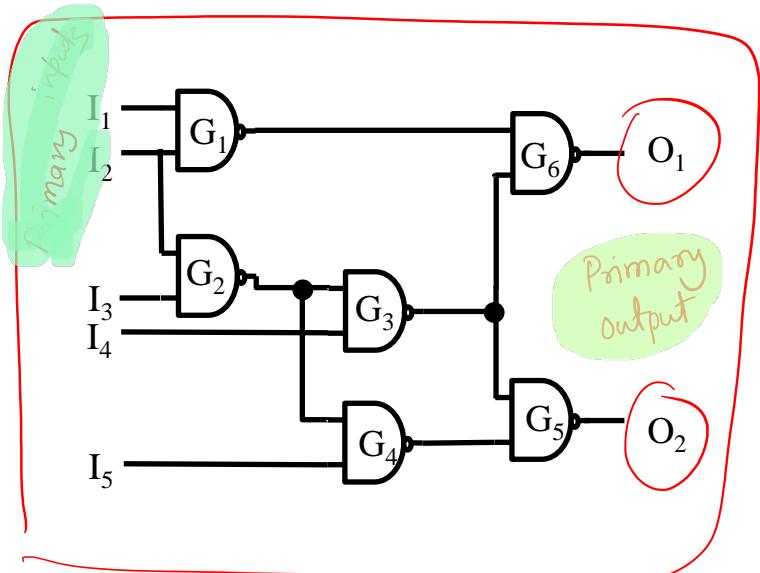
- Verifies functionality of the design by applying input vectors and checking the outputs against expected outputs.
- Checks for logical correctness of the designed circuit.
- Simulation time is relatively more than STA as all inputs need to be checked.
because ↑
- Best suitable for designs having clocks crossing multiple domains



Timing Paths



Timing Paths



Combinational Logic may have multiple paths

Timing Paths

- **Critical Path:** The path between an input and an output with the **maximum delay.**
- **Shortest Path:** The path between an input and an output with the **minimum delay.**

MAX

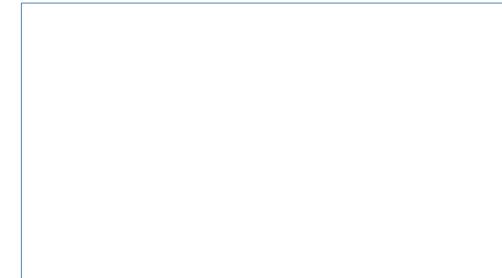
MIN

Critical Path
↳
Maximum Delay

False Path

- A false path is a path that exists in the design which:

1. is not functional
2. is not required to meet its timing constraints for the design to function properly.



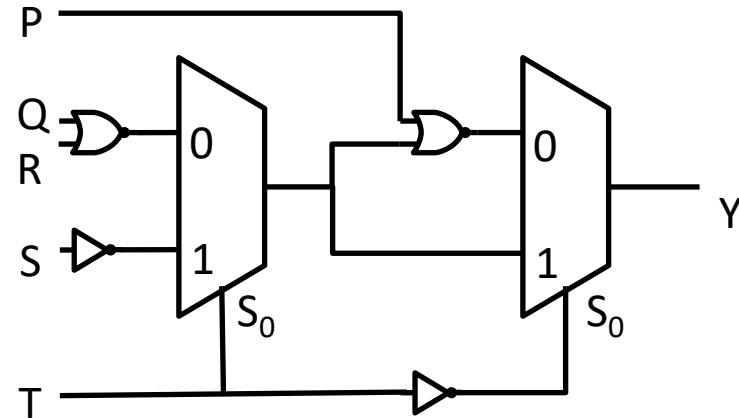
NUMERICALS



Type 1 : Finding Critical Path,
Shortest ->
False Path.

Example

- Let
 - Delay of the NOR gate = 4 ns
 - Delay of the MUX = 3 ns
 - Delay of the NOT gate = 1 ns
- Now, let's find the **critical**, **shortest**, and **longest** paths in the given circuit.

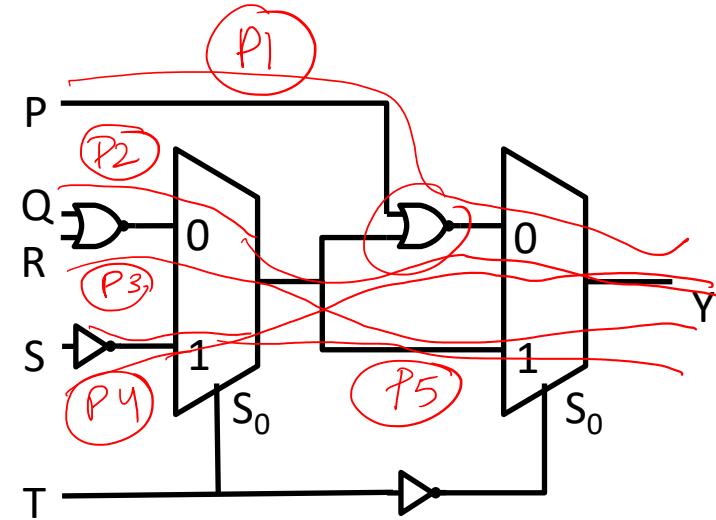


You've to
Find

Example

- Consider the given circuit
 - It has **five paths**
 - P1: NOR + MUX
 - P2: NOR + MUX + NOR + MUX
 - P3: NOR + MUX + MUX
 - P4: NOT + MUX + NOR + MUX
 - P5: NOT + MUX + MUX

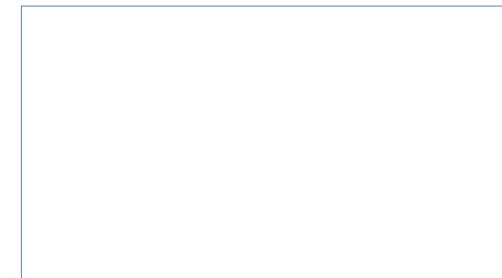
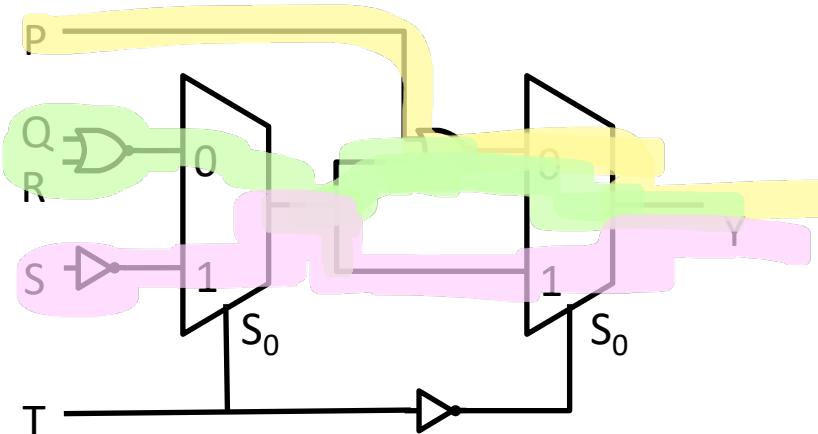
firstly find all the Path &



their
timing.

Example

- Delay of P1 = NOR + MUX
 $= 4 + 3$
 $= 7 \text{ ns}$
- Delay of P2 = NOR + MUX + NOR + MUX
 $= 4 + 3 + 4 + 3$
 $= 14 \text{ ns}$
- Delay of P3 = NOR + MUX + MUX
 $= 4 + 3 + 3$
 $= 10 \text{ ns}$



- Delay of P4 = NOT + MUX + NOR + MUX

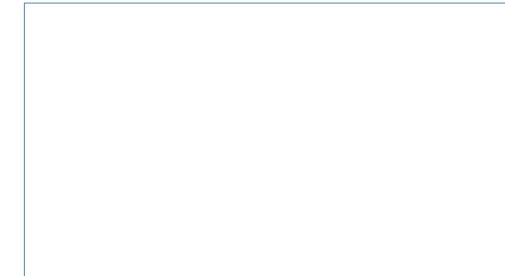
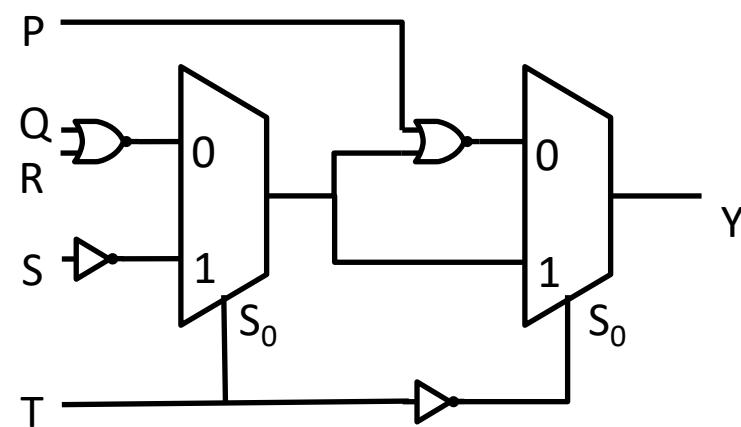
$$= 1 + 3 + 4 + 3$$

= 11 ns

- Delay of P5 = NOT + MUX + MUX

$$= 1 + 3 + 3$$

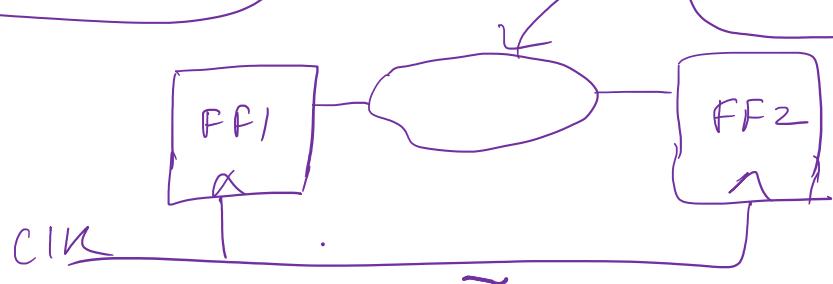
= 7 ns



Summary

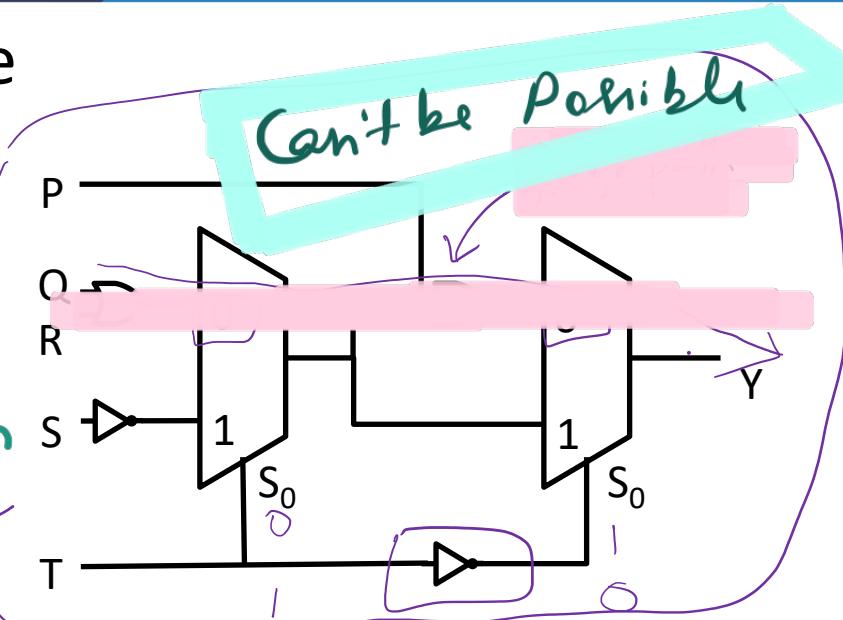
- Delay of P1 = 7 ns
- Delay of P2 = 10 ns → False Path
- Delay of P3 = 10 ns
- Delay of P4 = 11 ns → Critical Path
- Delay of P5 = 7 ns

Example



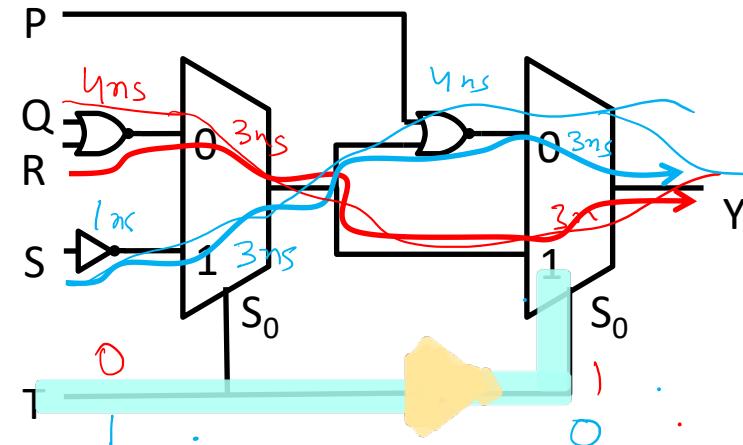
False Path

Critical Path



Two critical paths

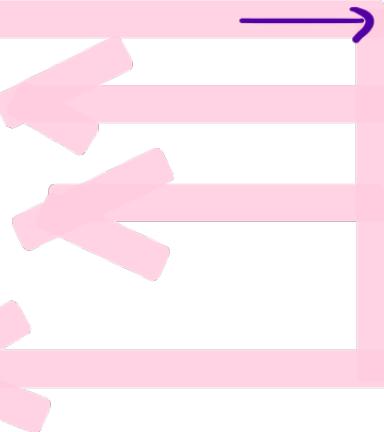
- Critical Path:**
 - Case – 1: $T = 0$**
 - Delay of P3 = NOR + MUX + MUX
 $= 4 + 3 + 3$
 $= 10 \text{ ns}$
 - Case – 2: $T = 1$**
 - Delay of P4 = NOT + MUX + NOR + MUX
 $= 1 + 3 + 4 + 3$
 $= 11 \text{ ns}$
- Actual Critical path delay ✓*

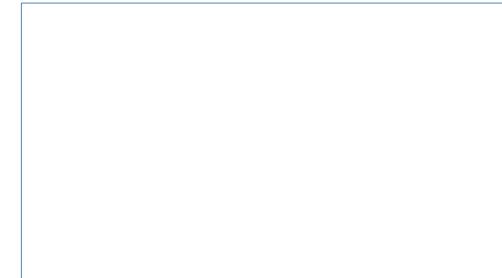


Check for both mux with clock.

STA Starts

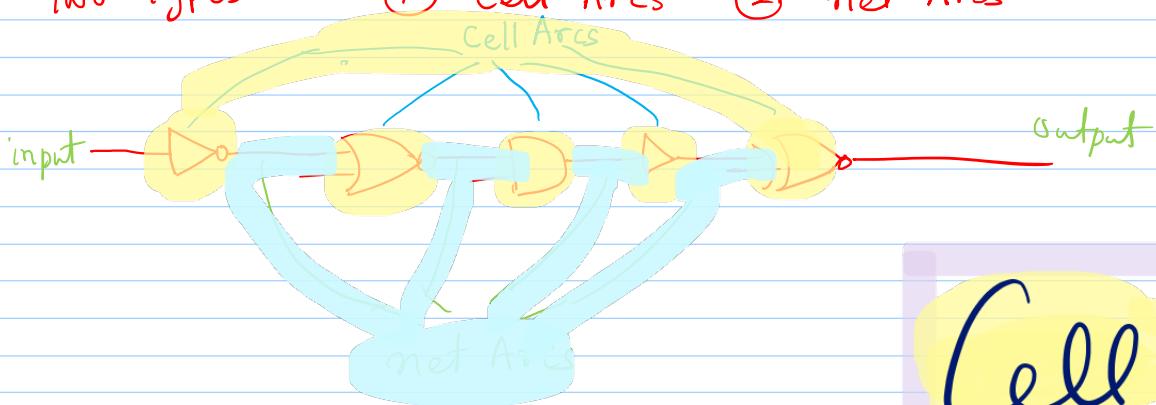
Contents

- Definition of **Timing arcs** → Relationship b/w 2 pins of a Logic GATE.
- **Source Pin** and **Sink pin**
-  → Change in output transition w.r.t. Input transition
 - (1) Positive Unate,
 - (2) Negative Unate
 - (3) Non-Unate
- Use of Unateness



Timing Arcs

- gt is defined as the
- gt is useful for the STA tools to do timing analysis
- gt is basically a part of the timing path
- Two types - ① cell Arcs ② net Arcs



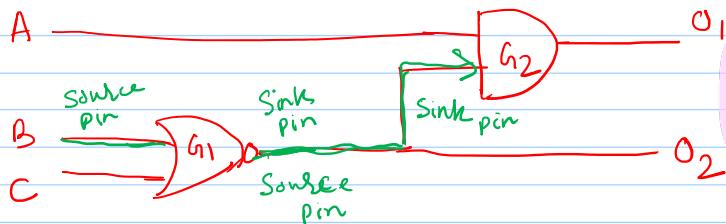
Timing Arcs

2 types

Cell Arcs

Net Arcs

Source Pin and Sink Pin



For gate G_1 , B and C are source pin and O_2 is the sink pin

For gate G_2 , A and O_2 are source pin and O_1 is the sink pin

In case of cell Arcs: input pins ^{of cell} are source pin
output pins ^{of cell} are sink pin

In case of net Arcs: output pin of cell are source pin
input pin of the cells are sink pin

$\mathcal{G}/P \Rightarrow \text{Source Pin}$
 $O/P \Rightarrow \text{Sink Pin}$

For cell Arcs

opposite ← For Net Arcs

Unateness

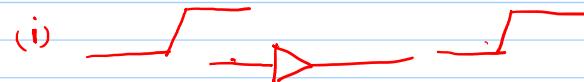
Each timing Arcs has a timing sense.

Change in the output transition  depends on the input transition.

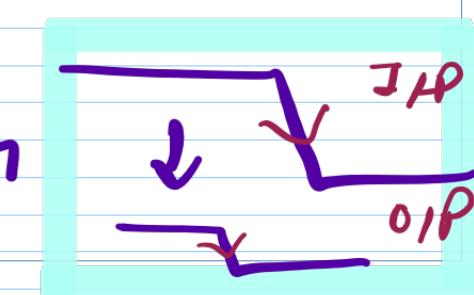
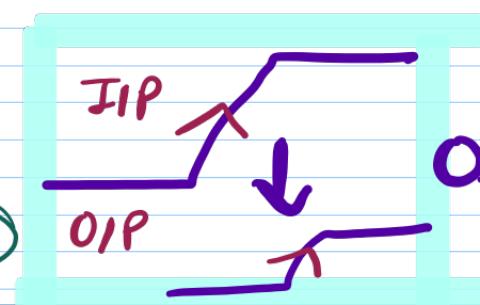
① Positive Unate

input signal is "Rising" \rightarrow Output signal is "rising" or No change.
" " is "falling" \rightarrow " " " " "falling" or No change

Buffer

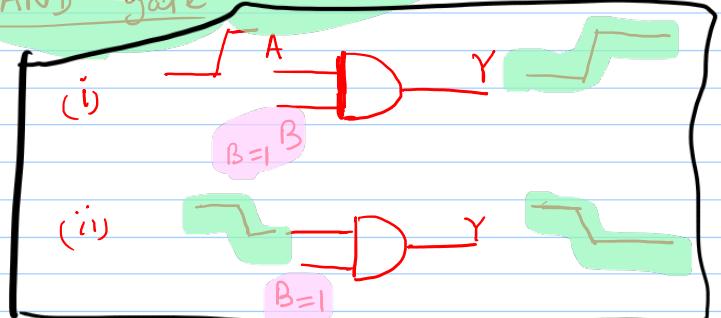


Buffer \rightarrow is ^{+ve} unate
Transition \rightarrow same

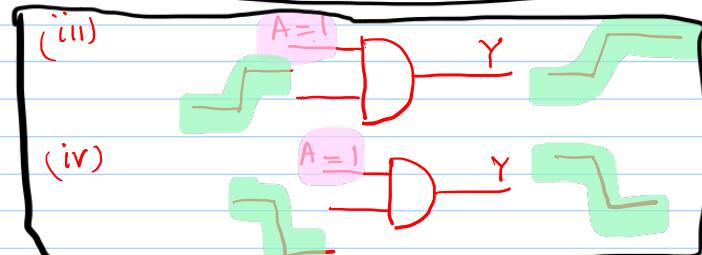


AND gate

$B=1$



$A=1$



(v) X



This Arc \rightarrow Not used
No change

AND gate has 4 timing Arcs

Unate & timing Arcs are two Diff. thing.

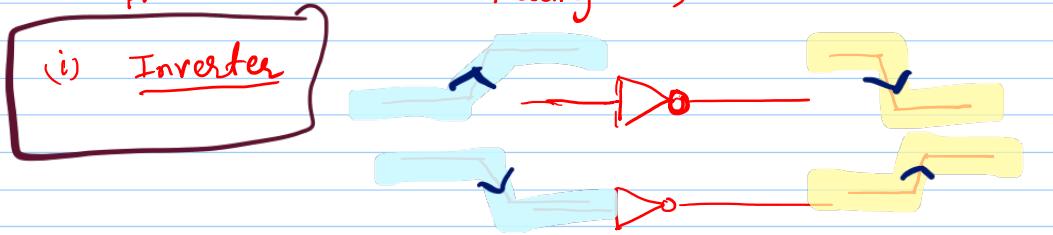
Same Transition

(2) Negative Edge

Change is O/P Waveform

input signal is "rising" → Output signal is "falling" or no change

input " " "falling" → " " is "rising" or no change



2 timing Arcs

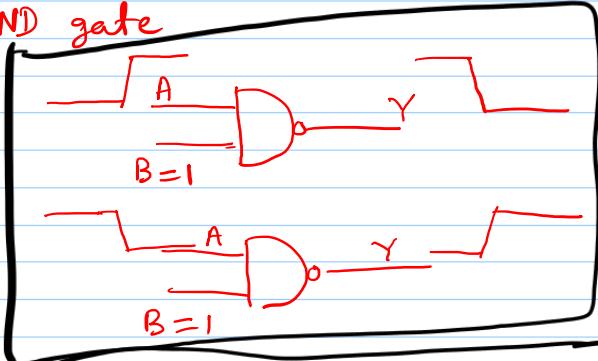
✓ Opp. or No change in Transition

is -ve Edge

(ii) 2-input NAND gate

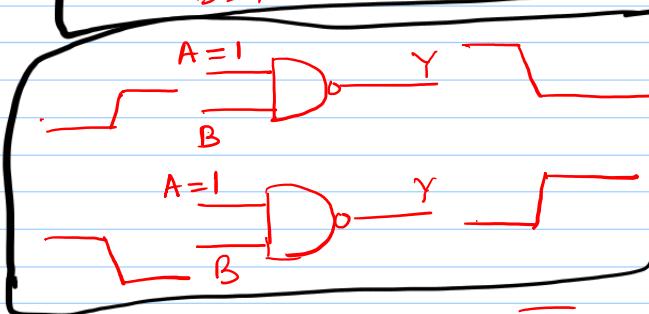
NAND

$B = 1$



4 timing Arcs

$A = 1$



If $B = 0$

$B = 0$

$$Y = \overline{A \cdot B} = \overline{A \cdot 0} = 1$$

then $\rightarrow V_{DD} \rightarrow$

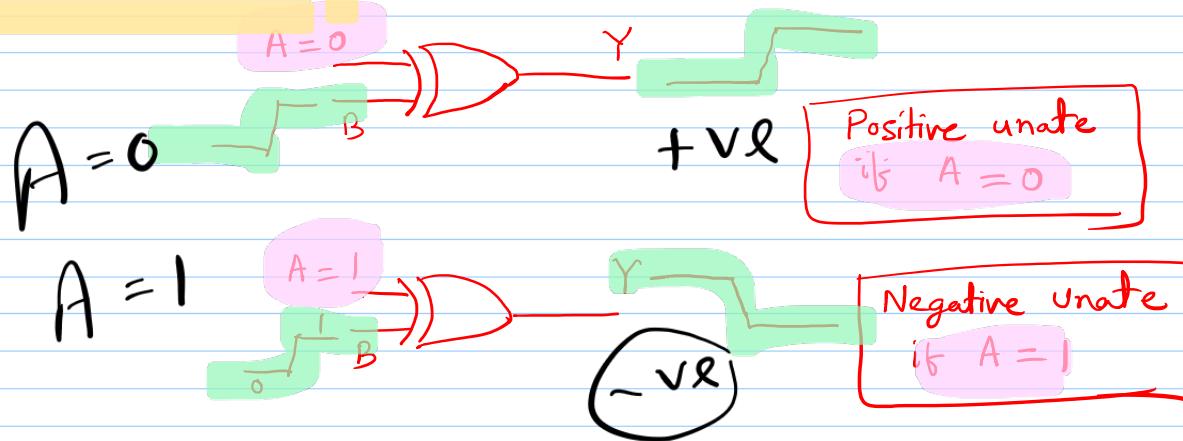
Neg. Unate

NAND gate

Signal is not
Passing

Non-Unate gate

XOR gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

both

Non-unate is that

+vl unate
-vl & unate

Main Timing things

Starts here:



Recovery
Removal

Timing
Arcs
of

Synchronous

s

Asynchronous

Timing Arcs of Sequential Circuits

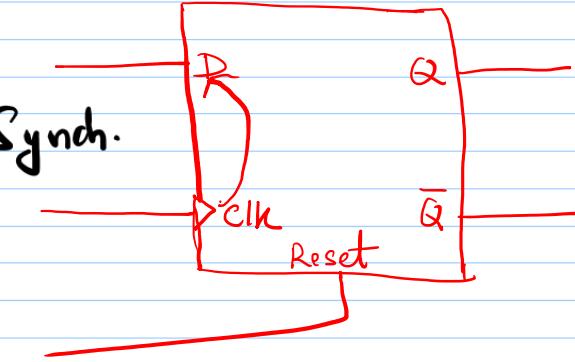
(1) For Synchronous inputs

- (i) Setup check Arc (Rising and falling)
- (ii) Hold check Arc (Rising and falling)

(2) For asynchronous inputs (Reset)

- (i) Recovery check arc
- (ii) Removal check arc

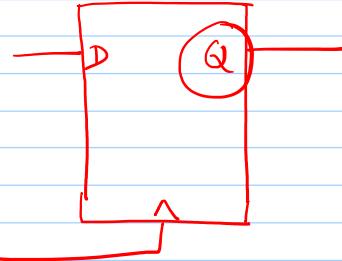
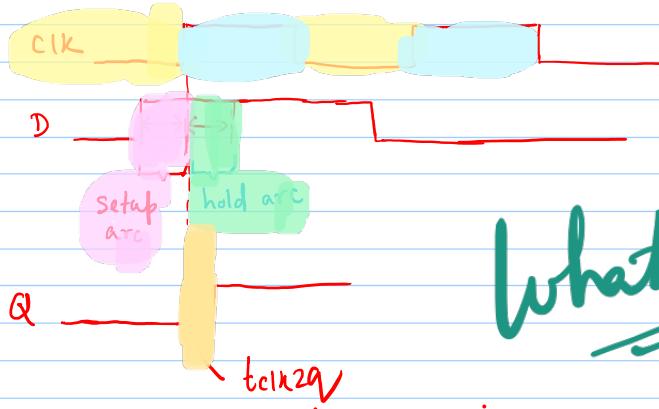
Asynch.



(3) For Synchronous outputs (Q , and \bar{Q})

(i) Clock-to-output propagation delay (rising and falling)





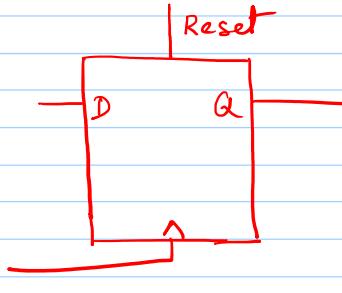
What is t_{clk2q} ?

* q is how much?

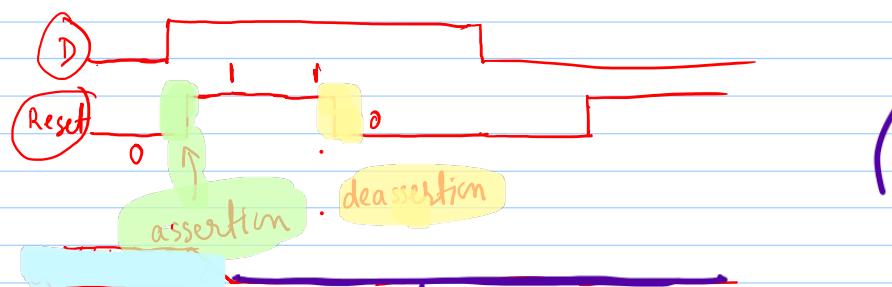
after clock transition

Reset

$$\text{Reset} = 1 \Rightarrow Q = 0$$



CLK

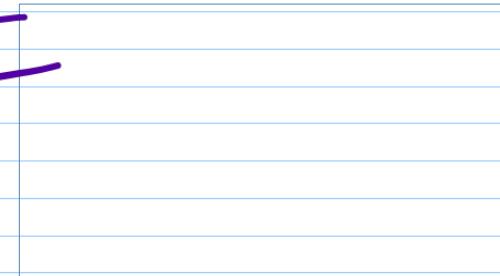


dig something

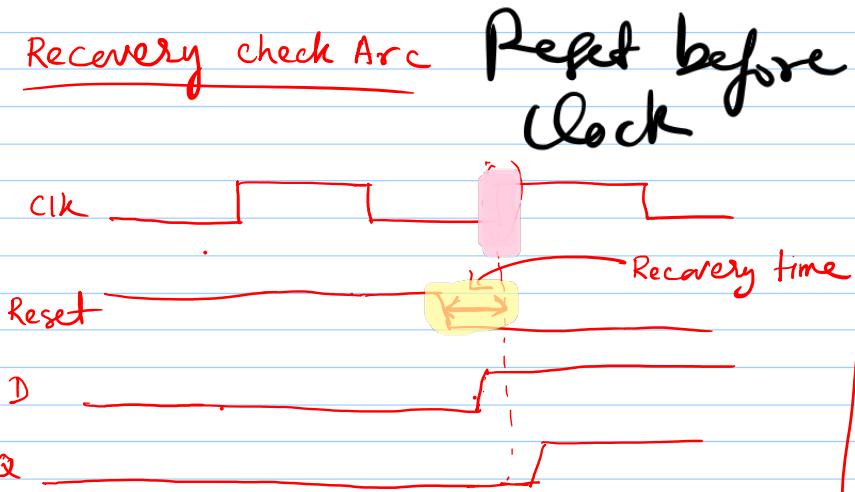


Now it is $1 \rightarrow 0$

Reset

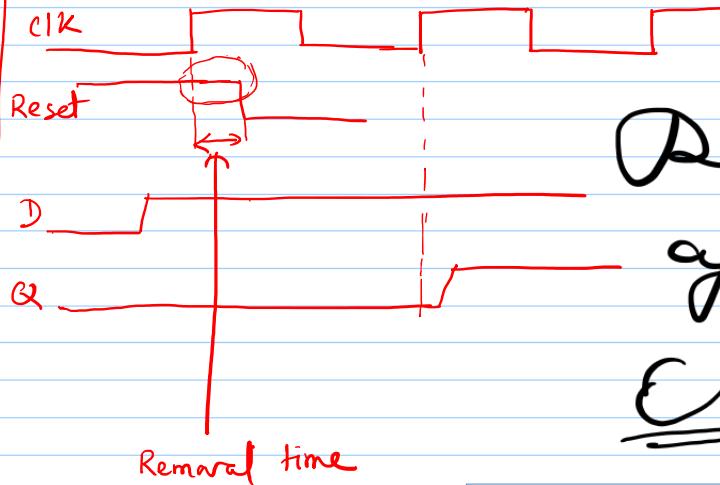


Recovery check Arc



Recovery

Removal check Arc



Removal

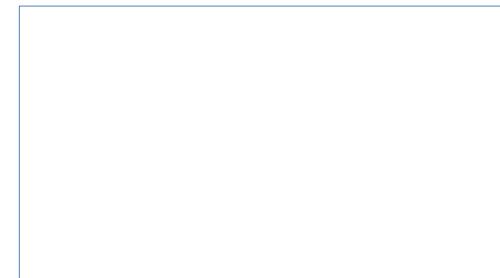
Contents

• Combinational Circuit

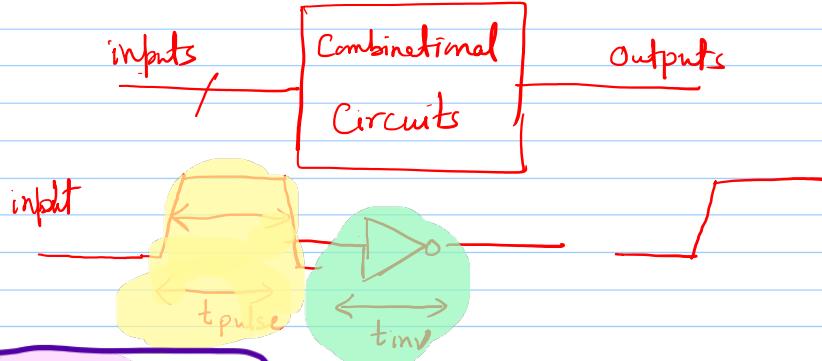
- Delay Parameters of Logic gate

(1) Propagation Delay and (2) Transition time

- Delay of Timing path



What are Combinational Circuits?



Pulse inverter

at Period $2t_{inv}$
✓ $t_{inv} < t_{pulse}$

✓ Case I $t_{pulse} > t_{inv}$, then the pulse will appear at the output of the gate

✗ Case II $t_{pulse} < t_{inv}$, then the pulse will not appear
at the output

✗

This property of the logic gate is called
internal delay property

Propagation Delay of Combinational Circuits :

- It is measured between the 50% transition points of the input and output waveforms.



Types of Propagation Delay

TYPES

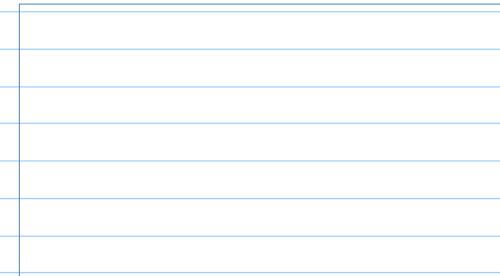
• **Rise Propagation Delay (Tp_{lh})** = The signal-delay time between 50% of the input and 50% of the output when the output changes from low to high level.

Output signal

* • **Fall Propagation Delay (Tp_{hl})** = The signal-delay time between 50% of the input and 50% of the output when the output changes from high to low level!

Output signal

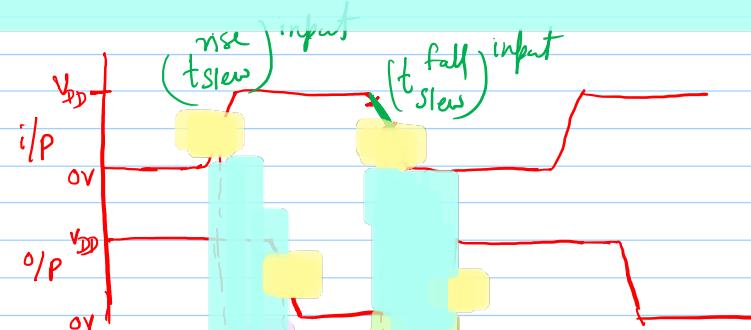
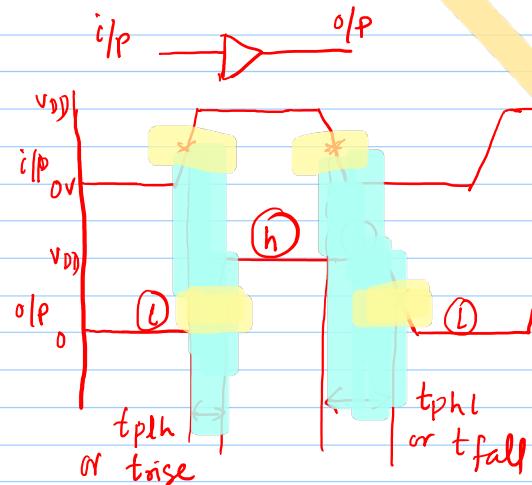
• Average propagation delay t_p = $(T_{phl} + T_{plh})/2$



Inverting gate



Non-inverting gate



O/P
fall

RISE

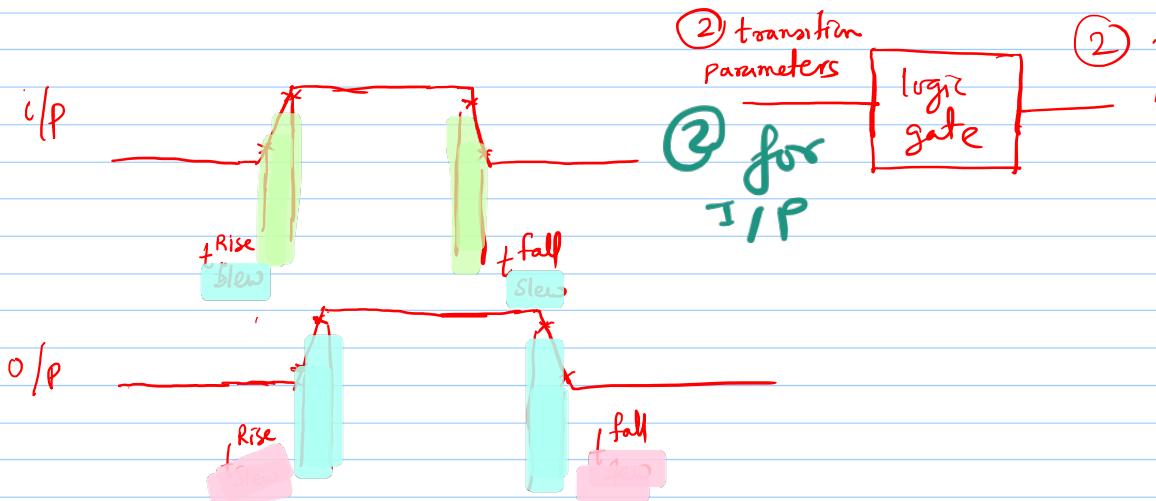
Transition word is used \approx SLEN.

Rise transition delay

- The time taken by the signal to rise from 10% (20%) to 90% (80%) of its maximum value.

Fall transition delay

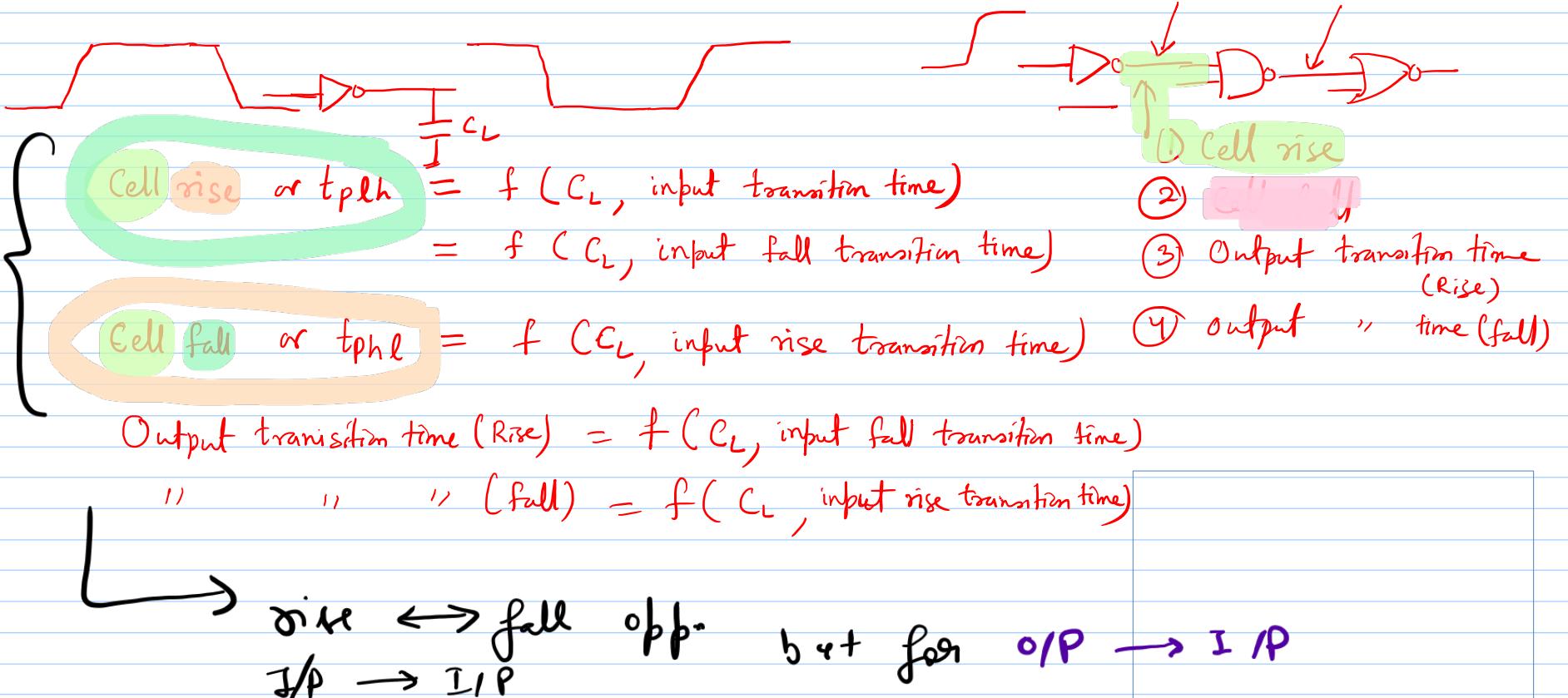
- The time taken by the signal to fall from 90% (80%) to 10% (20%) of its maximum value.



10 to 90%
20 to 80 %

② transition parameter
② for o/p

② transition parameters
③ for I/P

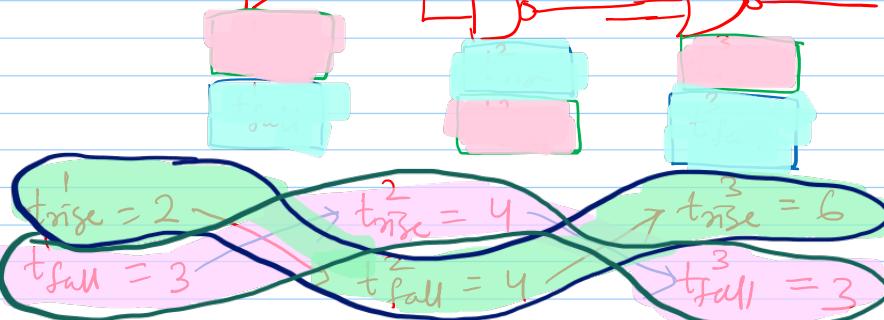
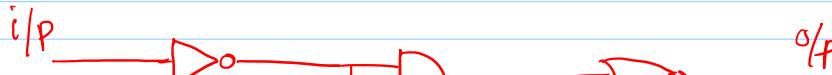


Cell {	(I/P) I/P	Rise \rightarrow I/P <u>fall</u> \rightarrow IIP	I/P IIP
O/P Transition Time	O/P O/P	Rise \rightarrow JIP fall \rightarrow IIP	JIP rise

Numerical S

Type 2: Prop. delay
Related

do a timing Path



$$T_{rise} = 2 + 4 + 6 = 12$$

$$T_{fall} = 3 + 4 + 3 = 10$$

Rise Path
is more
critical

$T_{rise} > T_{fall}$ what it means?
compared to fall path.

$$(t_{plh})_{Path} = t^1 + t^2_{fall} + t^3_{rise}$$
$$(t_{phl})_{Path} = t^1 + t^2_{rise} + t^3_{fall}$$

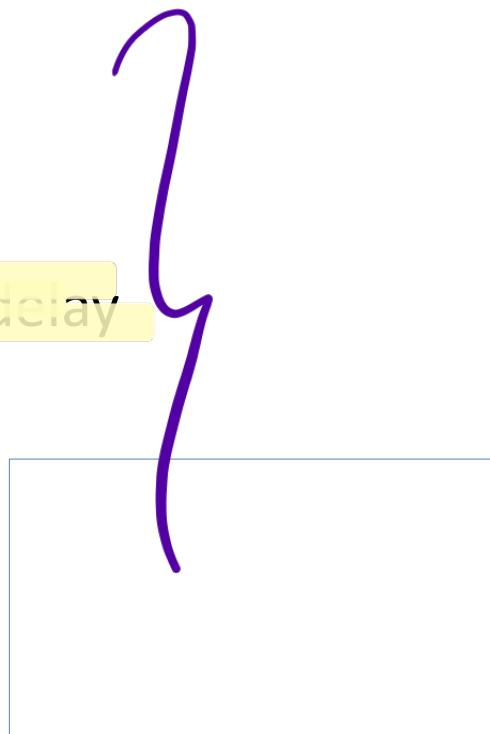
If odd no....

then same as LHS

If even no....
then ?
Opp.

Contents

- Sequential Circuits
- Delay Parameters of Sequential Circuits
 - (1) Setup time (2) Hold time and (3) Clock-to-Q delay
- Reason of Setup time in a Flip-flop
- Reason of Hold time in a Flip-flop



Sequential Circuits

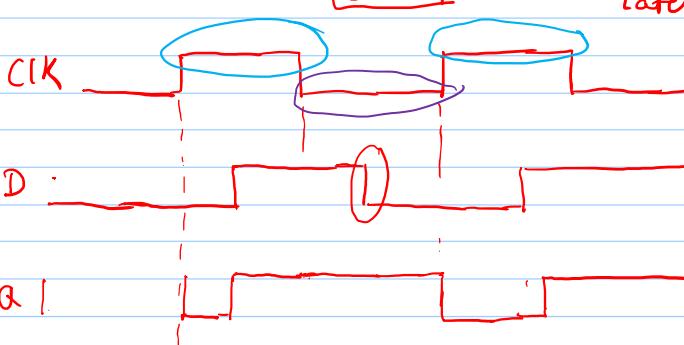
① Flip-Flop (FF)

(Edge-triggered)

F. F.



[Latch] Positive-transparent latch



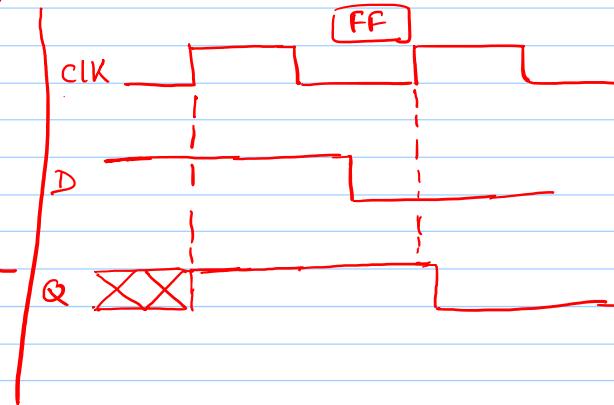
②

Latch

(Level triggered)



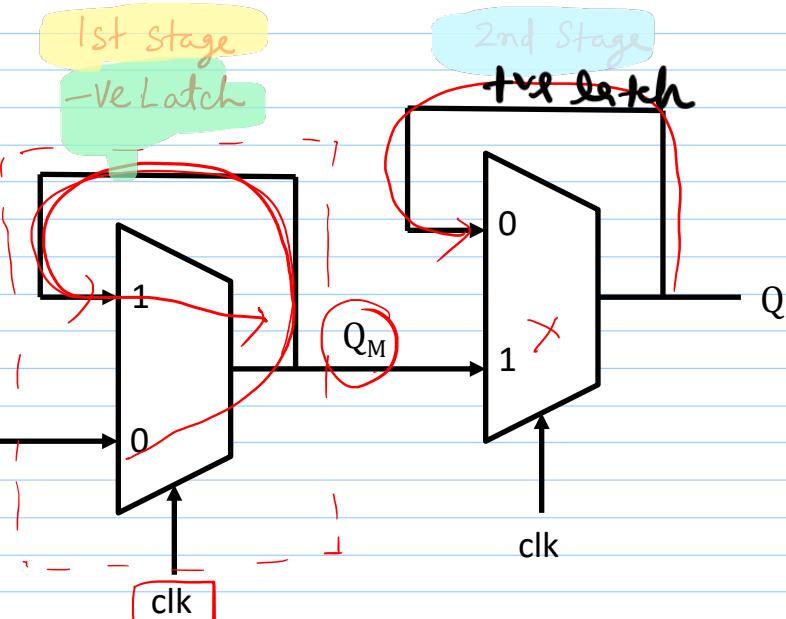
+ve edge-triggered FF



LATCH

- ve bcz
it is Sampling
@

$Clk = 0$
S
not $Clk = 1$



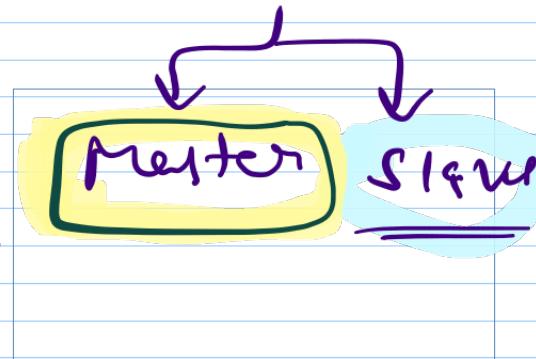
In 1st stage, $Clk = 0$; it samples the value 'D', Hence it is -ve latch.

In 2nd stage, $Clk = 1$, it samples the value in ' Q_M ', Hence it is +ve latch.

FF has two latches
① Master latch (1st stage)
② Slave latch (2nd stage)

FF is a +ve-edge triggered in this case.

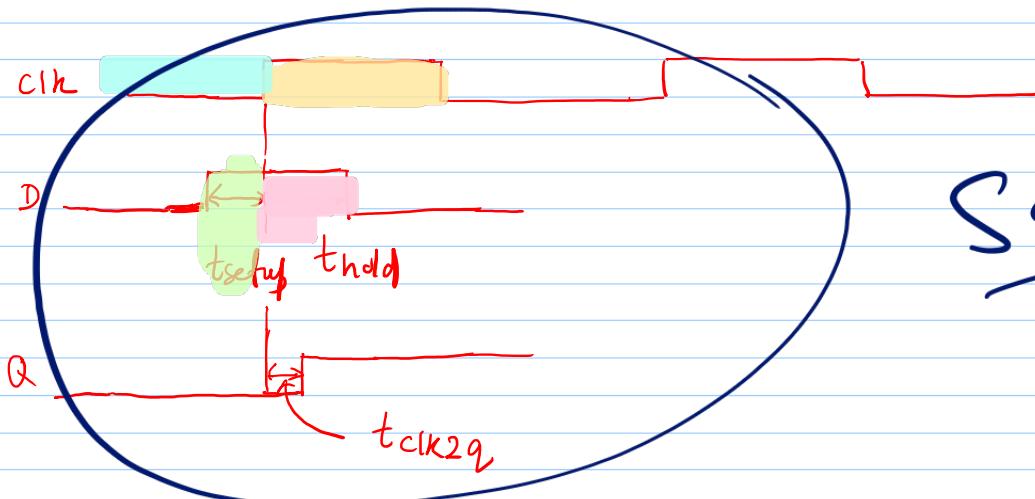
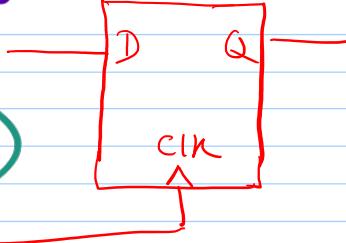
FF \rightarrow 2 latch



- ① Setup time (t_{setup})
- ② Hold time (t_{hold})
- ③ t_{clk2q} delay

Setup
Hold

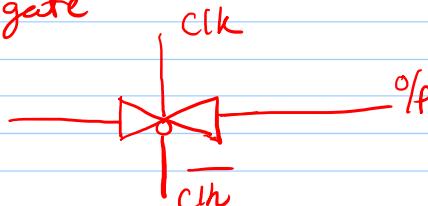
clk2q



~~Same as
Previous~~



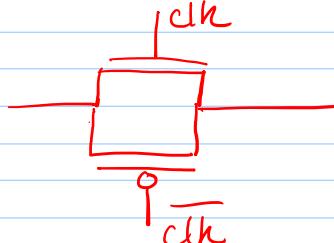
Transmission gate



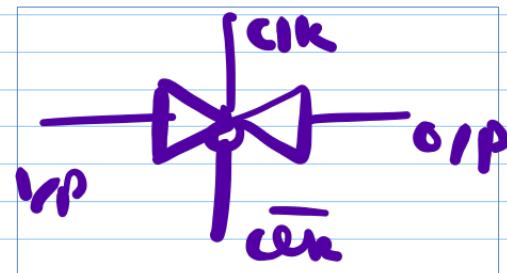
$$\text{clk} = 1 \text{ and } \overline{\text{clk}} = 0 \Rightarrow$$

$$\text{clk} = 0 \text{ and } \overline{\text{clk}} = 1 \Rightarrow 0_p$$

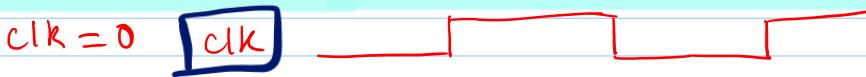
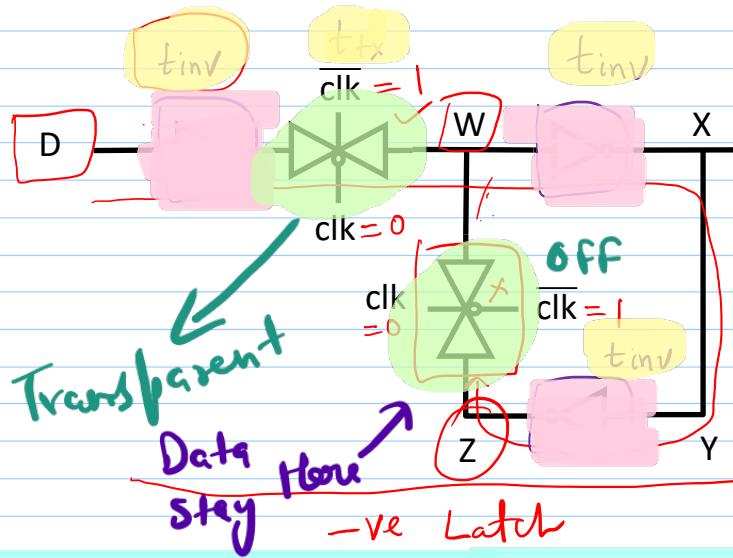
Transmission gate



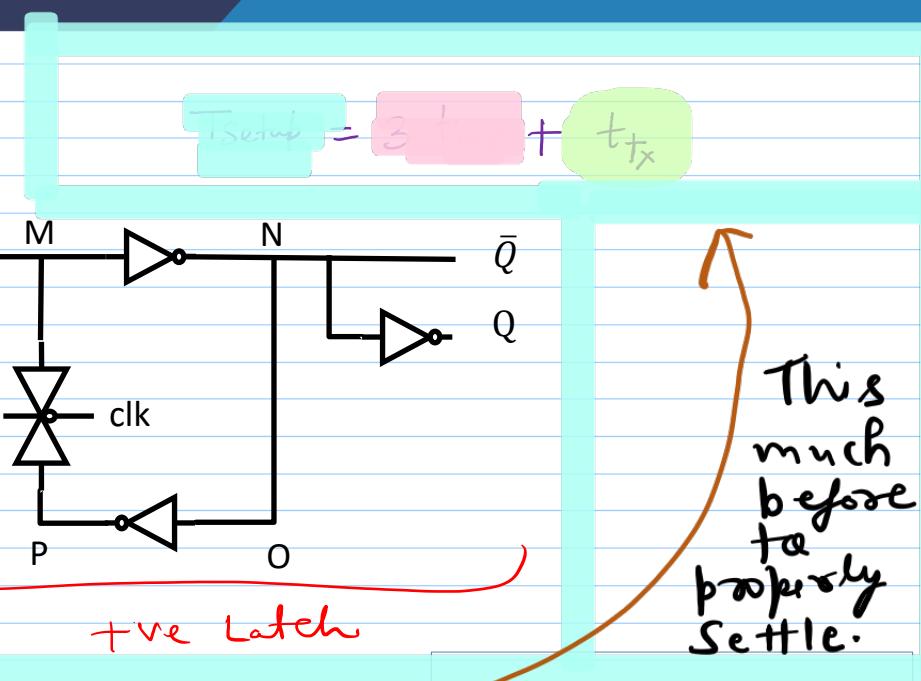
Why Schub time? ↗



Reason for Setup Time



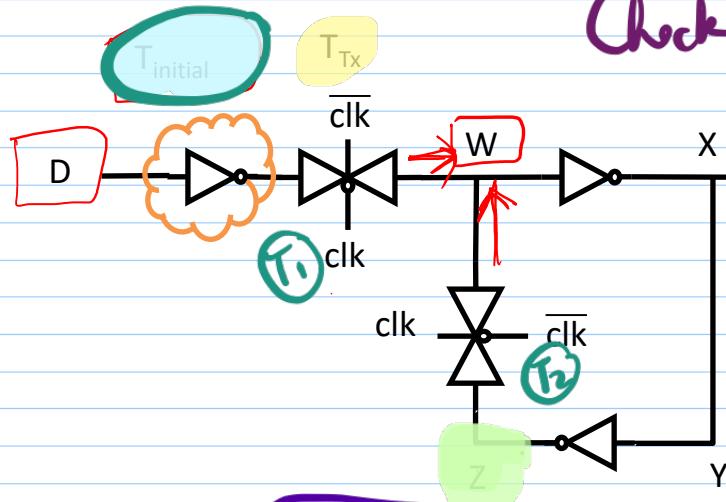
Data should come earlier than clock signal. How much before?



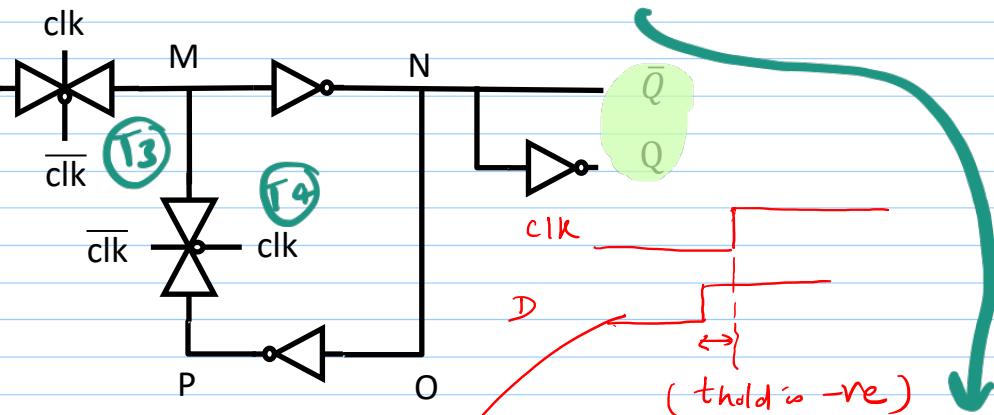
Why hold time?

This much before to properly settle.

Reason for Hold Time



Check $T_{initial}$ vs $T_{tx} \leq$

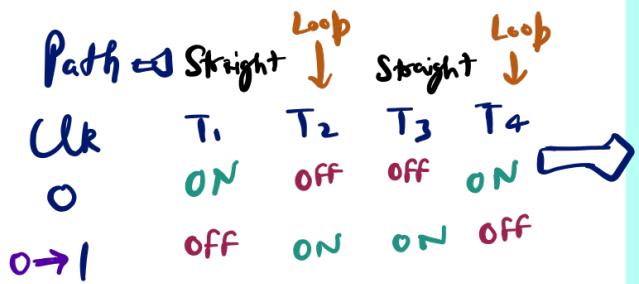


Case 1 : $T_{tx} > T_{initial} \rightarrow$ hold time +ve

Case 2 : $T_{tx} = T_{initial} \rightarrow$ hold time is 0

Case 3 : $T_{tx} < T_{initial} \rightarrow$ hold time is -ve

if equal No hold time



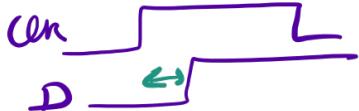
I want to sample data
 (Z) to output Q at the
 transition of $0 \rightarrow 1$.

(P₂)
 Path 2

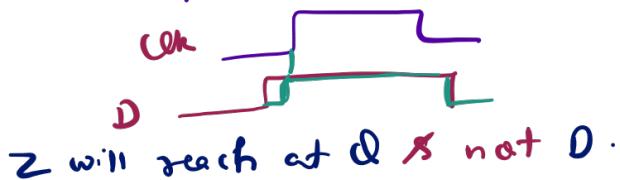
Path ①
 but the data (P₁)
 is directly going →
 from I/P to O/P.

That is HOLD VIOLATION.

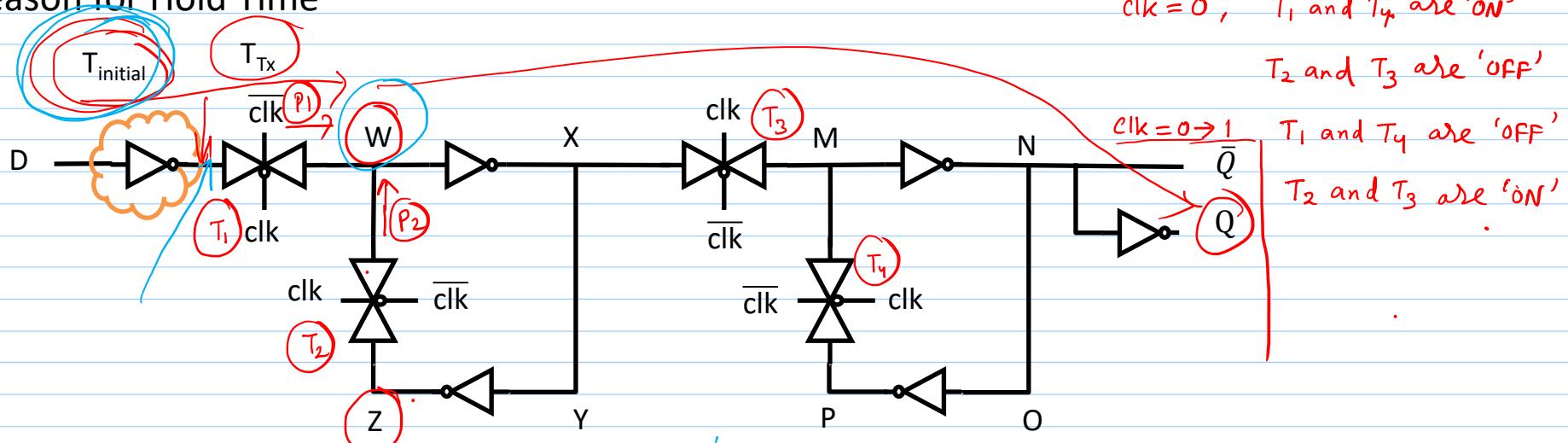
CASE ① $T_{Tx} > T_{initial}$
 hold time is +vl



CASE ② $T_{Tx} \leq T_{initial}$
 hold time = 0 & -vl



Reason for Hold Time



$\text{clk} = 0$, T_1 and T_4 are 'ON'

T_2 and T_3 are 'OFF'

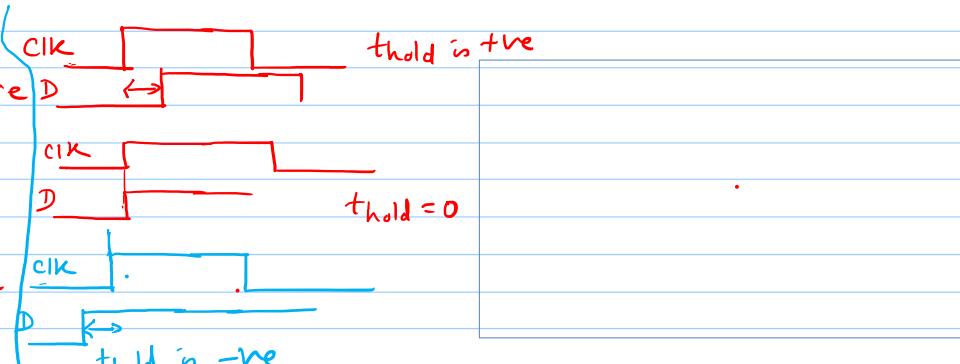
T_1 and T_4 are 'OFF'

T_2 and T_3 are 'ON'

Case 1: $T_{Tx} > T_{initial}$ \rightarrow hold time is +ve

Case 2: $T_{Tx} = T_{initial}$ \rightarrow hold time is 0

Case 3 $T_{Tx} < T_{initial}$ \rightarrow hold time is -ve



Contents

- Setup time and Hold time
- Maximum timing analysis (Setup check)
- Minimum timing analysis (Hold Check)
- Impact of Process corner on setup and hold Violation
- Solve the issues of setup and hold violation in a manufactured chip

FF delay Parameters

- ① $t_{\text{setup}} = \text{setup time}$
- ② $t_{\text{hold}} = \text{hold time}$
- ③ $t_{ccq} = t_{cq}^{\text{min}} = \text{Contamination delay betn clk and q (Min)}$
- ④ $t_{pcq} = t_{cq}^{\text{max}} = \text{propagation delay betn clk and q (Max)}$
- ⑤ $t_{cd} = t_{\text{comb}} = \text{contamination delay of the combinational circuit (Min)}$
- ⑥ $t_{pd} = t_{\text{comb}} = \text{propagation delay of the , , (Max.)}$

Imp.

⑤ t_{comb}
min

⑥ t_{comb}
max

① Setup
② Hold

③ c_q^{min} → Contamination

④ c_q^{max} → Propagation

t_{pd} - Logic Propagation Delay
 t_{cd} - Logic Contamination Delay

t_{comb}^{max}

t_{pq} - Latch/Flop Clock-to-Q Propagation Delay

t_{cq} - Latch/Flop Clock-to-Q Contamination Delay

t_{pdq} - Latch D-to-Q Propagation Delay

t_{setup} - Latch/Flop Setup Time

t_{hold} - Latch/Flop Hold Time

$t_{min.}$
 t_{comb}

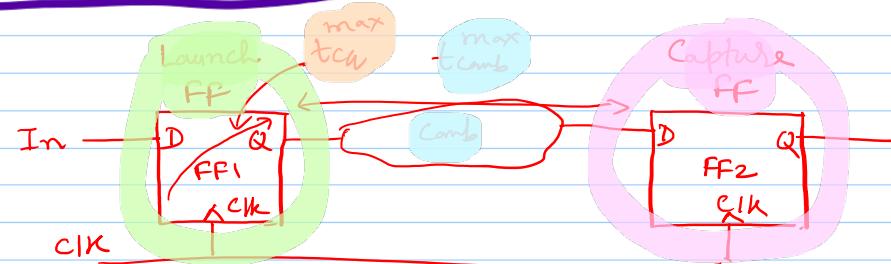
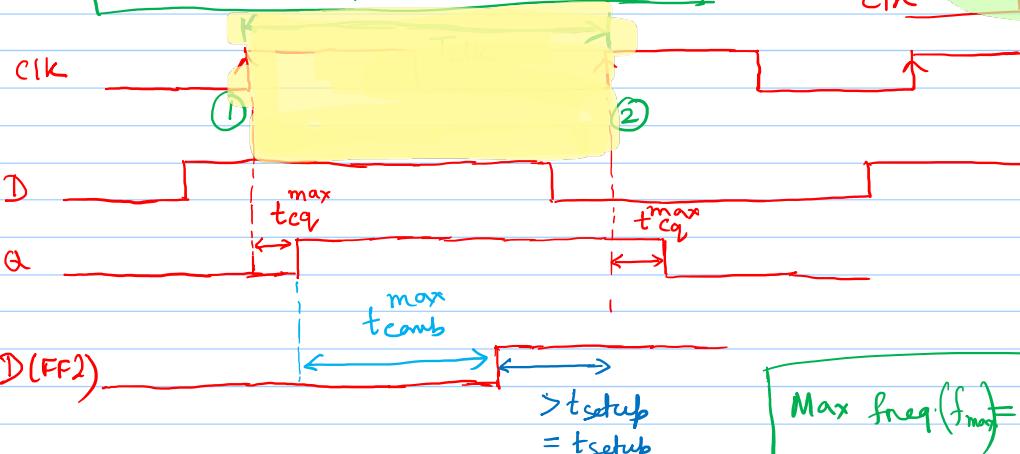
Max Timing Analysis

Max. Timing Analysis

① 1- FF — ① setup time ② hold time ③ clk2q delay

② 2- FFs — 2 FFs

$$\begin{aligned} t_{clk} &\geq t_{cq}^{\max} + t_{comb}^{\max} + t_{setup} \\ t_{clk} &\geq t_{pcq} + t_{pd} + t_{setup} \end{aligned}$$



① Manufactured chip has setup violation.
→ Slow down the clock speed

Summarized
Here ↴

$$\text{Max freq}(f_{\max}) = \frac{1}{T_{clk}}$$

Max. Analysis

$$T_{clk} \geq t_{cq}^{\max} + t_{comb}^{\max} + t_{setup}$$
$$\text{“} \geq t_{pre} + t_{pd} + t_{setup}$$

Setup violation

Slow down the process

Max.
Timing
Analysis

$\text{Max freq (fmax)} = \frac{1}{T_{clk}}$

- ① NMOS - (S, T, F)
② PMOS → (S, T, F)

Types of corners are ① SS (slow slow) ② TT ③ FF ④ FS ⑤ SF

- ③ Temperature
④ voltage

Max timing analysis → SS corner

Setup Check

Types of Corners

SS (slow slow)

FF

FS

SF

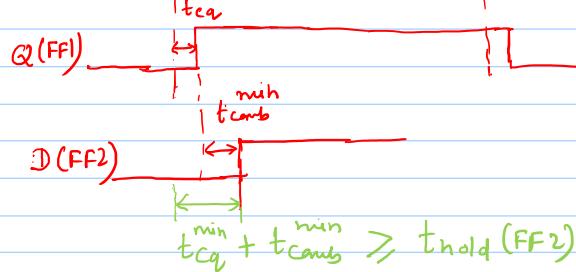
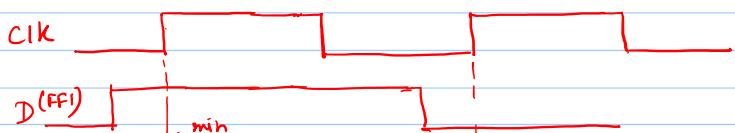
ST^T

Minimum Timing Analysis (Hold check)

① Hold time

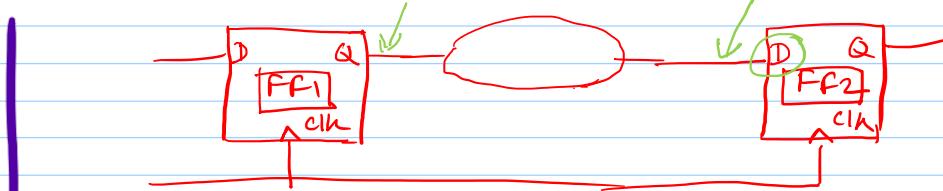
$$② t_{cq} = t_{cq}^{\min}$$

$$③ t_{cd} = t_{\text{Comb}}^{\min}$$



① Setup time check \rightarrow 2 clock edges

② Hold time check \rightarrow 1 clock edges



③ Hold check

ff corner

④ Fixing hold violation -

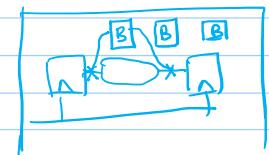
Increase the delay of combinational path

Buffer insertion

group.

Solution

⑤ Manufactured chip has hold validation

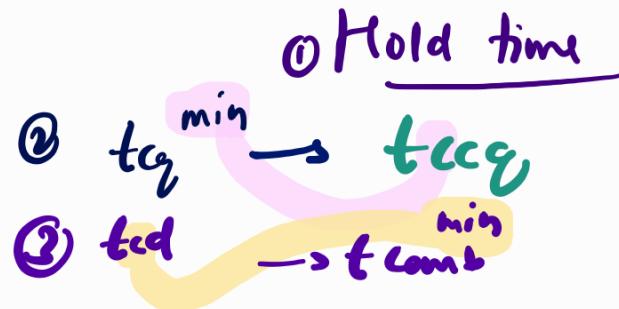


Clock edges

Setup time check \Rightarrow 2

Hold time check \Rightarrow 1

Min. Timing Analysis



Setup time check \rightarrow 2 clock edges
Hold time check \rightarrow 1 " "

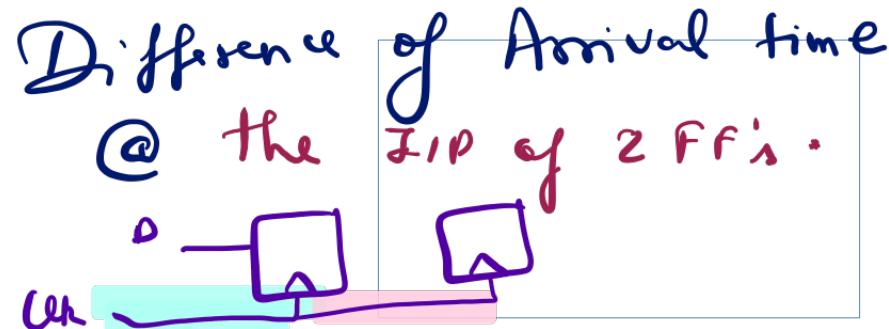
$$t_{CQ}^{\min} + t_{COMB}^{\min} \geq t_{hold}$$

Contents

- What is clock skew?
- Types : Positive Skew and Negative Skew
- Max. timing constraint (Setup check) with Clock Skew
- Min. timing constraint (Hold Check) with Clock Skew

Clock Skew

:



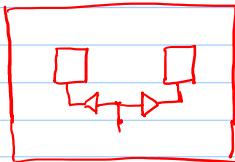
What is Clock Skew?

- ① The difference in arrival time of the clock signal at the inputs of two consecutive FFs in a design → clock skew

- ② Reasons of clock skew

Reasons

- ③ The clock skew occurs due to spatial variation:



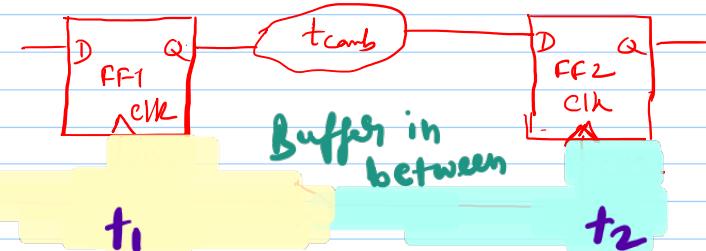
Space

- ④ The clk skew → static variation in the path length.

- ⑤ The clock skew does not change the clock period but

it will shift the phase of the clock.

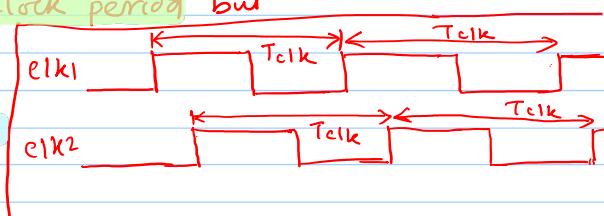
- ⑥ Skew is constant from cycle to cycle



$$\text{clock skew} = (t_2 - t_1)$$

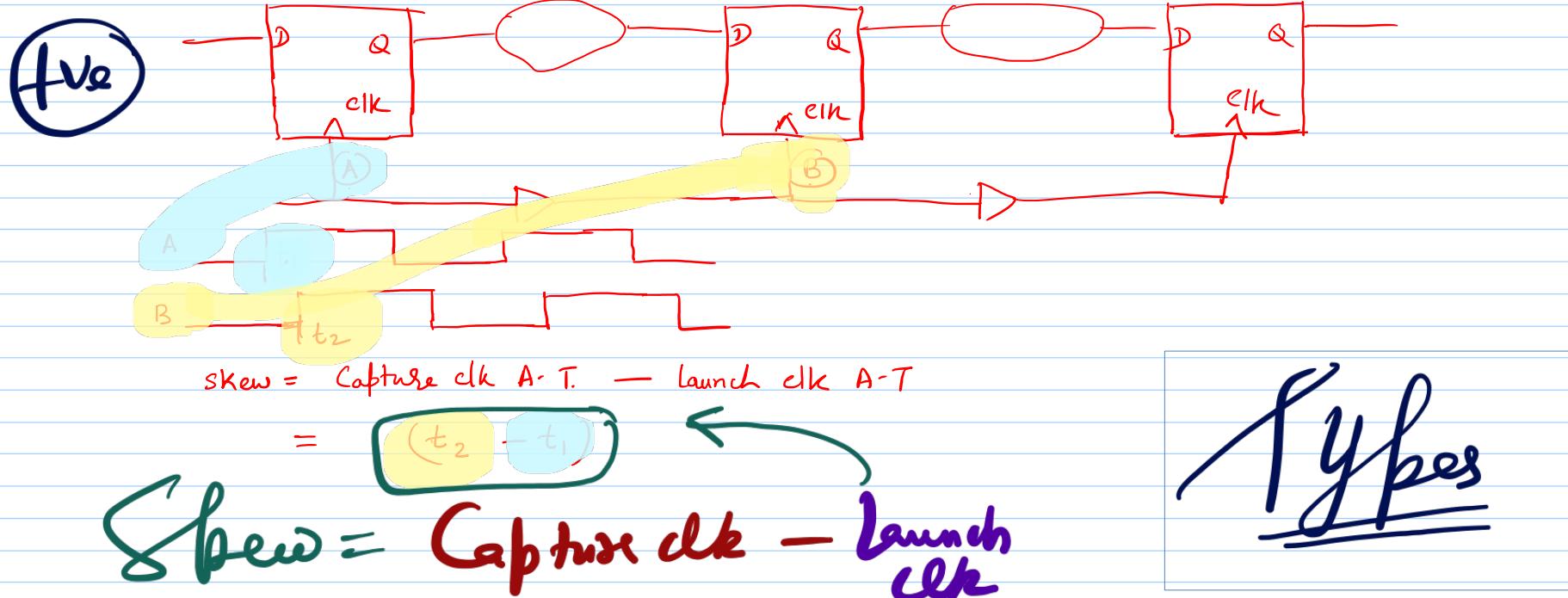
= (Capture clock A-T - launch clock A-T)

It will only
Shift the
phase of
the clock.



Types of Clock skew :

① Positive Skew : The clock and data signals are moving in same direction

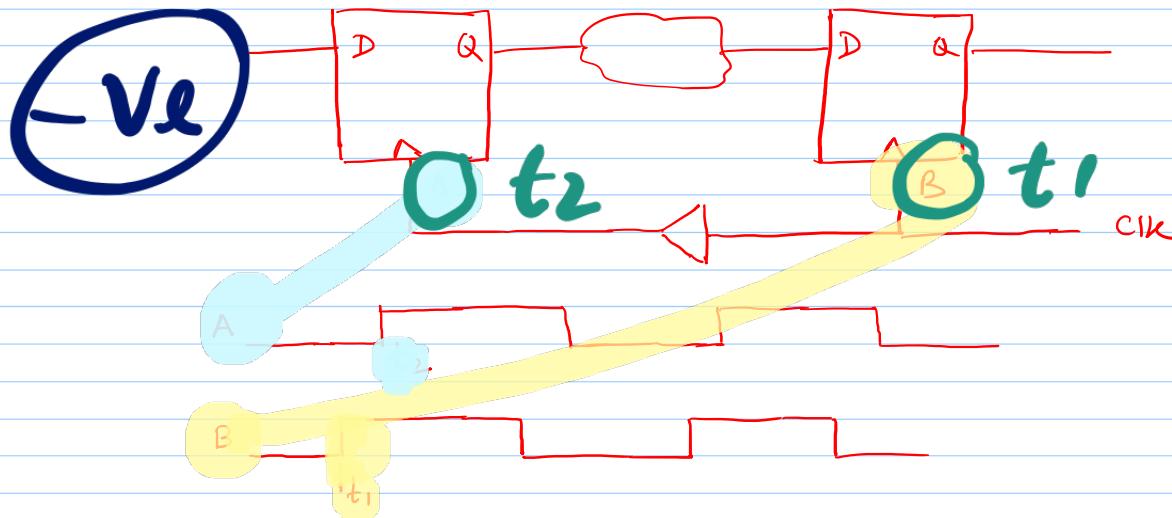


Types

② Negative Skew:

Data and Clock signal

" $t_1 - t_2$ " direction.

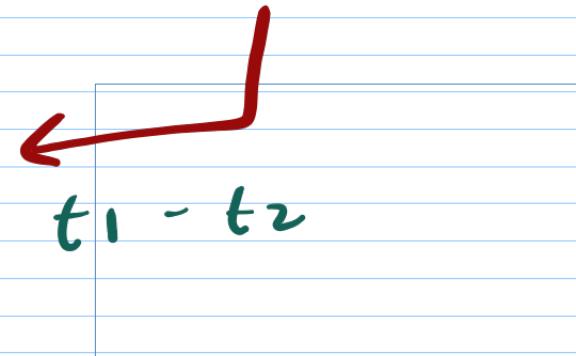


$$\text{Skew} = \text{Capture clk A.T.} - \text{Launch clk A.T.}$$

$$= (t_1 - t_2)$$

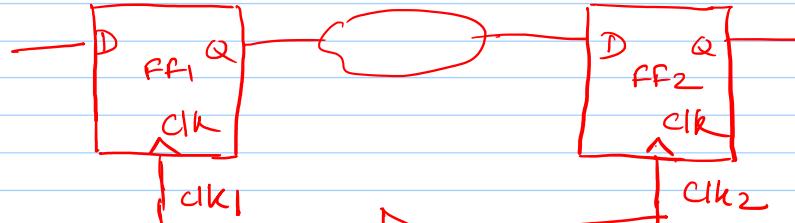
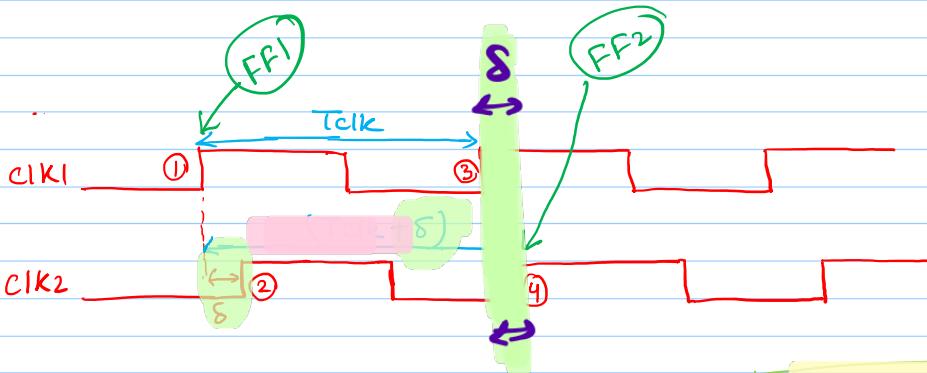
Skew is $-ve$

Data & clock sig
are moving in
Opposite
dirac^n



Max. Timing analysis considering skew (δ is +ve)

Max Analysis with ~~free~~ Skew



Case I (without skew): $t_{cq}^{\max} + t_{comb}^{\max} + t_{setup} \leq T_{clk}$

Case II (with skew):

$$t_{cq}^{\max} + t_{comb}^{\max} + t_{setup} \leq (T_{clk} - \delta)$$

FF1 samples the data at edge 1

Positive skew improves the speed of the design

FF2 samples the data at edge ④

Tclk ①

Tclk ↓ \Rightarrow $t_{clk} \uparrow$

$$t_{cq}^{\max} + t_{comb}^{\max} + t_{setup} - \delta \leq T_{clk}$$

Tclk ↘
सीट ④ डॉड
ट्रैक

Minimum timing Analysis Consider +ve skew

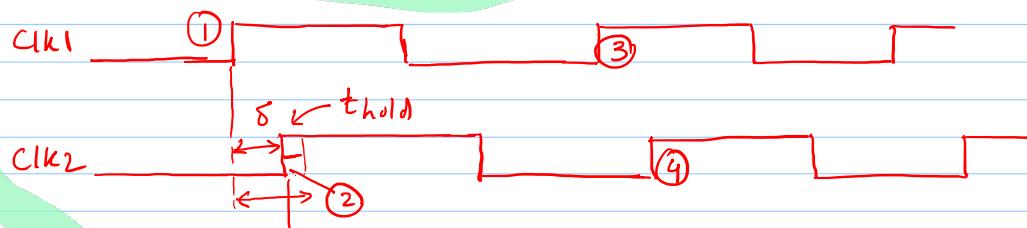
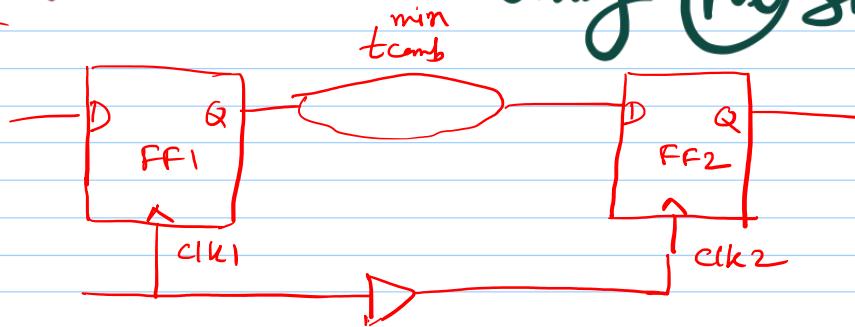
MIN ANALYSIS Using +ve skew

① Case I (without clock skew)

The hold time is t_{hold}

$$t_{hold} \leq t_{cq}^{\min} + t_{comb}^{\min}$$

② Case II (with clock skew)



The hold time of the FF2 is $(t_{hold} + \delta)$

$$(t_{hold} + \delta) \leq t_{cq}^{\min} + t_{comb}^{\min}$$

hold check \Rightarrow clk1 - ①
clk2 - ②

But it

+ve skew
degrades
the hold requirement

$t_{hold} \neq$
2TTSR8
 $\text{clock } \neq \text{ at } 1$

+ve SKEW

It improves the speed of design

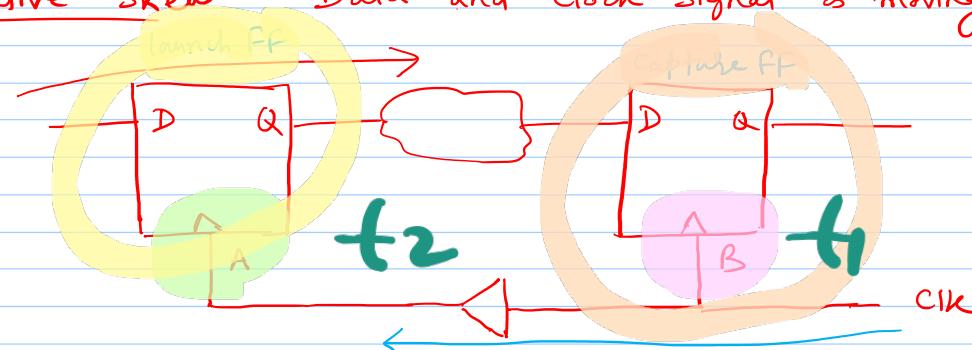
but it degrades
hold requirement.

Contents

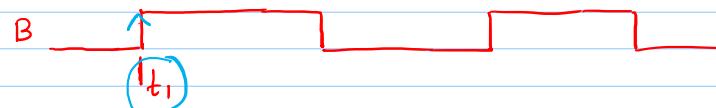
- What is negative clock skew?
- Max. timing constraint (Setup check) with negative Clock Skew
- Min. timing constraint (Hold Check) with negative Clock Skew
- Some examples

Negative Skew

② Negative Skew: Data and clock signal is moving in "opposite" direction.



$$t_1 - t_2 = -v_d$$



Skew = Capture clk A.T. - Launch clk A.T.

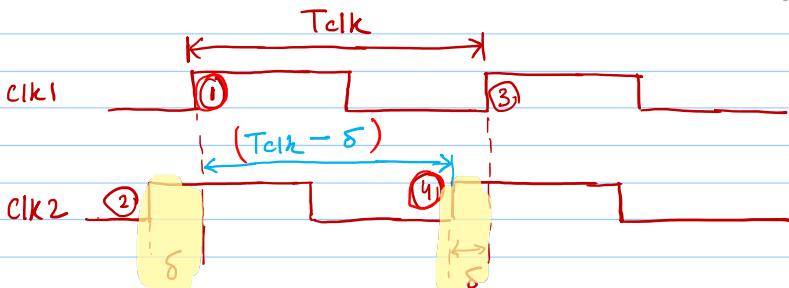
$$= (t_1 - t_2)$$

Skew is -ve

Capture-Launch
= 2nd - 1st

Max timing Analysis considering -ve skew

- ① FF1 will sample at edge ①
- ② FF2 will sample at edge ④



Case I (without clock skew) : $t_{clk2q}^{\max} + t_{comb}^{\max} + t_{setup} \leq T_{clk}$

Case II (with clock skew) : $t_{clk2q}^{\max} + t_{comb}^{\max} + t_{setup} \leq (T_{clk} - \delta)$

on - ve
skew *



$\Rightarrow f_{clk} \downarrow$

Max speed of clock will decrease.

Max ANALYSIS USING



-Ve Skew

↓
Opt. of
+ve

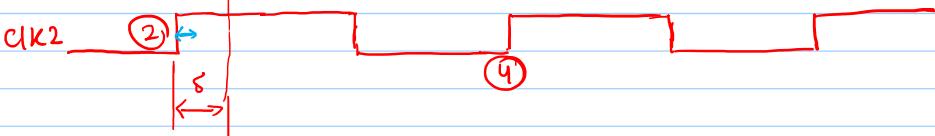
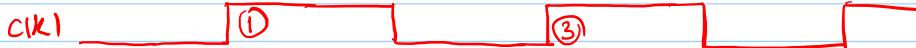
→ Subtract from
Tclk

Min. timing Analysis considering -ve skew (Hold check)

We are checking edge ① and ②

-ve
with skew,
 $\delta < 0$

$t_{hold} \rightarrow (t_{hold} - \delta)$



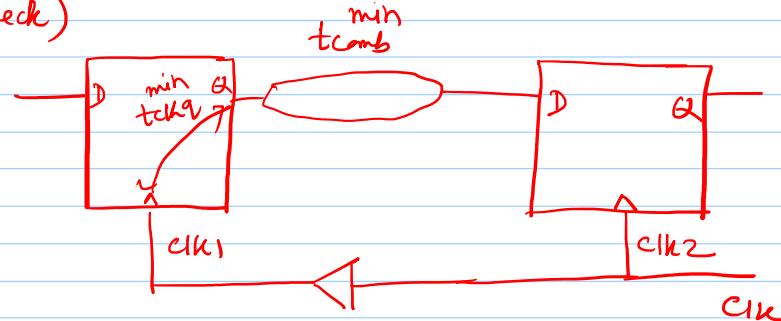
① Case I (without ^{-ve} clock skew) :

$$t_{hold} \leq t_{clk2}^{\min} + t_{comb}^{\min}$$

② Case II (with ^{-ve} clock skew) :

$$(t_{hold} - \delta) \leq t_{clk2}^{\min} + t_{comb}^{\min}$$

$$t_{hold} \leq t_{clk2}^{\min} + t_{comb}^{\min} + \delta$$



M/N Analysis
with **clock skew**
Subtract from
 t_{hold}

#

Numericals

for Max. freq. of operation

→ do Max. timing Analysis
(Setup Check)

⑨ → w/o clock skew

Ex

$$t_{\text{setup}} = 2 \text{ ns}$$

$$t_{\text{hold}} = 1 \text{ ns}$$

$$t_{\text{clk2q}}^{\text{max}} = 10 \text{ ns}$$

$$\begin{aligned} t_{\text{combi}} &= 5 \text{ ns (max)} \\ &= 2 \text{ ns (min)} \end{aligned}$$

$$\begin{aligned} t_{\text{combi}} &= 6 \text{ ns (max)} \\ &= 1 \text{ ns (min)} \end{aligned}$$

Find the max. frequency of operation.

Ans!

Case I: Path betⁿ FF1 and FF2

Path
bw

Using

$$T_{\text{clk}} \geq t_{\text{clk2q}}^{\text{max}} + t_{\text{combi}}^{\text{max}} + t_{\text{setup}}(\text{FF2})$$

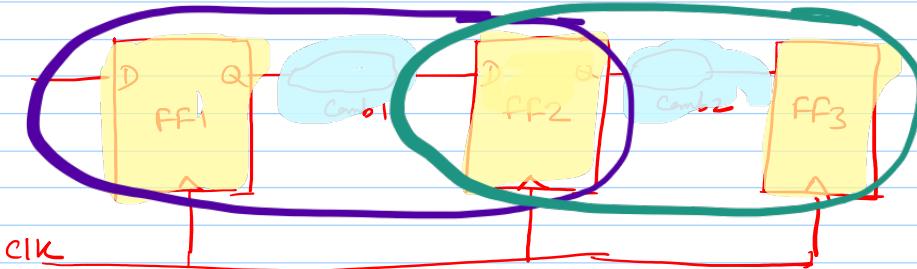
$$\geq 10 \text{ ns} + 5 \text{ ns} + 2 \text{ ns}$$

$$T_{\text{clk}} \geq 17 \text{ ns}$$

Case II: Path betⁿ FF2 and FF3

$$T_{\text{clk}} \geq 10 \text{ ns} + 6 \text{ ns} + t_{\text{combi}}^{\text{(max)}}$$

$$T_{\text{clk}} \geq 18 \text{ ns}$$



$$= 18 \text{ ns}$$

$$f_{\text{clk}} = \frac{1}{T_{\text{clk}}} = \frac{1}{18 \text{ ns}} = 55.56 \text{ MHz}$$

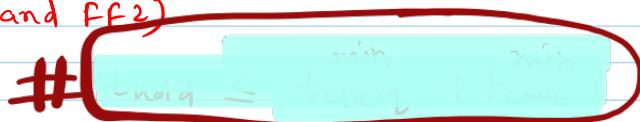
$$f_{\text{clk}} = 55.56 \text{ MHz}$$



for Hold
Check

Min. Timing analysis in the circuit. (Hold check)

Case I (FF1 and FF2)



$$1\text{ns} \leq 10\text{ns} + 2\text{ns}$$

$$1\text{ns} \leq 12\text{ns}$$

No hold violation.

Case II (FF2 and FF3)

$$t_{hold} \leq \underset{\text{min}}{t_{clk2q}} + \underset{\text{min}}{t_{comb}}$$

$$1\text{ns} \leq 10\text{ns} + 1\text{ns}$$

$$\boxed{1\text{ns} \leq 11\text{ns}}$$

No hold violation.

HOLD VIOLATION

Assume: $\underset{\text{min}}{t_{clk2q}} = 0.5\text{ns}$ and $\underset{\text{min}}{t_{comb}} = 0.2\text{ns}$
 $t_{hold} = 1\text{ns}$

$$t_{hold} \leq \underset{\text{min}}{t_{clk2q}} + \underset{\text{min}}{t_{comb}}$$

$$1\text{ns} \leq 0.5\text{ns} + 0.2\text{ns}$$

$$\boxed{1\text{ns} \leq 0.7\text{ns}}$$

X

hold violation.

MIN ANALYSIS

W/O Clock skew

Ex-2

- (i) Max freq. of operation
- (ii) hold check

① MAX

Case I (FF1 and FF2)

$$(T_{Clk1}) \geq t_{clkq} + t_{(max)}^{(max)} + t_{combi} + t_{setup}$$

$$\geq 10\text{ns} + 5\text{ns} + 2\text{ns}$$

$$T_{Clk1} \geq 17.5 = 16.5\text{ns} \Rightarrow T_{Clk1} = 16.5\text{ns}$$

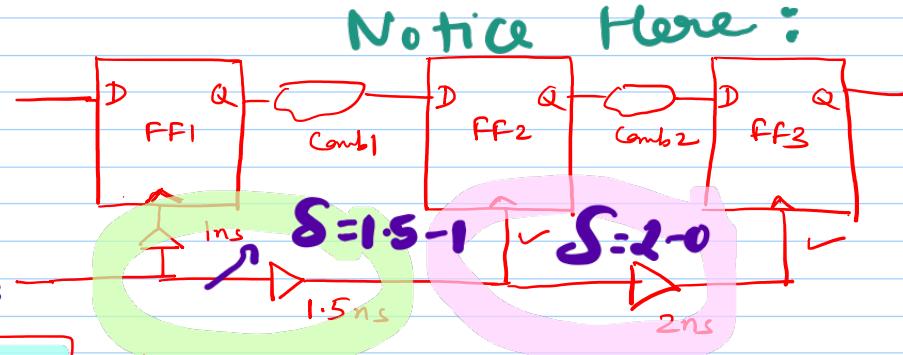
Case II (FF2 and FF3)

$$\delta = 2\text{ns}$$

$$T_{Clk2} = 18\text{ns} \quad (\text{without clock skew})$$

$$\begin{aligned} T_{Clk2} &= 18\text{ns} \\ T_{Clk2} &= 16\text{ns} \end{aligned} \quad (\text{with clock skew})$$

With
Clock
Skew



$$T_{Clk} = \max(T_{Clk1}, T_{Clk2}) = \max(16.5\text{ns}, 18\text{ns}) = 18\text{ns}$$

$$f_{clk} = \frac{1}{18\text{ns}} = 55.56\text{MHz}$$

① with +ve skew,
Speed of
clock →

21G 22G

Hold Check

② $\text{MIN} = \text{HOLD}$ CHECK

Case I (betn FF1 and FF2) \Rightarrow $t_{hold} \leq 5\text{ns}$

$$t_{hold} \leq t_{clk2q}^{\min} + t_{cmb}^{\min}$$

$$1\text{ns} + ? \leq 10\text{ns} + 2\text{ns}$$

$$1.5\text{ns} \leq 12\text{ns}$$

(No hold violation)

Case II (betn FF2 and FF3) \Rightarrow $t_{hold} \leq 2\text{ns}$

$$t_{hold} + ? \leq t_{clk2q}^{\min} + t_{cmb2}^{\min}$$

$$1\text{ns} + ? \leq 10\text{ns} + 1\text{ns}$$

$$3\text{ns} \leq 11\text{ns}$$

(No hold violation)

Assume!

$$t_{clk2q}^{\min} = 0.5\text{ns} \text{ and } t_{cmb}^{\min} = 0.5\text{ns}$$

$$t_{hold} \leq 1\text{ns} \text{ and } ?$$

$$\Rightarrow t_{hold} + ? \leq t_{clk2q}^{\min} + t_{cmb}^{\min}$$

$$\Rightarrow 1\text{ns} + ? \leq 0.5\text{ns} + 0.5\text{ns}$$

$$\Rightarrow 1.5\text{ns} \leq 1\text{ns}$$

(Hold violation)

If +ve Skew is there then add S with Tck for Max. clock S with Thold for Min. clock

How to find S

If directⁿ of D is opp. of directⁿ of clock signal then -ve skew.

