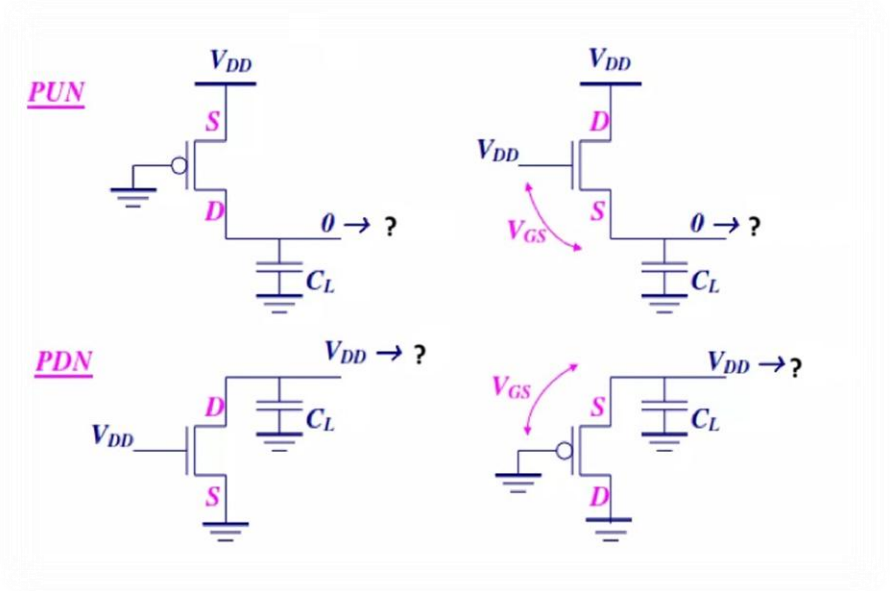
EE535L Digital VLSI Design
Model Question Paper

Question 1. Implement the following Boolean function using CMOS Logic:

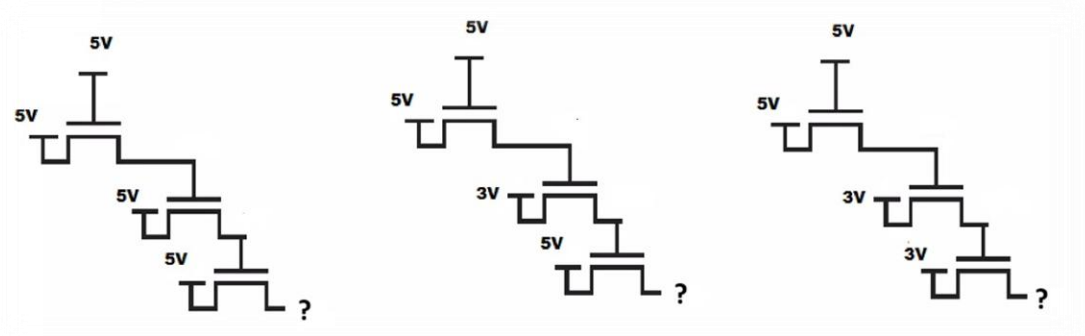
$\overline{A + (B + D)CE}$.

Question 2. Write Proper Analysis for all 4 Cases.



Question 3. Provide the value of Voltage at the output.

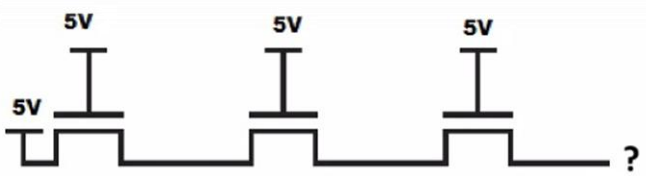
(a) (b) (c)



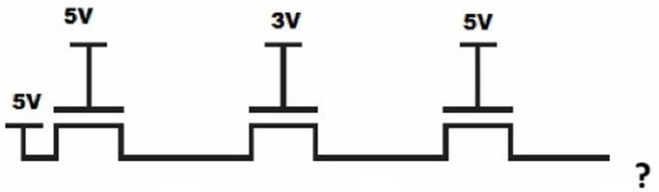
Question 4. All are identical NMOS. Write Values of in-between Voltages also after each NMOS.

Also Give a thought assuming them PMOS and 0 V being supplied for their gate to get them ON. And all other V_{dd} replaced by ground.

(a)



(b)



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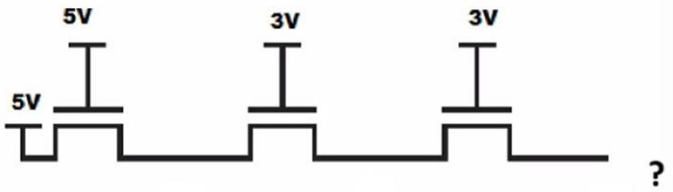

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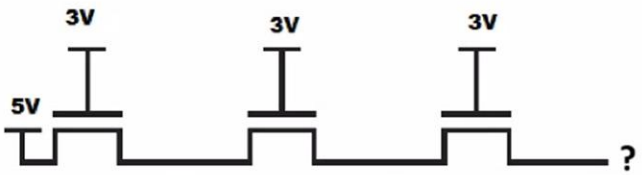

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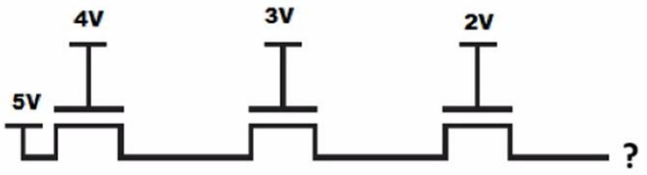
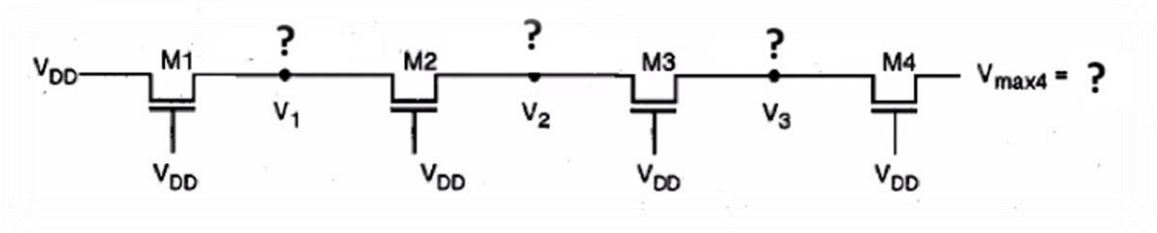


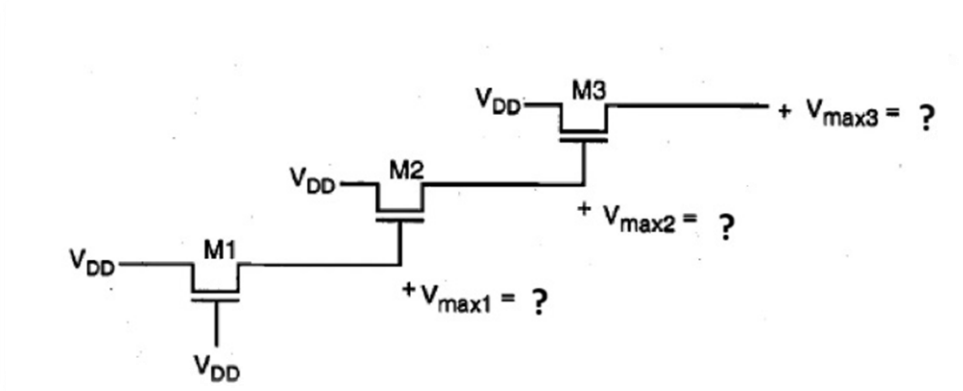
Question 5. Consider once all Vth_n to be

(a) same and

(b) different.



Question 6. Provide the values for V_{max1} , V_{max2} , V_{max3} . Assuming Different V_{thn} .



Question 7. Draw the equivalent CMOS Inverter for A(B+E)+CD, by assuming that all the transistors have equal W/L ratios and write the equivalent W/L values of PMOS and NMOS transistors of CMOS Inverter.

Question 8. Why Pass-transistors require lower switching energy to charge up a node?

Question 9. Draw the circuit diagram for f(a, b, c) = $ab + \overline{cd} + def$ using

a) pass-transistor logic

b) transmission gate logic.

Question 10. Draw the equivalent CMOS Inverter for A(C D)+BE , by assuming that all the transistors have equal W/L ratios and write the equivalent W/L values of PMOS and NMOS transistors of CMOS Inverter.

Question 11. Derive the switching threshold voltage of generic CMOS N-input NAND gate and calculate High- and Low-level Noise Margin for 2 input NAND gate only.

Question 12. A NOR CMOS gate with the device/parasitic parameters below must drive (output to) the inputs of 3 NAND gates (one input on each gate) with the same MOSFET gate dimensions as the NOR gate

The parameters as follows

$$VDD = 2.0V \quad C_{ox} = \frac{2fF}{\mu m^2} \quad C_{DBp} = 1fF \quad C_{DBn} = 0.5fF$$

$$\left(\frac{W}{L}\right)_p = \frac{4}{0.5} \quad k_p^{'} = 100\frac{\mu A}{V^2}3 \quad |Vtp| = 0.5V$$

$$\left(\frac{W}{L}\right)_n = \frac{2}{0.5} \quad k_n^{'} = 250\frac{\mu A}{V^2}3 \quad Vtn = 0.6V$$

1) What is the total parasitic capacitance at the output of the NOR gate?
2) What is the total load capacitance contributed by the 3 NAND gates?
3) What is the total capacitance at the output of the NOR gate?
4) What is the effective resistance between the output and VDD when the NOR gate pulls the output high? Use the "general" formula for channel resistance.
5) Combining results from (3) and (4), what is the output RC time constant?

Question 13. Write the drain current equation of the P-channel MOSFET?

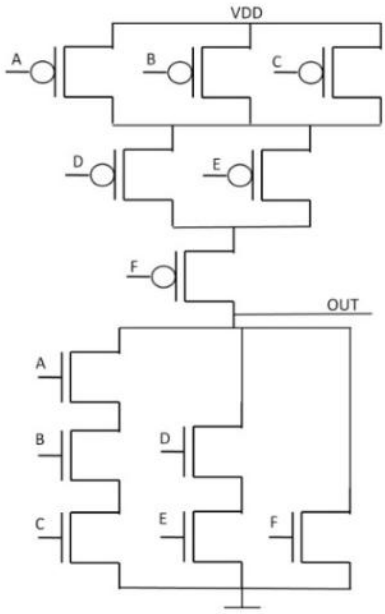
Question 14. Assume that an inverter drives a load capacitance of 0.2 ff and the supply voltage is 1V. Further assume that the inverter makes 1 X 10^9 ZERO-to-ONE transitions in 1 second and 1 X 10^9 ONE-to-ZERO transitions in 1 second. What is the power dissipated in charging and discharging the load capacitance?

Question 15. Consider the static CMOS gate shown below. Assuming that gn/gp = 1.5 and $V_{thn} = |v_{thp}|$. As consequence, a reference, balanced inverter for this technology has an NMOS width W_n = 1 unit and a PMOS width W_p = 1.5 units.

(a) What Boolean function does this gate implement?

b) Size the transistors in this gate so that the worst-case on resistance for the pull-up and pull-down networks are the same as that for the static CMOS inverter.

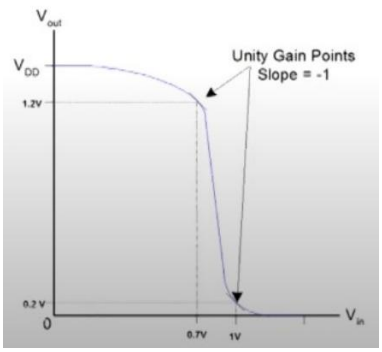
c) Size the transistors in this gate so that the best-case on resistance for the pull-up and pull-down networks are the same as that for the static CMOS inverter.



Question 16. A CMOS inverter with minimum sized transistors has β_n = 0.2mA/V2, β_p = 0.1mA/V2 and $V_{tn} = |V_{tp}|$=0.6V. Assume V_{DD} = 3.3V.

1) What is the inverter switching threshold (midpoint) voltage VM?
2) What is the resistance of each transistor using our general expression for MOSFET resistance in saturation?
3) What are the rise and fall times of this circuit if the parasitic capacitance at the output is 9fF?
4) If a load capacitance, CL = 25fF is added to the output, what are the new rise and fall times?
5) What are the propagation delays for this circuit considering both parasitic and load capacitances?

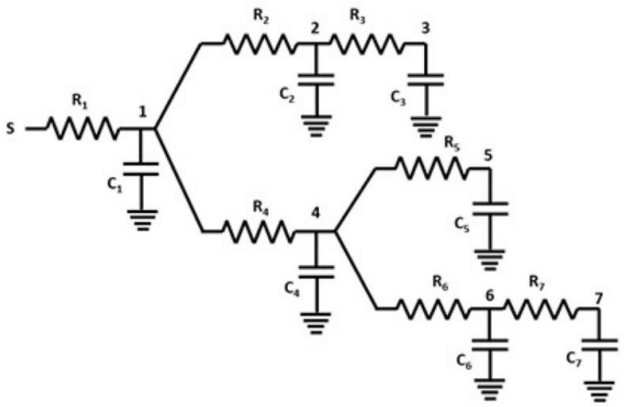
Question 17. Compute low and high noise margins for the inverter with the following VTC.



Question 18. (a) What are the rise time, fall time, and average propagation delay for a symmetrical CMOS inverter with $(WIL)_P$ = 5/1, $(W/L)_N$ = 2/1,V_{DD}= 2.5 V, and C = 0.20 pF?
(b) Repeat for V_{DD} = 2.0 V.
(c) Repeat for V_{DD} = 1.8N.

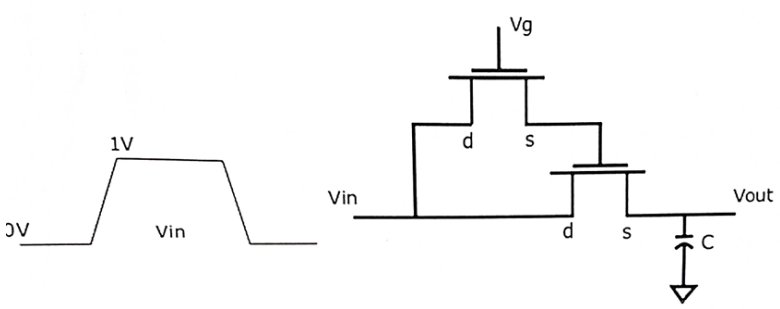
Question 19. Find the dynamic power dissipation of a CMOS inverter operated from a 1.8-V supply and having a load capacitance of 100 fF. Let the inverter be switched at 100 MHz.

Question 20. Consider the following Circuit.



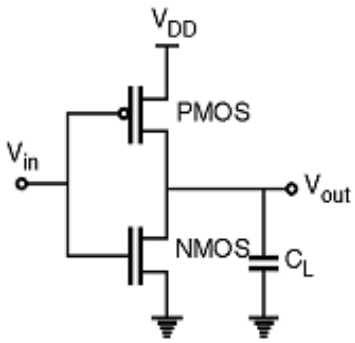
(a) What is the shared path Resistance, R_{75} ?
(b) Consider the circuit given above. The values of resistors and capacitors are Ri = i KΩ and Ci = i+1 pF.
Using the Elmore delay model, Calculate the delay from the source node to node 7 (in ns).

Question 21. Draw the output of the following circuits shown in Figure. The input V_{in} is square wave, V_g is 1 V and C is 10pF, the threshold hold voltage of the NMOS and PMOS are 0.2 V. Draw V_{out} only, no need to write the calculations.



Question 21. Consider a CMOS inverter that is designed in a process with the following parameters:
k'_n=100 $\mu A/V^2$, k'_p = 40 $\mu A/V^2$, $V_{T0N=}$ +0.7V and $V_{T0P=}$ -0.8V.
The transistors have aspect ratios of and $(W/L)_P$ =15, $(W/L)_N$ =10, and the power supply is chosen to be 5V.
(a) Calculate the value of the inverter midpoint voltage V_M=V_I.
(b) Calculate the values of V_{IL} and V_{IH}, and then find the voltage noise margins.

Question 22. Draw all Capacitances around an Inverter Circuit.



Question 23. Explain & Solve the probability for switching logic for:
(a) NAND Gate
(b) NOR Gate
(c) Full Adder

Question 24. Provide the expression for :
(a) High to Low time of the inverter
(b) Low to High time of the inverter
(c) Inverter switching maximum frequency

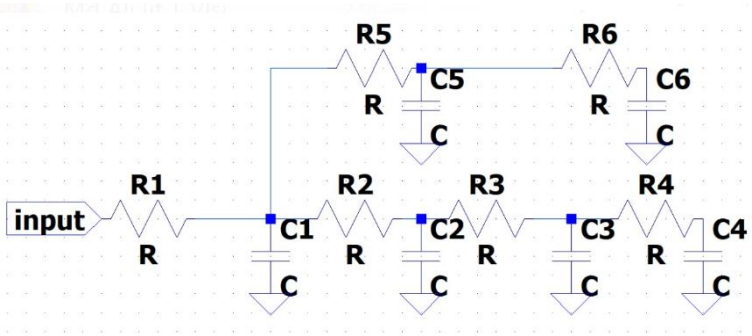
Question 25. Consider 16 cascaded minimum-sized transmission gates, each with an average resistance of 8 kΩ. The node capacitance consists of the capacitance of two NMOS and PMOS devices (junction and gate). Since the gate inputs are assumed to be fixed, there is no Miller multiplication. The capacitance can be calculated to be approximately 3.6fF for the low-to-high transition.

Question 26. Provide Relation between Tapering factor and Delay, Area. Draw the rough plot for Tapering Factor (f) and plot the optimized point.

Question 27. Explain and derive the necessary DC region equations of a CMOS inverter?

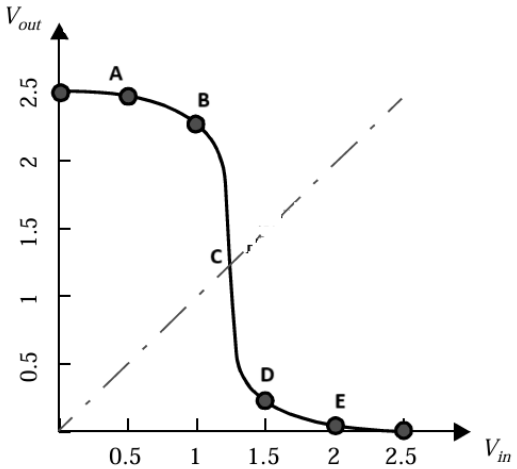
Question 28. (a) Realize 3 Input NAND gate by Pseudo NMOS Logic and perform its functional verification by using functional verification table.
(b) Develop a 2 X 1 Multiplexer using Transmission gates and interpret its operation using different input combinations.
(c) Develop a Full Adder using minimum number of 2 X 1 Multiplexer.

Question 29. Write the final equation for Propagation delay at node C_6.



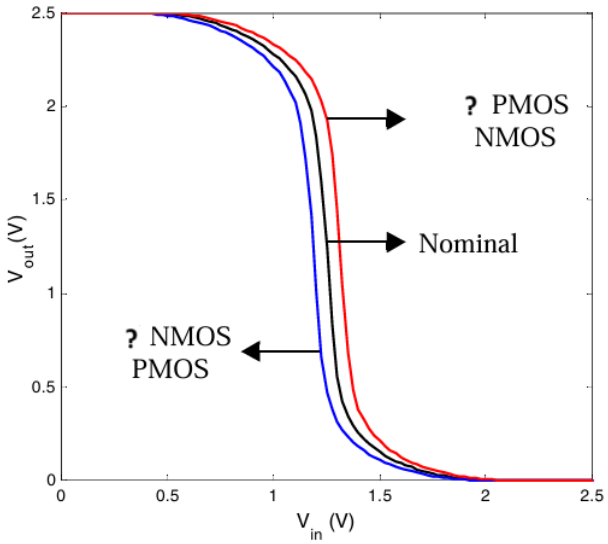
Question 30. Complete the following table by seeing the following plot:
Remember you have V_{DD},V_{IL},V_{IH},V_{IN},V_{OL},V_{OH},V_{THN},V_{THP} with you.

	V_{in}	V_{out}	NMOS (Region of operation)	PMOS (Region of operation)
A				
B				
C				
D				
E				

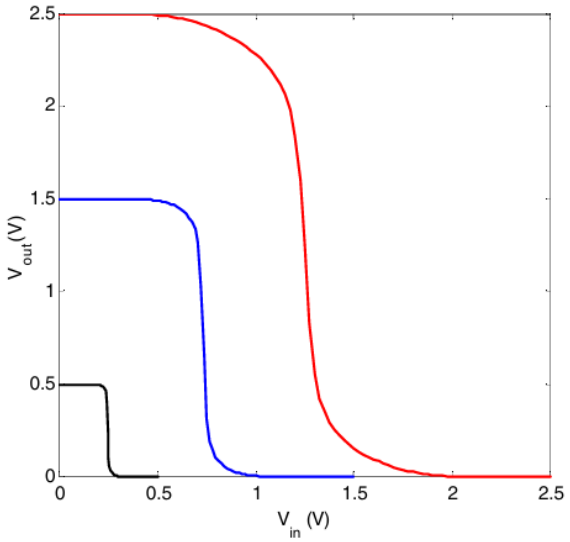


Question 31. Comment on these plots of VTC of CMOS inverter as a function of supply voltage (0.25 µm CMOS technology) :

(a) Impact of device variations on static CMOS inverter VTC. Comment Good/Bad.



(b) Reducing V_{DD} ? the gain... What happens at very low supply Voltages



Question 32. (a) In terms of noise margin, how do NAND and NOR gates perform in VLSI?
(b) Explain how you will implement an XOR function using NAND & NOR gates.
(c) Which has better "fan-in" out of NAND and NOR gates?
(d) Which has better “propagation delay" among NAND and NOR gates?
(e) Why is NAND more commonly used than NOR in digital circuit design?

Question 33. How does the transistor count differ between NAND and NOR gates in CMOS technology ? Also Draw the same.