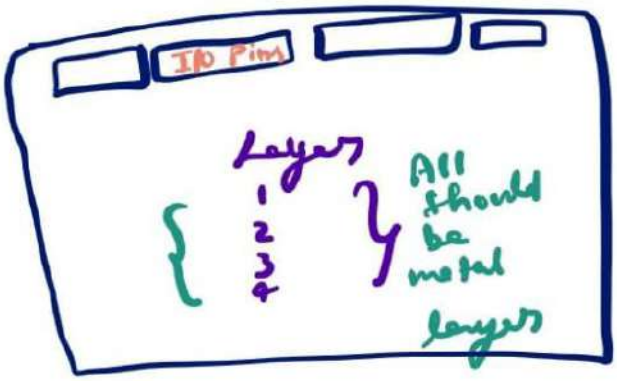
Inverter → Layout

Launch → Layout XL → OK All

Connectivity → Generate → All from Source



Shift + F → to visible it

To extend Rectangle

Click S & then Select →

Now, we'll detach the body → Select PMOS

Q → Properties ← Parameter

Parameter → Bodytie type → Detached → Top Tap

" for NMOS → " → Bottom Tap

For PMOS → Make a Nwell → Select from left side

Layer Section → Nwell → Make a rectangle outside PMOS

Now, make all connections as per video

Now, DRC check → Go to PVS → DRC Check

① Select your current directory & file → inverter in Run Directory

then ② Go to Rules → Select Technology Mapping file

Computer/PC → VLSI → Cadence_RB → FOUNDRY → install → analog → 45nm → pvtech.lib

Next Row → Technology → gpdk045_pvs

↓

Submit

↓

Remove errors.

How to make via from Metal to Poly.

Just Right click & select via to Poly when you are extending metal wise & vice-versa.

LVS Check → PVS → Run LVS

↓

Same Process

↓

Select Directory

↓

New thing is add my.rul file in Rule Set

↓

in Input

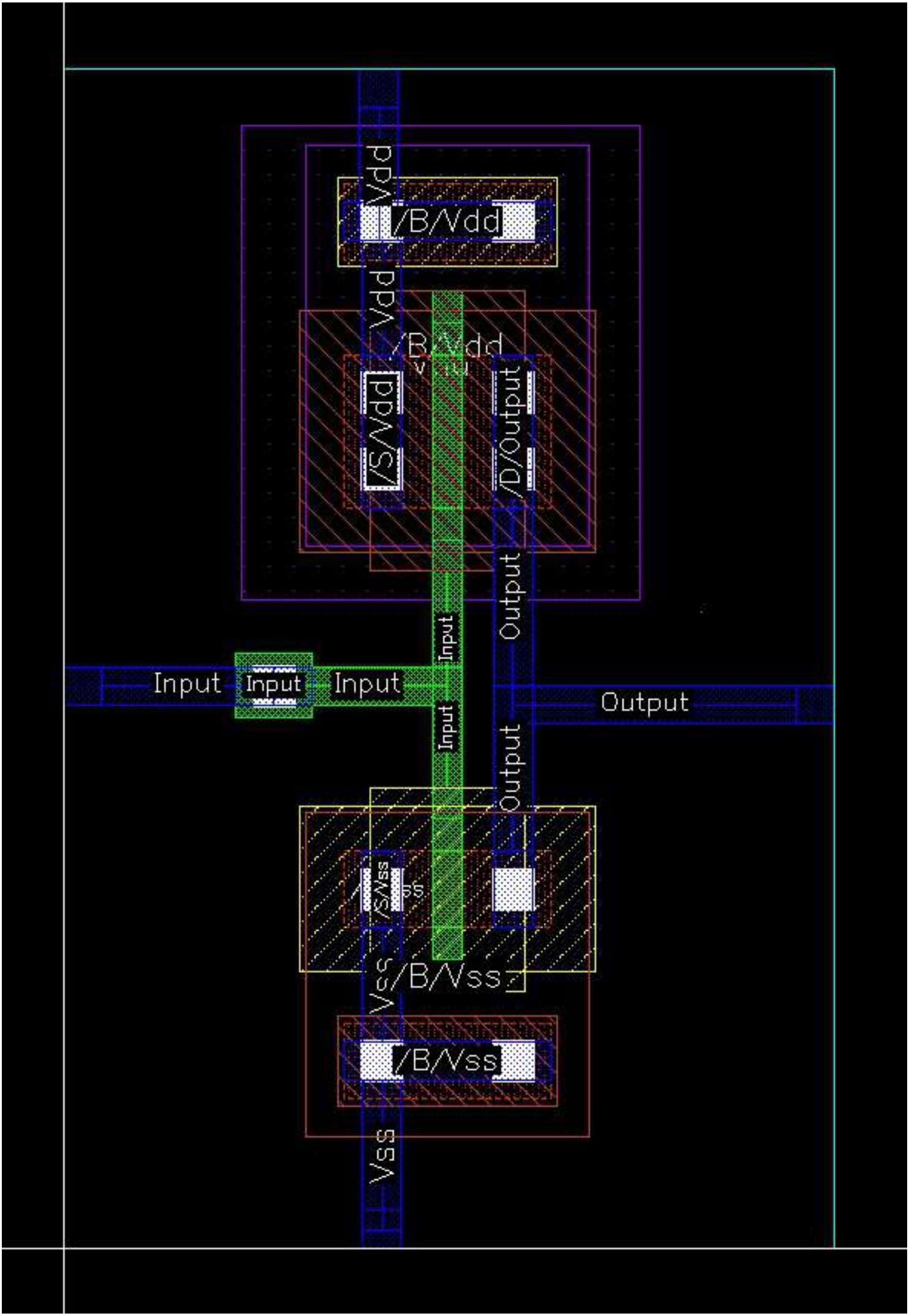
Convert Pin to Geometry + Text

↓

in Output

Additional Output Tick → Create Quantus QRC Input Data

SUBMIT


Vdd
/B/Vdd
Vdd
/B/Vdd
/S/Vdd
/D/Output
Output
Input
Input
Input
Input
Input
Output
Output
/S/Vss
ss
Vss/B/Vss
/B/Vss
Vss


PVS 19.13-64b LVS Run Status@vlsiserver
ERC Results
Empty
Extraction Results:
Clean
Comparison Results:
Match
Do you want to start the LVS DE?
Yes
No