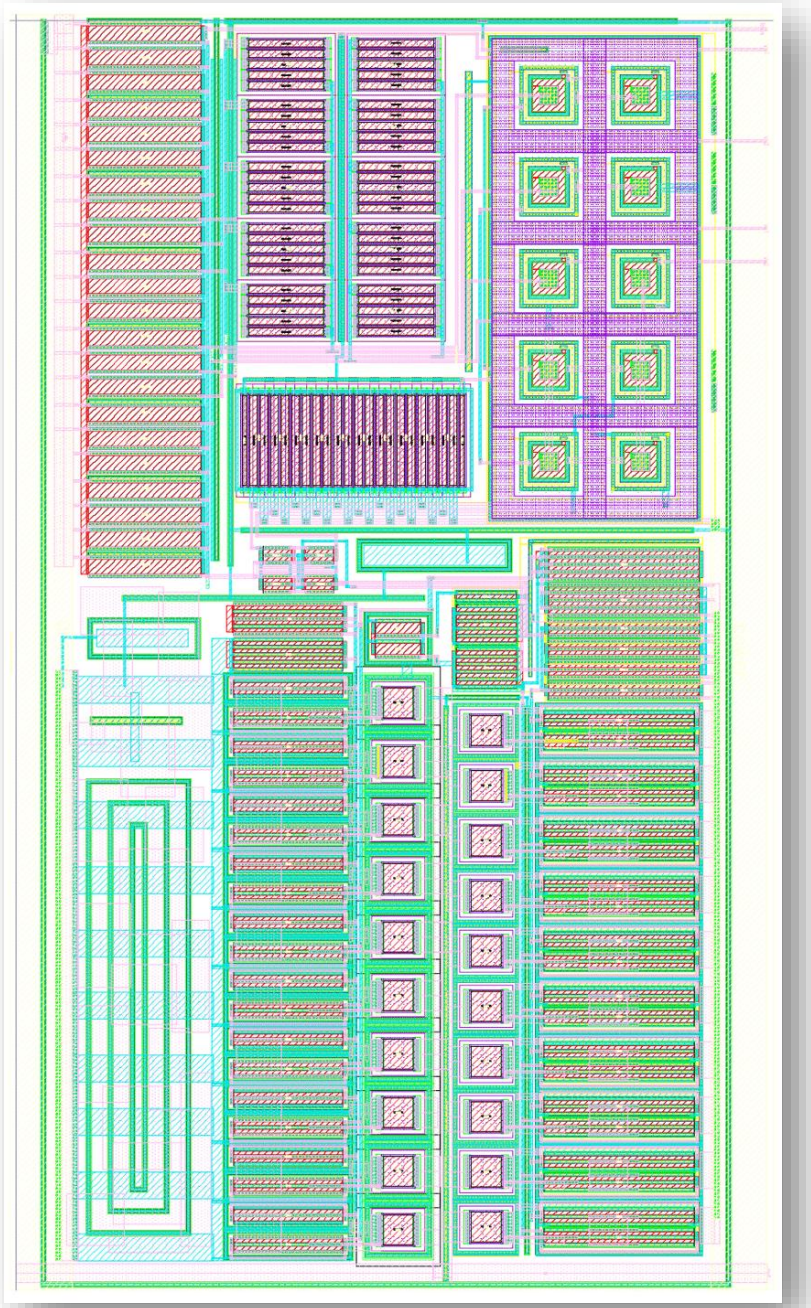
LAYOUT DESIGN



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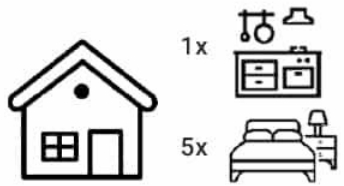
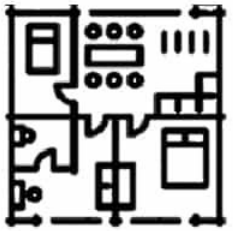
PREFACE

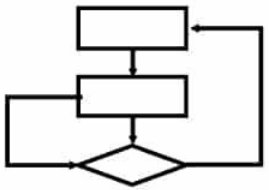
The preface underscores the critical role of human expertise in IC layout design, despite advancements in automation tools. It highlights the historical evolution of design methodologies and the constant need for adaptation to evolving challenges. The text emphasizes that while automation aids in efficiency, a deep understanding of fundamental concepts, methodologies, and the limitations of software remains indispensable for successful layout design.

Figure 1. The phases of IC design can be likened to the steps in building a house

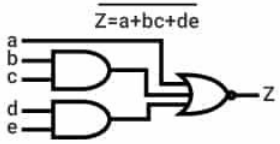


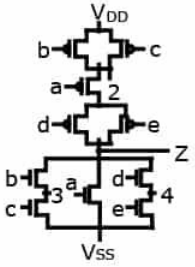


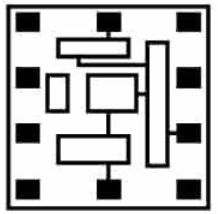
IC Specification & Funcional Design → RTL Code → Pre-sim Synthesis → Gate Level Netlist → Placement Routing → Layout → Post-sim Verification → Tape-out

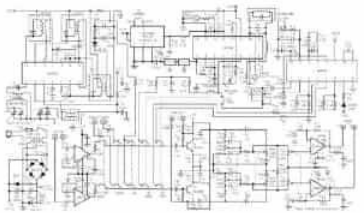


```
module fz (a,b,c,d,e,Z);
input a,b,c,d;
outout Z;
assign Z =
~(a|(b&c)|(d&e));
endmodule
```









Introduction

History of the profession

- The electronics industry has experienced rapid growth in size and complexity. IC layout design, initially performed manually, transitioned to computer-aided design due to the need for faster time-to-market and improved accuracy.
- Hardware platforms evolved from expensive mainframe computers to more affordable engineering workstations, making CAD tools accessible to a wider range of designers.
- As the hardware platforms evolved, software development progressed at an even faster rate. Companies such as Mentor Graphics, Cadence, Compass, and Daisy gained larger and larger shares of the IC and PCB design tools market.
- For the PC platform, a company such as Tanner, with a product called L-Edit, is an example of how the software development market has grown for IC design

Concept	Summary
What is layout design?	Also covers how layout design fits in the IC design flow
How do I read a schematic?	A schematic has more information than meets the eye!
Layer definition	An introduction to CMOS processes
CMOS transistor layout	A basic introduction
Design rules	These define the limits of what you are able to do
Layer connectivity	This defines what can be connected to what
A procedure to follow	General instructions
Developing a plan	Potentially the most important step for success!
General guidelines	Concepts to follow to do it right the first time

What is layout design?

The process of creating an accurate physical representation of an engineering drawing (netlist) that conforms to constraints imposed by the manufacturing process, the design flow, and the performance requirements shown to be feasible by simulation.

Let’s look at this definition in greater detail as there are numerous implications buried within.

• **Process**: Layout design follows a step-by-step process, involving setting up tools, defining floorplans, and performing verification checks.

• **Creation**: Design is creative, as layouts differ between technologies and regions, reflecting the adaptation to their specific contexts.

• **Accuracy**: The layout must match the schematic exactly, ensuring transistor-level equivalence without altering circuit design.

• **Physical representation**: Layout design translates the circuit into a physical form, depicting transistors and wires on silicon.

• **Engineering drawing**: Historically, schematics or block-level drawings have been the primary visual reference for layout designers.

• **Conform**: The design must meet requirements, balancing trade-offs like manufacturability, reliability, and time-to-market.

• **Manufacturing constraints**: Layout rules and guidelines, such as metal track width, ensure manufacturability and reliability.

• **Design flow constraints**: Guidelines enable compatibility with design tools and facilitate later stages like routing and text identification.

• **Performance constraints**: Layout is guided by assumptions from circuit design, with feedback loops for adjustments based on simulation.

IC Design Flow

Let us look at layout design in the context of an IC's complete life cycle and where it fits in the "flow." IC design is a multi-step process involving various teams and disciplines. The flow typically includes:

1. **Product definition**: Marketing defines the product concept to be developed.
2. **Architecture definition**: Circuit design engineers determine the chip architecture to meet market and functional requirements.
3. **System simulation**: Engineers verify block definitions and architecture, ensuring the design is sound and manageable.
4. **Circuit simulation**: Circuit design groups run digital and analog simulations, checking gate connectivity and timing, interfacing with layout designers.

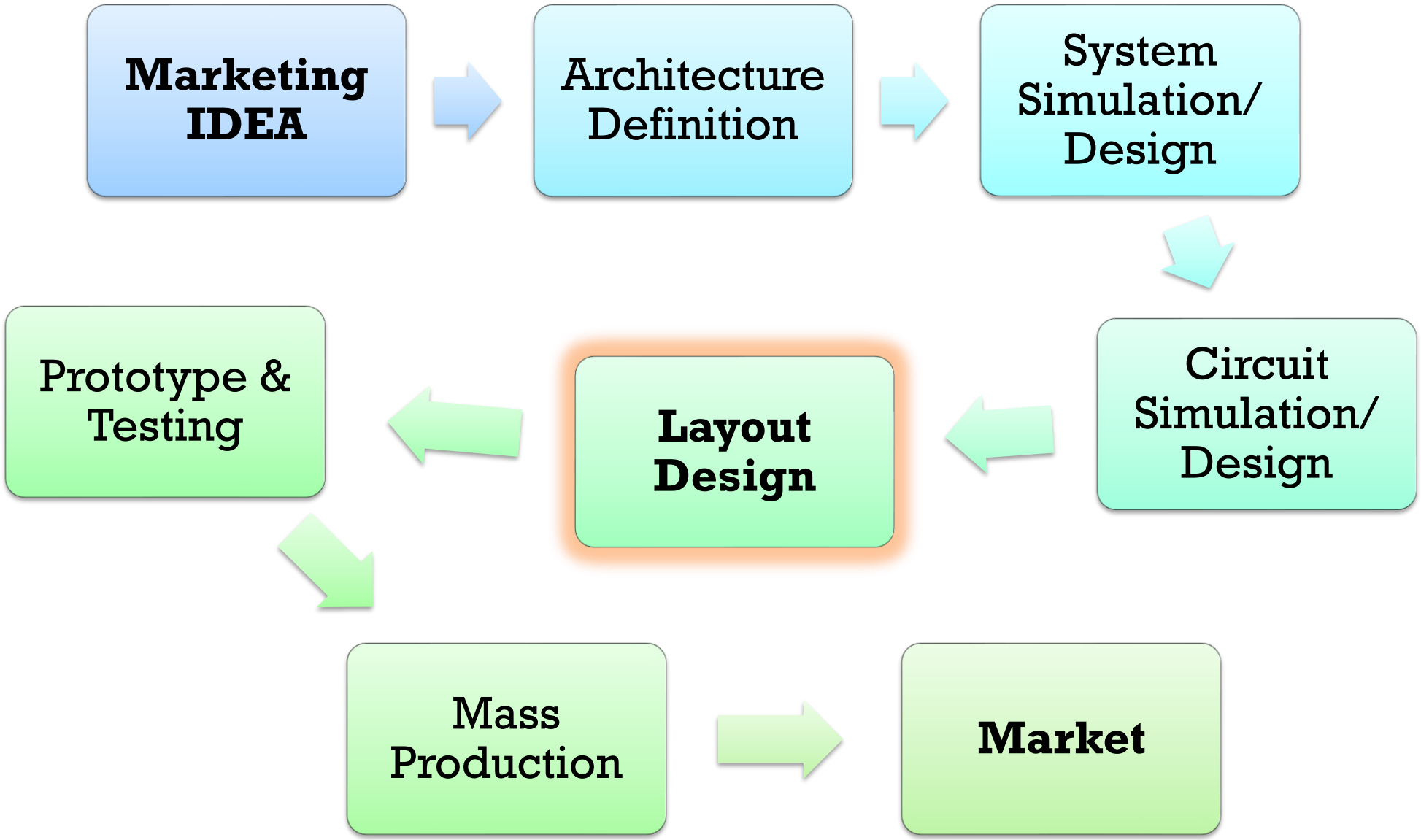
5. **Layout design**: Layout engineers create the chip's physical layout, implementing transistors, connections, and layers based on circuit schematics.
6. **Chip testing**: Test engineers validate process parameters and specifications, fixing errors with an engineering tester.
7. **Mass production**: Once errors are resolved, the chip proceeds to mass production and market.

This flow involves feedback loops and iterations to resolve design constraints and layout issues.

Q. Where do a layout designer’s work starts?

Ans. Once a schematic or netlist is created.

IC Design Flow



Schematic fundamentals :

Some basics

You have been given or have designed a schematic and are ready to move to layout. What's next?

The transistor is the smallest building block or device that we need to understand to effectively implement or layout a design. Let's first consider the functionality of the transistor and try to provide a basic understanding of the operation of a transistor so that we can maximize the performance of the design.

The MOS transistor

- Metal oxide semiconductor field transistors can be considered as switch which operates with proper biasing.
- MOSFET is three terminal device source , drain and gate.
- Biasing means application of appropriate voltage at three terminal of MOSFET so that it can be moved from on to off state or vice versa.

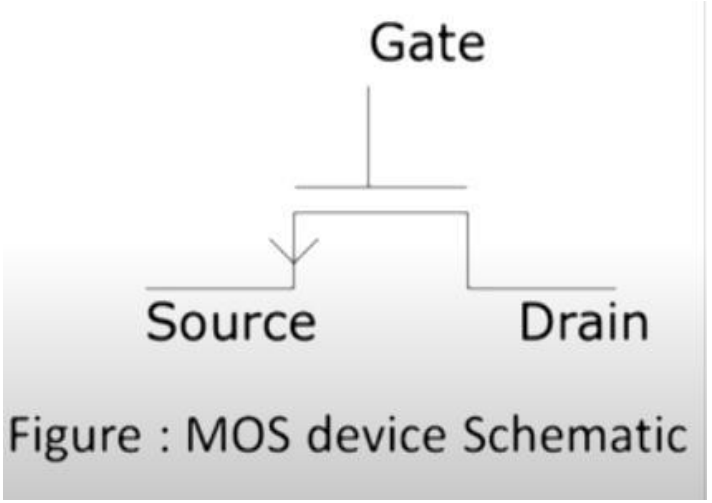


Figure : MOS device Schematic

- Metal-Oxide-Semiconductor (MOS) structure is created by superimposing several layers of conducting and insulating materials to form a sandwich- like structure.
- These structures are manufactured using a series of chemical processing steps involving oxidation of the silicon, selective introduction of dopants, and deposition and etching of metal wires and contacts.
- Transistor operation is controlled by electric fields so the devices are also called Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

Types of MOSFET:

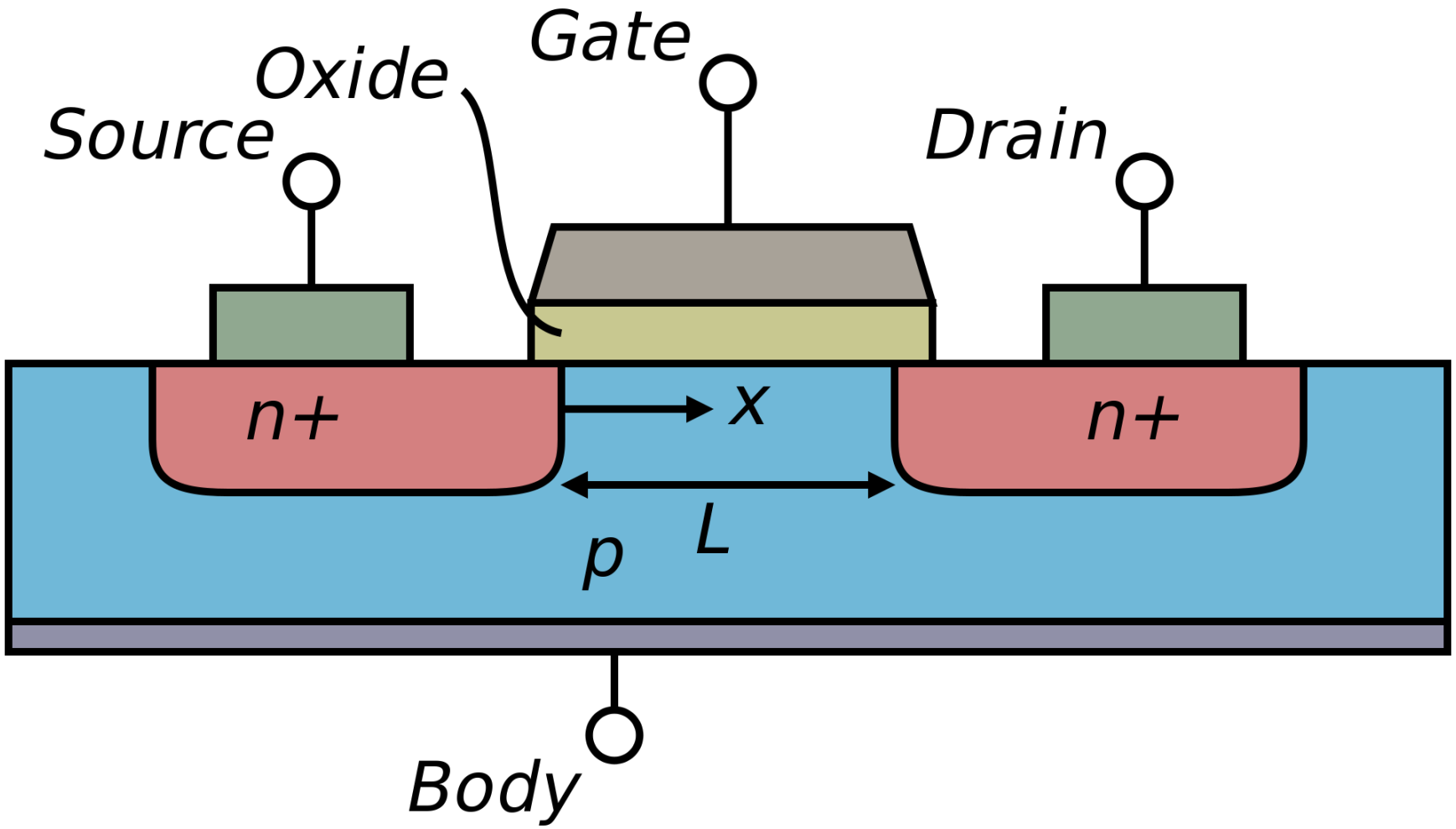
- Based on material properties

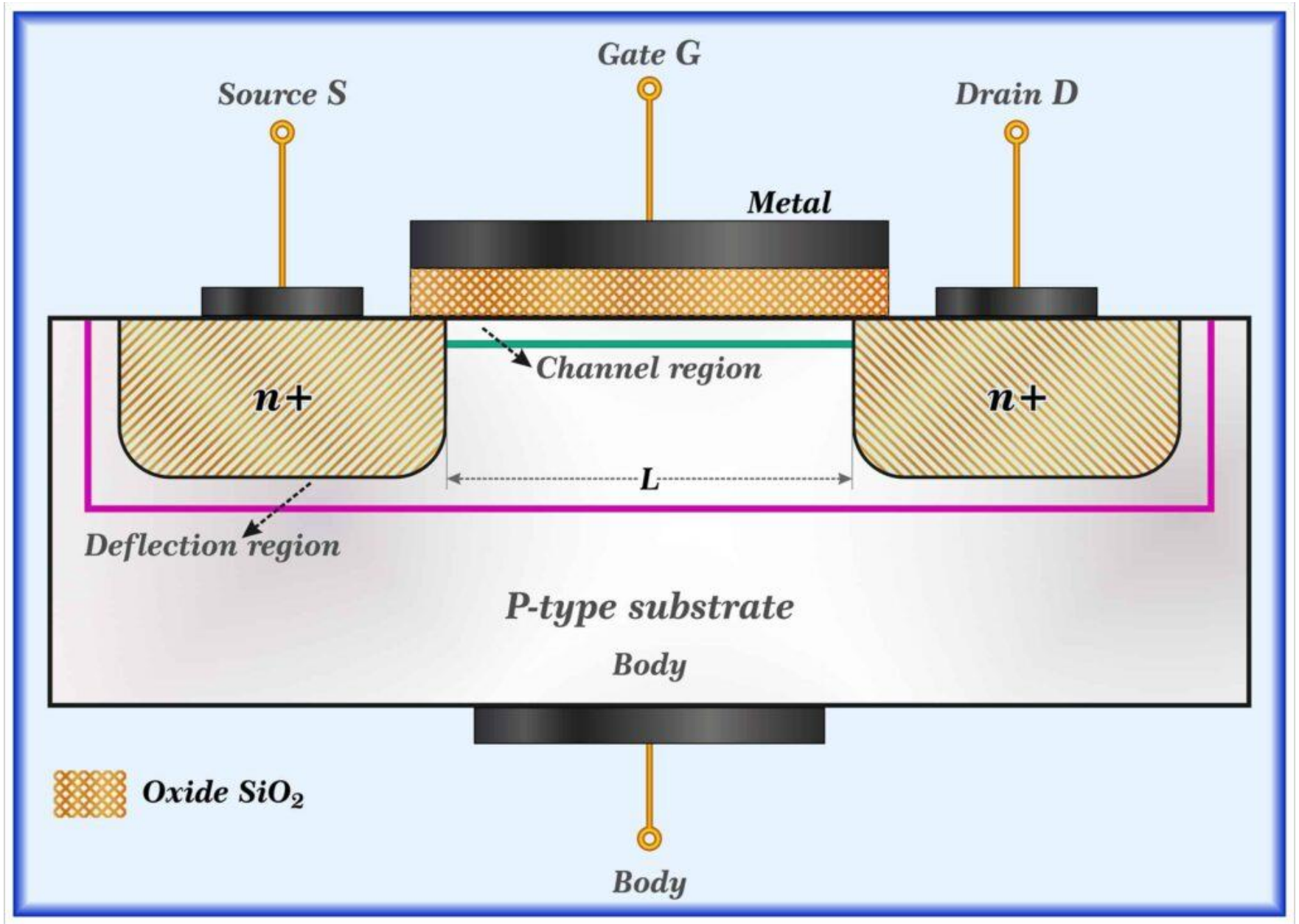
- N Mos- where electrons are charge carriers
- P Mos- where holes are charge carriers

- Based on electrical properties

- Enhancement mode MOSFET
- Depletion mode MOSFET
- So technically four types of MOSFET
  - N channel Enhancement mode MOSFET
  - P channel Enhancement mode MOSFET
  - P channel Depletion mode MOSFET
  - N channel Depletion mode MOSFET

MOSFET Structure




Gate G
Source S
Drain D
Metal
Channel region
n+
n+
L
Deflection region
P-type substrate
Body
Oxide SiO_2
Body

- The **main principle** of the MOSFET device is to be able to control the voltage and current flow between the source and drain terminals. It works almost like a switch and the functionality of the device is based on the MOS capacitor. The MOS capacitor is the main part of MOSFET.

- The semiconductor surface at the below oxide layer which is located between the source and drain terminal can be inverted from p-type to n-type by the application of either a positive or negative gate voltages respectively.

- When we apply a repulsive force for the positive gate voltage, then the holes present beneath the oxide layer are pushed downward with the substrate.

- The depletion region populated by the bound negative charges which are associated with the acceptor atoms.

- When electrons are reached, a channel is developed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel.

- Now, if a voltage is applied between the drain and source, the current flows freely between the source and drain and the gate voltage controls the electrons in the channel.

- Instead of the positive voltage, if we apply a negative voltage, a hole channel will be formed under the oxide layer.

Logic gates

•**Transistor-Level Schematics**: Modern schematics no longer primarily use transistors due to design complexity; higher-level abstractions are preferred.

•**Logic Gates**: Transistors are grouped into logic gates like NAND, NOR, and inverters to simplify designs and enhance efficiency.

•**Boolean Logic**: Logic gates are used to implement Boolean logic functions, performing operations on binary data.

•**CMOS Implementation**: Most logic gates are implemented using CMOS technology, combining p-type and n-type transistors for low power consumption and efficiency.

•**Inverters**: The inverter is the simplest logic gate and serves as a fundamental building block in digital circuits.

•**NANDs, NORs, and Transmission Gates**: Common logic gates used in CMOS technology for implementing Boolean logic functions.

INVERTER

•**Inverter Function**: The inverter is the simplest logic gate, inverting the input signal to its opposite polarity at the output.

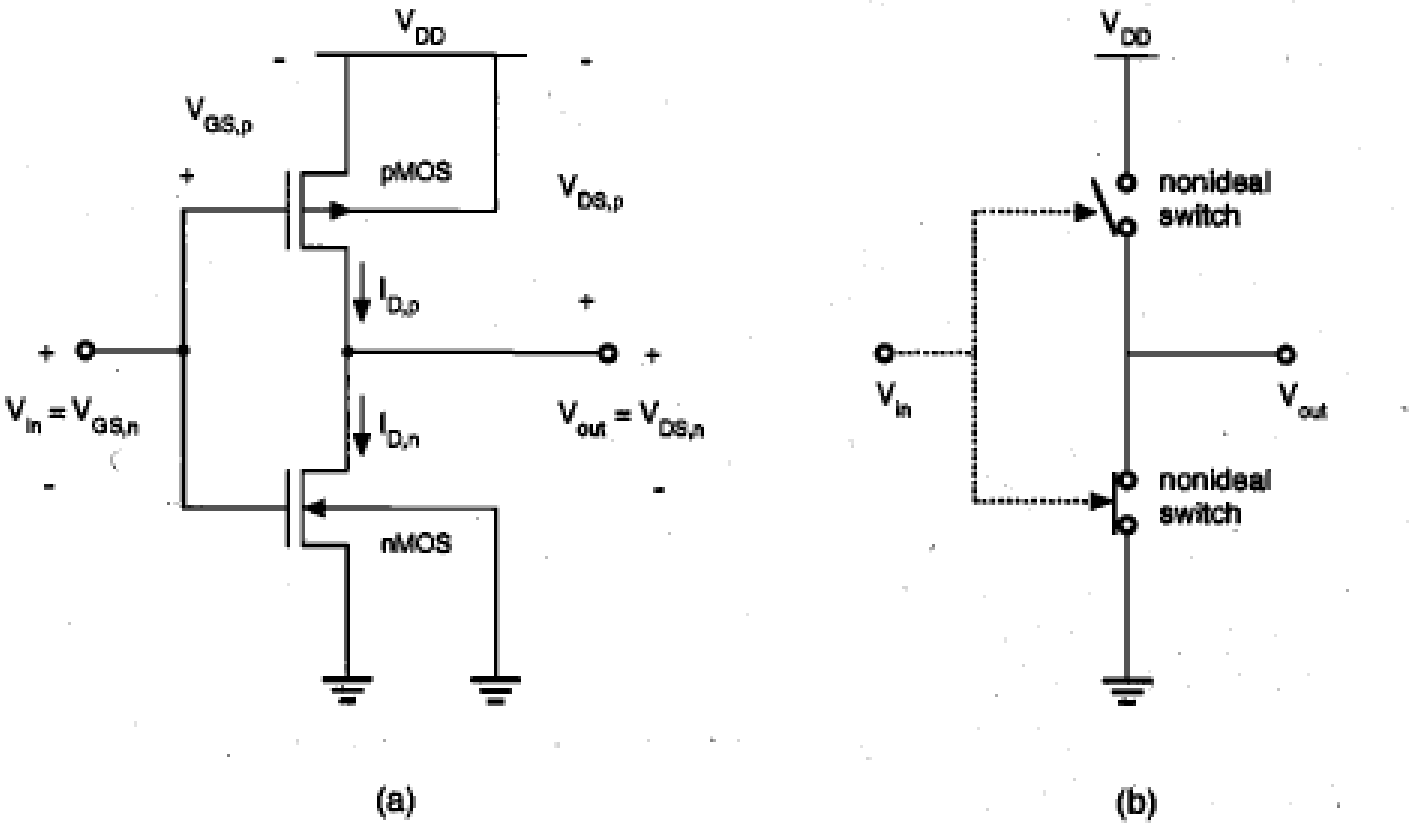
•**PMOS and NMOS Operation**: When the PMOS receives a "0", it drives a "1" to the output, while the NMOS is off. Conversely, when the input is "1", the NMOS drives a "0" to the output.

•**CMOS Inverting Nature**: CMOS logic is inherently inverting, with the NMOS and PMOS transistors never being "on" simultaneously, which minimizes power consumption.

•**Low Power Consumption**: CMOS circuits consume low power because there is no DC current path between VDD and VSS when the gate switches states.

•**Inverter Sizing**: In CMOS inverters, both PMOS and NMOS transistor sizes are specified, with widths typically listed first. For example, the PMOS width might be 2mm and NMOS 1mm, with a default transistor length for the process.

Schematic


V_DD
V_GS,p
pMOS
V_DS,p
I_D,p
I_D,n
V_in = V_GS,n
V_out = V_DS,n
nMOS
(a)
V_DD
nonideal switch
V_in
V_out
nonideal switch
(b)

Layout design

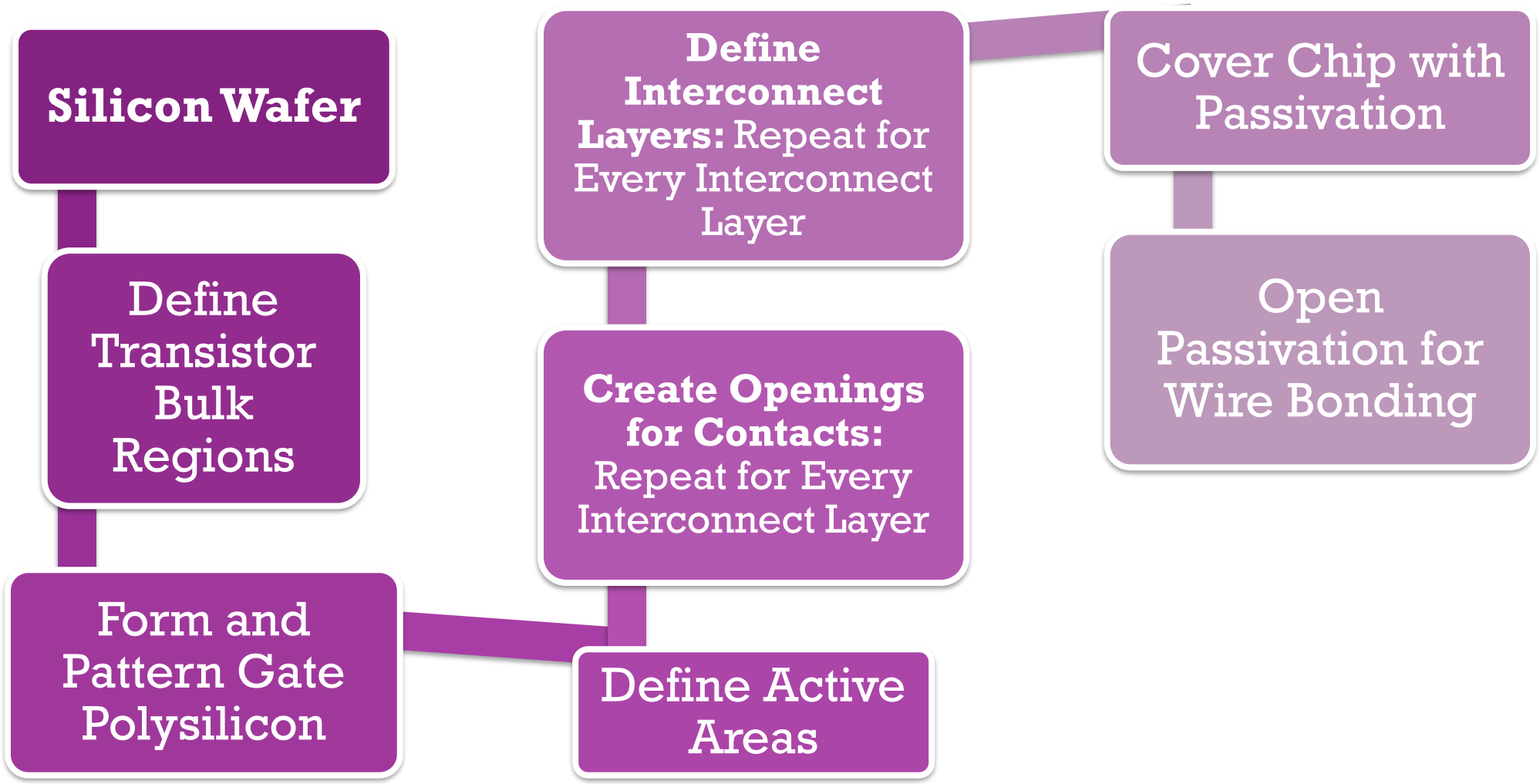
Q. What does a Layout Engineer do ?

Ans. The process of creating an accurate physical representation of an engineering drawing that conforms to constraints imposed by the manufacturing process, the design flow, and the performance requirements shown to be feasible by simulation.

Q. Who is a Layout Engineer ?

Ans. a layout designer is a person who knows basic electrical concepts, process limitations, and properties; has a talent for seeing and feeling space and floor plans; and can learn and use various CAD tools.

CMOS VLSI manufacturing processes



This diagram is a very simple explanation of the manufacturing process. Different process technologies have significantly different manufacturing steps.

Layers and connectivity

If we analyze most CMOS processes, we find that there are four basic layer types:

1. **Conductors:** These layers are conducting layers in that they are capable of carrying signal voltages. Diffusion areas, metal and polysilicon layers, and well layers fall into this category.

2. **Isolation layers:** These layers are the insulator layers that isolate each conductor layer from each other in vertical and horizontal directions. This isolation is required in both the vertical and horizontal direction to avoid “short circuits” between separate electrical nodes.

3. **Contacts or vias:** These layers define cuts in the insulation layer that separates conducting layers and allow the upper layer to contact down through the cut or “contact” hole. Metal vias or contacts are examples of these. Openings in the passivation layer for bonding pads are another example of a contact layer.

4. **Implant layers:** These layers do not explicitly define a new layer or contact, but customize or change existing conductor propriety. For example, diffusion or active areas for PMOS and NMOS transistors are defined simultaneously. A P^+ mask is used to create P^+ implant areas that define certain diffusion areas to P-type by the use of a P-type implant.

THE POLYGON

•Polygons are a fundamental building block in layout design.

•A polygon is an N-sided shape with N + 1 vertices (the last vertex is double-counted as both the origin and end point).

•Common uses include defining cell boundaries, transistors, n-wells, contacts, diffusion areas, and transistor gates.

•Polygons can be drawn in 90°, 45°, or freehand shapes for flexibility in covering irregular areas.

Advantages of Using Polygons:

•**Flexibility**: Can enclose odd-shaped areas not easily covered by simple rectangles.

•**Ease of Manipulation**: Polygons can be easily drawn, added to, or subtracted from, allowing for quick adjustments in design.

•**Merging Capability**: Polygons can be merged with other polygons at the same level and layer, simplifying hierarchical designs.

Disadvantages of Using Polygons:

•**Difficult to Modify**: Editing complex polygons for consistency (e.g., ensuring uniform width) can be tedious and time-consuming.

•**Larger Database Size**: Polygons require more computer memory compared to simpler design elements like "paths" in situations where paths can be used efficiently.

THE PATH

Paths are a highly efficient and flexible tool in layout design, particularly for connecting components. They offer consistent width, flexible angles, and a variety of justification and termination options, while requiring fewer computer resources than polygons.

•A path is a shape defined by a start point, end point, intermediate vertices, and a consistent width value.

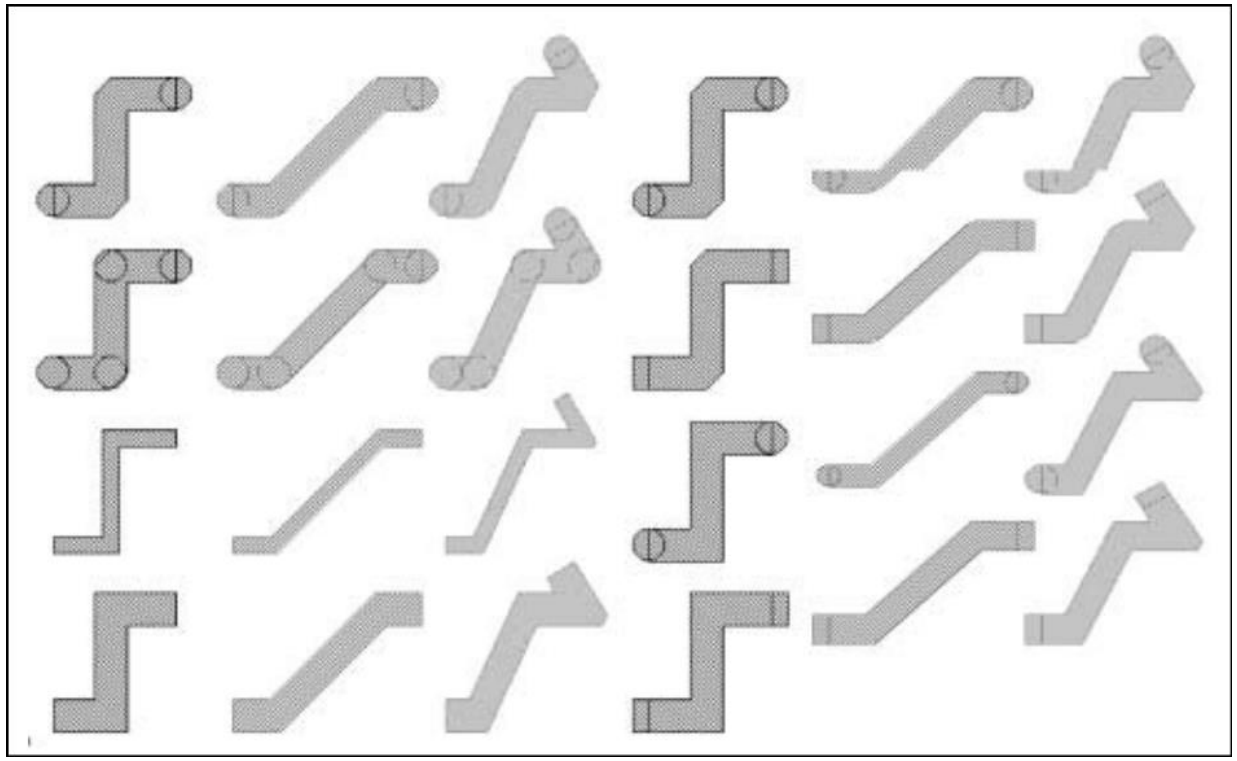
•Paths are primarily used to connect devices and run signals, ensuring uniform width across their length.

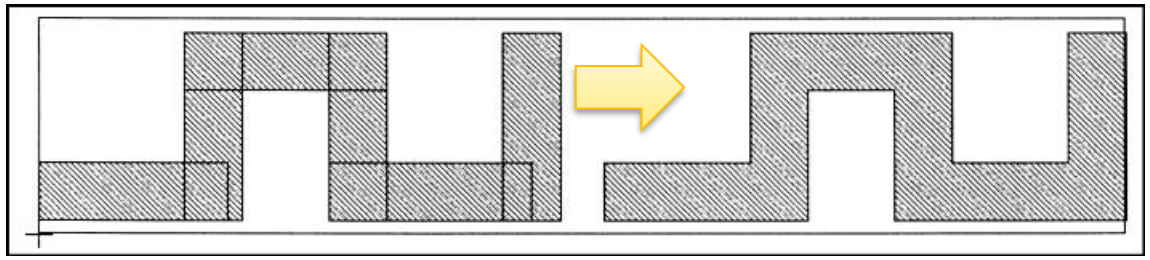
•The shape is controlled by vertices that define a centerline (or sideline), with an additional variable specifying the width.

Advantages of Using Paths:

- Efficient Use of Resources
- Flexibility in Angles
- Justification Options

Examples of Paths





Multiple paths flattened to a single polygon

Introduction to Transistor layout

The length and width of a transistor are the two most important dimensions of a transistor that we need to fully understand. As we stated previously, when people in the industry talk about the gate size of a specific technology, they are referring to the minimum gate length. Note the following:

- In terms of layout design, the length of the transistor is the distance between the source and the drain of a transistor.
- In terms of transistor performance, the length of the transistor is the distance electrons have to travel when the gate is “on” or “open” to produce a measurable current flow.
- The length of a transistor in terms of manufacturing capabilities is the narrowest possible piece of polysilicon (poly) that can be manufactured reliably.

Let’s now consider the width of a transistor. The width of a transistor should be thought of as the number of parallel channels that are available for current to pass from the source to the drain. Wider transistors have more channels available; more channels mean more current.

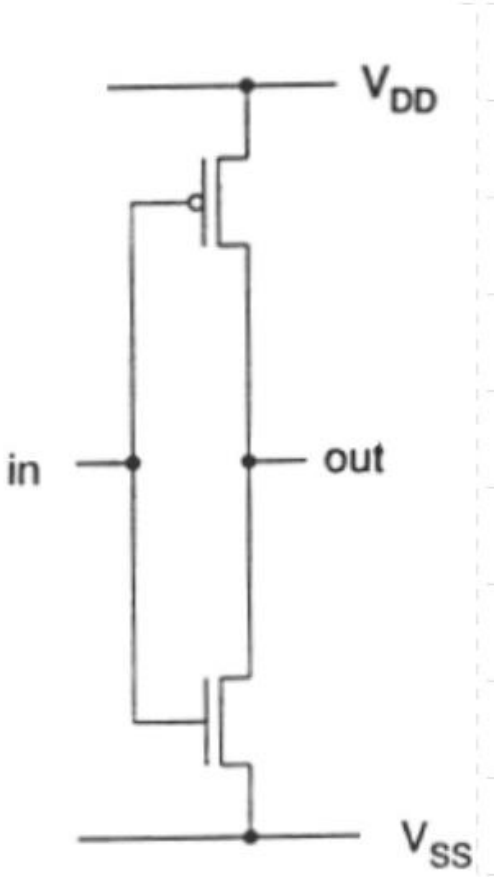
- To help you remember the convention of transistor length and width, think of a transistor like a bridge.
- The length of the bridge is the distance between the two sides of the river and the width of the bridge is the number of lanes of traffic that the bridge can accommodate.
- The amount of traffic that can cross the bridge is limited by the length and width of the bridge in the same way that current is limited by the length and width of the transistor.
- If the design of the bridge is to allow 100 cars to cross over in 1 minute, then the bridge needs to be made wide enough to achieve this goal.

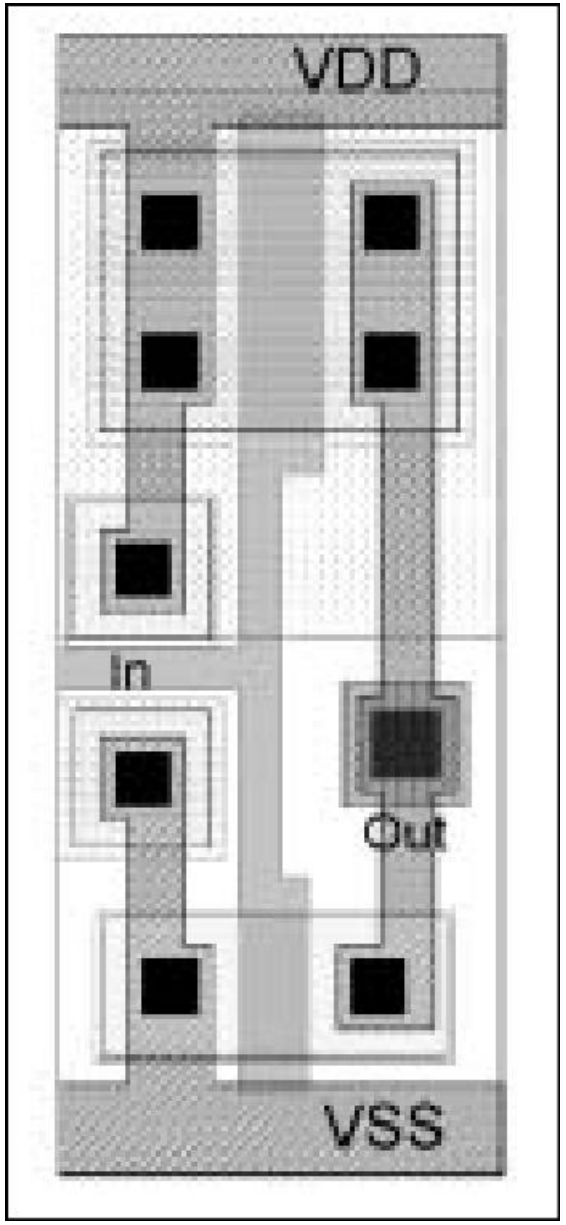
In most cases the length of the bridge is fixed (similar to the minimum allowable gate length) and the only degree of freedom we have to achieve our goal is to adjust the width.

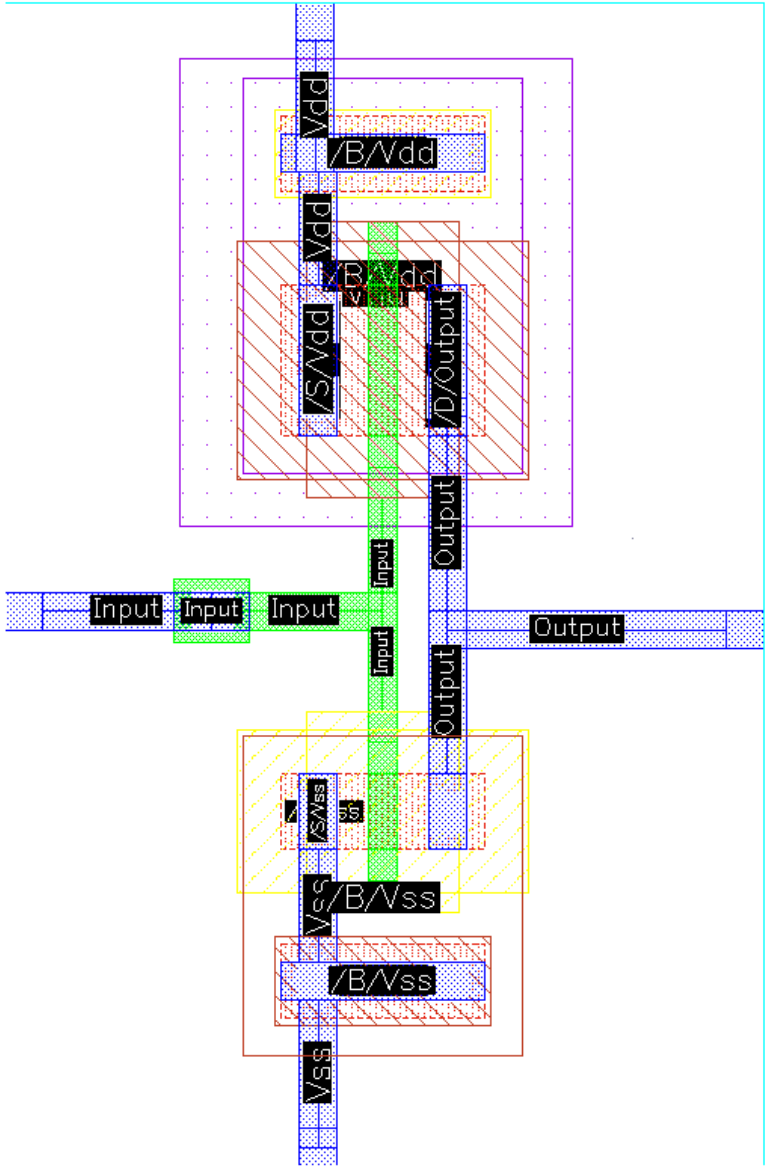
INVERTER LAYOUT

Now that we have all the basic concepts of transistor layout design, let's once again look at the simplest combination of transistors, the inverter. As you can see, the transistor representation is very simple, and now we are able to generate a layout since we know how a transistor looks and where it is connected.

- The PMOS is connected to VDD in the schematic as well as in layout.
- The NMOS is connected to VSS in both pictures.
- NMOS and PMOS transistors have the same IN signal on their gates and same OUT on their drains—in both pictures.
- The widths are different—the PMOS is twice as big as the NMOS transistor in this example.
- The lengths look similar, but they are different, and the difference cannot be seen.
- For N-well there is a N+ connection to VDD. This connection is implied in the schematic.


V_{DD}
in
out
V_{SS}


VDD
in
Out
VSS


Vdd
/B/Vdd
/S/Vdd
/D/Output
Output
Input
Input
Input
Input
Output
Output
/S/Vss
/D
Vss
/B/Vss
/B/Vss
Vss

Process design rules

Design rules are the rules that have to be respected when a given design is laid out. There are design rules for all of the components we have been introduced to: polygons and paths, transistors, and contacts.

Fundamentally, these design rules represent the physical limits of the manufacturing process.

Width Rule : Minimum width rules are fundamental constraints in layout design, ensuring the manufacturability and reliability of integrated circuits (ICs).

- These rules define the smallest allowable width for various design elements, such as metal tracks, transistors, and other components.
- Adhering to minimum width rules is crucial to prevent open circuits, short circuits, and other defects that can compromise the functionality of the IC.
- Violations of these rules can lead to manufacturing failures, yield loss, and potential device malfunctions.

Space Rule : Space rules are another critical dimension in layout design, defining the minimum distance between polygons.

- These rules are essential to prevent short circuits and ensure proper separation between components.
- Combined with width rules, space rules determine the layer pitch, which is a key parameter for routing and layout density.
- Designers must carefully consider both width and space rules to create layouts that meet manufacturing requirements and achieve optimal performance.

Overlap Rule : Overlap rules define the minimum overlap required between polygons on different layers to ensure proper connectivity and prevent misalignment-related defects.

- This is especially important for structures like metal layers over vias or contacts.
- Overlap rules help mitigate the impact of manufacturing variations and maintain the desired electrical connections.

A general procedure to follow

This procedure is straightforward and self-explanatory and could be applied to almost any engineering task. Of course we will concentrate on how it applies to layout design.

Layout Design Process

Step 1: Define Floorplan

•Collect and review relevant knowledge of layout design.

•Develop a strategy for component placement and signal routing.

•Create a high-level floorplan outlining general areas for components and signals.

Step 2: Implement Design

•Execute the floorplan and place components.

•Consider special requirements and routing constraints.

•Implement the design bottom-up, starting with lower-level components.

•Adjust the floorplan as needed based on implementation results.

Step 3: Layout Verification

•Perform computer-based checks (e.g., DRC, LVS, parasitic extraction).

•Conduct a visual inspection to identify any issues not detected by computer checks.

•Take corrective action as needed.

Step 4: Final Steps

•Perform a final sanity check to ensure all requirements are met.

•Conduct a layout audit to verify accuracy and completeness.

•Extract parasitics for simulation.

Key Points for consideration:

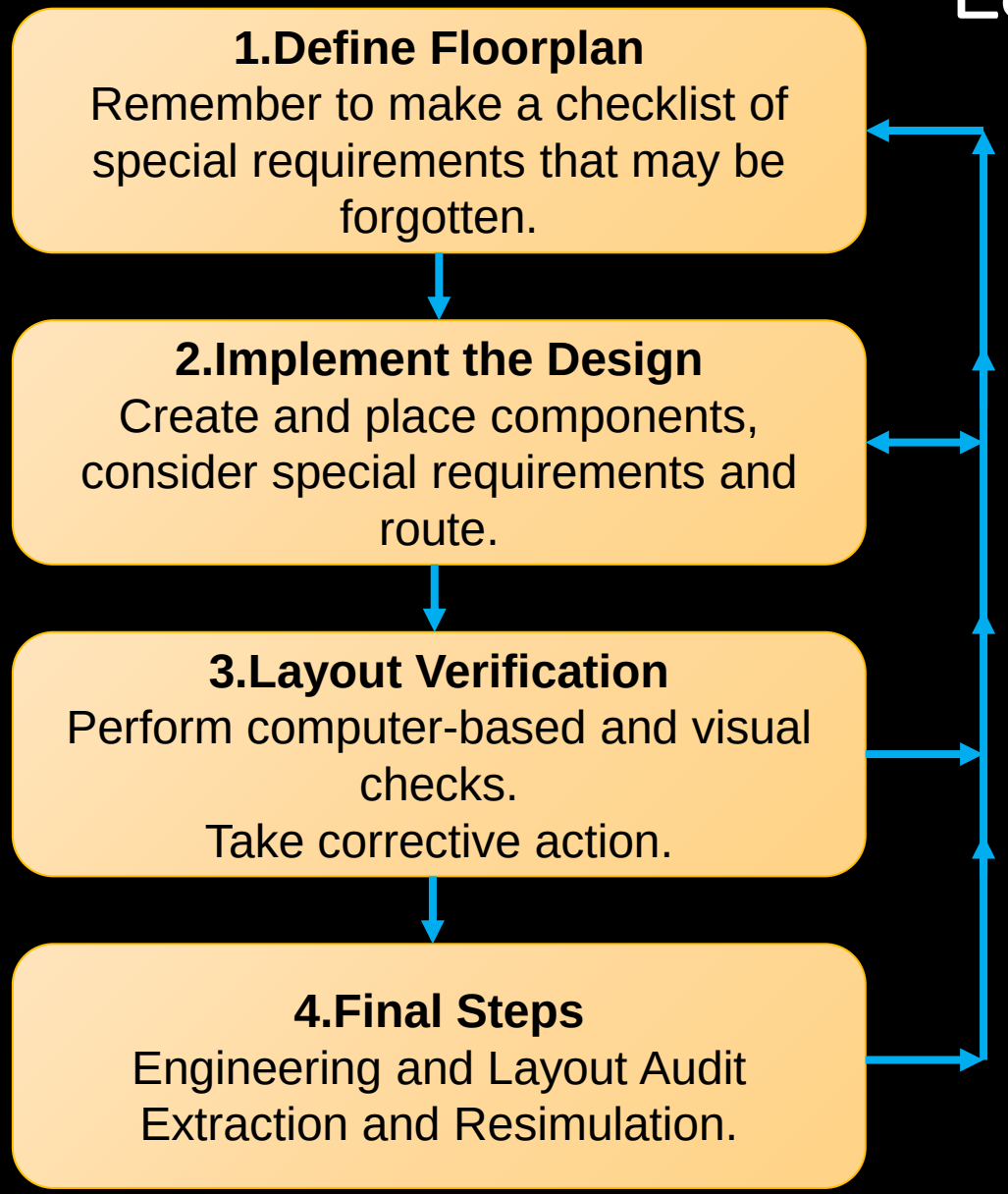
•The layout design process is iterative and may involve revisiting previous steps.

•A well-defined floorplan is essential for efficient layout implementation.

•Both computer-based checks and visual inspection are crucial for verification.

•The final steps involve ensuring the layout meets all requirements and preparing it for manufacturing.

Layout design procedure



Plan your work!

Implement

Verify

Get a second opinion

Planning stage

- The most important stage in any kind of layout design is the planning stage. Quality in layout means that the end results, the final layout, meets the customer's (i.e., the design engineer's) requirements.
- To achieve quality results, a layout designer has to prepare a list of input requirements.
- Taking into consideration all the specifications and a list of output requirements in order to ensure that output layout requirements are met.

1. **Developing a Layout Floorplan:** Now that we understand how to build single transistors and the concepts behind design rules and manufacturing process, we can start to plan our layout with some sound fundamental knowledge.
    1) The first step, 1.1, is related to the planning of the layout of the power supplies and/or global signals. The power supply connectivity is typically called the power grid. Power supply resistance from the interface to all parts of the design must be considered.

2) Step 1.2 is to list all of the input and output signals. Each signal is assigned a position on the interface of the design to the neighboring designs. The interface is defined as the boundary of the design.
3) In Step 1.3 we have to deal with special design requirements such as layout symmetry, specific requirements for latch-up protection, or noise immunity.
4) Step 1.4 is very important to help finalize the size of the design and estimate the feasibility of meeting all of the design requirements within the area and schedule constraints.
5) Step 1.5 is a sanity and cross-check to confirm that all requirements have been met and none missed. There are requirements related specifically to layout guidelines and styles for the process, but also circuit design requirements as well.

The layout audit also relates to the next level of integration for the piece that you designed. The "brick" that you have now floor-planned has to interface perfectly to all of its neighbors and their interfaces; otherwise, when put together it won't work exactly as planned.

2. Stick Diagrams
3. Hierarchical Design

2. **Stick Diagrams:** Stick diagrams are a simple way of floor planning a circuit in preparation for layout. In many cases it is very useful for circuit design engineers to sketch for themselves a simple layout drawing without respecting any design rules, in order to imagine more realistically how the layout can be done and if it can be done at all.

    1. Step 1 shows a preliminary placement of all of the devices. In this case the VDD and VSS power line architecture has been predefined, as has the orientation and location of PMOS and NMOS transistors.
    2. Step 2 shows the procedure for identifying which actives are connected to the same potential, and also the effect of flipping devices in order to take advantage of “sharing” these nodes.
    3. Step 3 shows the final result of the active sharing. This is, in fact, the final layout with the interconnect optimized. The cell is narrower than in the previous steps.

3. Hierarchical Design

2. **Hierarchical Design:** A hierarchical design is one that has a reference or uses another component as part of its construction. These subcomponents in turn may reference other components. This is similar to the concept of a subroutine in a computer program.

Advantages of Using Subcomponents in Layout Design:

•**Efficient Resource Management**: Subcomponents reference existing data, reducing redundant copies and saving memory.

•**Component Reuse**: Pre-verified components can be reused, improving efficiency and quality.

•**Concurrent Engineering**: Design partitioning allows parallel tasks, speeding up the design process.

•**Hierarchical Design**: Layouts resemble tree structures with repeatable and reusable leaf cells.

•**Scalability and Flexibility**: Cells can be flipped, rotated, and arrayed to optimize layout design and resource usage.

In terms of layout design we refer to these reusable subcomponents as **leaf cells**. The term **leaf cells** comes from the fact that a hierarchical design resembles a tree with a trunk, more primary branches, many more smaller branches, and finally, many, many, many leaves

Layout planning procedure

1.Define Floorplan
Remember to make a checklist of special requirements that may be forgotten.

2.Implement the Design
Create and place components, consider special requirements and route.

3.Layout Verification
Perform computer-based and visual checks.
Take corrective action.

4.Final Steps
Engineering and Layout Audit
Extraction and Resimulation.

1.1 **Define Power Grid & Global Signals**
Position, width, abutment requirements, and global connections such as tub contacts.

1.2 **Define Signals**
Interface location and width as well as critical and special cases.

1.3 **Consider Special Design Requirements**
i.e., symmetrical layout cells, guard banding, noise, and latch-up protection.

1.4 **Approximate Size and Hierarchy**
Floorplan components and signals, estimate total size and check against budget.

1.5 **Arrange for Audit**
Engineering and Layout Sanity Check.

General guidelines

Now that we have considered a layout floorplan, it is time to implement the design. There are general guidelines that should be followed both in planning and implementing the design, and the fundamental ones are listed here.

1. Guidelines for the Layout of Power Lines:

•**Line Width:** Determine line width based on power requirements and resistivity information.

•**Metal Layer Selection:** Use the lowest metal layer possible for power distribution to minimize vias and improve cell porosity.

•**Avoid Notching:** Notching power lines can create weak points and increase the risk of failure.

•**Internal Routing:** Ideally, route power lines within the cell to ensure correct construction and avoid external connections.

2. Guidelines for the Layout of Signals:

•**Layer Selection:** Choose routing layers based on process parameters and circuit requirements.

•**Signal Width:** Minimize input signal width and routing length to reduce capacitance.

•**Routing Width:** Select routing width carefully to accommodate vias and contacts.

•**Routing Direction:** Maintain consistent routing direction within cells to simplify routing and improve layout density.

•**Signal Labeling:** Label all important signals for easier verification and debugging.

•**Contact Placement:** Consider the number of contacts required for each connection, as multiple contacts may be necessary for certain applications.

3. Guidelines for the Layout of Transistors
4. Guidelines for the Layout of a Hierarchical Design
5. Quality Metrics

3. Guidelines for the Layout of Transistors:

•**Cell Templates:** Use predefined templates for PMOS and NMOS transistors to ensure consistent placement and sizing.

•**Transistor Fingering:** Use fingering for large transistors to optimize performance and meet design rules.

•**Power Supply Sharing:** Share power supply nodes between transistors to save area and reduce routing complexity.

•**Contact Placement:** Carefully consider the number and placement of contacts for source and drain connections.

•**Routing Considerations:** Use 90-degree polygons and paths whenever possible to simplify layout and verification.

•**N-Well and Substrate Connections:** Plan for and standardize connections to N-well and substrate regions.

•**Avoid Soft Connections:** Ensure all connections are made through designated routing layers to avoid performance issues.

4. Guidelines for the Layout of a Hierarchical Design

- **Floorplan Planning:** Develop a well-defined floorplan at all levels of the design.
- **Hierarchy Definition:** Establish a clear hierarchy for the design, considering factors like reusability, parallelism, and symmetry.
- **Cell Interface Standards:** Define and adhere to standard interfaces for cells to ensure smooth integration.
- **Boundary Considerations:** Plan for and maintain consistent boundary interfaces between cells.
- **Half Design Rule Approach:** Use this approach to ensure proper spacing and avoid violations when cells are abutted.
- **Verification:** Verify cells with their neighbors to ensure correct integration and avoid issues.

5. Quality Metrics

- **Area:** Minimize the overall area occupied by the layout.
- **Performance:** Optimize for speed and power consumption.
- **Porosity:** Ensure sufficient space for routing and avoid congestion.
- **Manufacturability:** Design for easy fabrication and high yield.
- **Maintainability:** Consider the ease of making future modifications.
- **Reliability:** Ensure long-term reliability, including resistance to electromigration.
- **Interface Compatibility:** Design for compatibility with other components and systems.
- **Shrinkability:** Consider the ability to scale the layout for future process technologies.
- **Reuseability:** Design for potential reuse in different applications or processes.
- **Layout Flow Compatibility:** Ensure compatibility with downstream tools and methodologies.

Implementing the design

1. **Pre-Design Planning**:

•**Make a Plan**: Before starting the layout, always have a well-thought-out plan in place. Anticipate the next steps and potential challenges to minimize rework due to missed details or mistakes.

2. **Component Placement**:

•**Initial Placement** : Component placement is crucial, as it determines how easily the design can be routed. This includes transistors, contacts, power lines, and interface locations for signals.

•**Label Signal Lines**: Ensure all important signal lines, such as power and feed-through lines, are clearly labeled to avoid connection errors during routing.

•**Placement Feasibility**: Initial Placement ensures the floorplan is feasible and sets the foundation for detailed placement.

3. **Detailed Placement and Critical Routing** :

•**Consider Special Design Requirements**: This step involves paying attention to critical paths, layout symmetry, noise immunity, and latch-up protection.

•**Routing of Critical Signals**: Difficult signals, such as power supplies and clock lines, should be routed during this stage to ensure proper signal integrity.

•**Allocate Extra Space**: Always allow for extra space during the layout to accommodate potential design changes or new requirements later in the process.

4. **Interconnect Routing :**

•**Completing the Routing**: With a well-planned floorplan and optimal component placement, interconnect routing becomes much easier. The routing should respect the design's special requirements and be straightforward if the earlier steps were properly executed.

•**Routing Layers**: Consider the direction of routing and space for signal lines to ensure proper connectivity.

1. Cell Layout

- The leaf or logic cell is in general a layout that is drawn from a transistor-based schematic; therefore, the majority of components to be used in this type of design would be polygons, transistors, contacts, and signal pins.
- “Polygon pushing” is the layout design style used here, as we are implementing circuitry at the lowest level of abstraction and we need detailed knowledge of the entire set of layers and layout design rules.
- Formally, this is known as a “full custom” design style.

The key concepts to be addressed at this level of layout include the following:

- ✓ Detailed knowledge of the entire set of layers and layout design rules.
- ✓ The size of the design, estimated from the number of transistors in the design and the layout design rules.
- ✓ Attention to transistor-level placement and interconnect to implement logic gates.
- ✓ Careful floorplanning and architecture definition to minimize area and maximize performance.
- ✓ Careful design of the power supply implementation.

2. Block Layout

The difference between a cell and a block is open to interpretation, but in general a cell is referred to as a block when it incorporates circuitry of medium complexity and functionality and is mainly composed of instantiated cells.

The important factors to keep in mind for block level design are as follows:

- The size of the design is estimated from the number of cells in the design and the number of external and internally routed signals.
- It is most common in blocks to have a significant amount of space allocated for spare components and signals as well as signals that may simply pass through the block. These signals are referred to as feed-through signals.
- Some blocks will have functionally different components such as a mix of digital and analog cells. In this case there may be special considerations for the different circuit requirements such as latch-up and noise immunity.

3. Chip layout

- Implementation of the full chip layout is conceptually identical to that of a large block in that the steps from layout planning through to auditing remain the same.
- Full chip layout designs will incorporate blocks and cells of diverse types, so detailed knowledge of all layout design styles is required to maximize the chance of success.

Aspects that must be addressed at the chip level and generally nowhere else include the following:

- Design partitioning of very large and diverse blocks.
- Defining and planning the interface to the outside world.
- Planning and implementing critical signals that are routed over the entire chip.
- Floorplanning techniques and maintenance are of paramount importance here.
- Estimating the chip size is a significant task in itself.
- In the role of a layout leader responsible for a full chip layout, there is also the requirement to define layout methodologies, task allocation, and scheduling for the entire team.
- Also, an understanding of the suite of layout design and layout verification tools is important in ensuring that the team performs efficiently.

Layout planning procedure

1.Define Floorplan
Remember to make a checklist of special requirements that may be forgotten.

2.Implement the Design
Create and place components, consider special requirements and route.

3.Layout Verification
Perform computer-based and visual checks.
Take corrective action.

4.Final Steps
Engineering and Layout Audit
Extraction and Resimulation.

2.1 Design and/or Place Components
Create and place components as required using the floorplan and layout guidelines.

2.2 Consider Special Design Requirements
Consider critical and methodology elements and refine the placement of cells.

2.3 Complete Interconnect
Complete all connections usually addressing critical items first.

Verification

- **Importance:** Verification is a critical step to ensure the accuracy and functionality of the layout design.
- **Cost and Time:** Errors in IC design can be extremely expensive and time-consuming to fix.
- **Robust Verification Plan:** A comprehensive plan is necessary to address all potential failure mechanisms.
- **Step-by-Step Approach:** The verification process involves multiple steps to check different aspects of the design.
- **Goal:** The goal is to get the design right the first time to avoid costly revisions.

Three Types of Checks :

1. Design Rules Check (**DRC**)
2. Layout versus Schematic (**LVS**)
3. Electrical Rules Check (**ERC**)

DESIGN RULES CHECK (**DRC**)

- **Purpose:** Checks the layout against manufacturing process rules.
- **Scope:** Includes width, space, and other design rules.
- **Supplementary Rules:** Verifies methodology, connectivity, and guideline rules.
- **Comprehensive Approach:** Consider the design in its intended context, including interfaces with other cells.

Important Points:

- DRC is a critical step to ensure manufacturability and avoid defects.
- It involves checking the layout against a set of design rules.
- Supplementary rules help identify potential issues related to design methodology and connectivity.
- A comprehensive approach includes verifying the design in its intended context with other components.
- DRC tools can automate much of the verification process.
- Designers should carefully review the DRC results and address any identified violations.

LAYOUT VERSUS SCHEMATIC (**LVS**)

- **Purpose:** Compares the layout to the schematic to ensure correct connectivity and component matching.
- **Key Checks:**
  - Electrical connectivity of all signals
  - Device sizes (transistors, resistors, capacitors)
  - Identification of extra components or signals not included in the schematic
- **Relationship with Electrical Rules Check:** LVS partially overlaps with electrical rules checks, as both verify the correctness of electrical connections and component parameters.

Important Points:

•LVS is a crucial step in layout verification to ensure the layout accurately represents the intended circuit.

•It involves comparing the layout to the schematic and checking for discrepancies.

•LVS helps identify errors in connectivity, component sizing, and the presence of unintended components.

•LVS can be used in conjunction with electrical rules checks for a more comprehensive verification process.

ELECTRICAL RULES CHECK (**ERC**)

- **Purpose:** Checks for electrical connectivity errors and device-related issues.
- **Overlap with LVS:** Many ERC checks are also covered by LVS.
- **Efficiency:** ERC can be faster than LVS and useful for debugging specific issues like VDD-to-VSS shorts.
- **Common Checks:**
  - Unconnected, partly connected, or extra devices
  - Disabled transistors
  - Floating nodes
  - Short circuits
  - Antenna rules

Important Points:

- ERC is a valuable tool for identifying electrical connectivity errors.
- It can be used as a standalone check or in conjunction with LVS.
- ERC is often faster than LVS, making it useful for initial debugging.
- It can help identify issues like unconnected devices, floating nodes, and short circuits.

Layout planning procedure

1.Define Floorplan
Remember to make a checklist of special requirements that may be forgotten.

2.Implement the Design
Create and place components, consider special requirements and route.

3.Layout Verification
Perform computer-based and visual checks.
Take corrective action.

4.Final Steps
Engineering and Layout Audit
Extraction and Resimulation.

3.1 Design Rule Check (DRC)
Checks process design rules and supplementary rules.

3.2 Layout versus Schematic (LVS)
Checks that layout connectivity is identical to schematic connectivity.

3.3 Electrical Rules Check (ERC)
1. Check for connectivity problems (Sometimes optional).

3.4 Visual Inspection
1. Plot the design and inspect. Check against layout guidelines and special rules.

Final steps

1. Verifications :

- In terms of verifications of the final files, here are some considerations. Because the mask shop requires GDSII file type, the final verification will be done on the same file that goes to manufacturing.
- If the layers shipped to the mask shop are different from the ones used for design, the final verification has to be done on the GDSII required by the mask.
- The database has to be translated from the design layers that were used and verified online into the mask shop layers and verified as the final “golden” verification.
- Most important factor is that the final verification be done using “frozen” GDSII generated from a “frozen” database, which means that nobody can touch the original online data.
- This way you can ensure unique data.

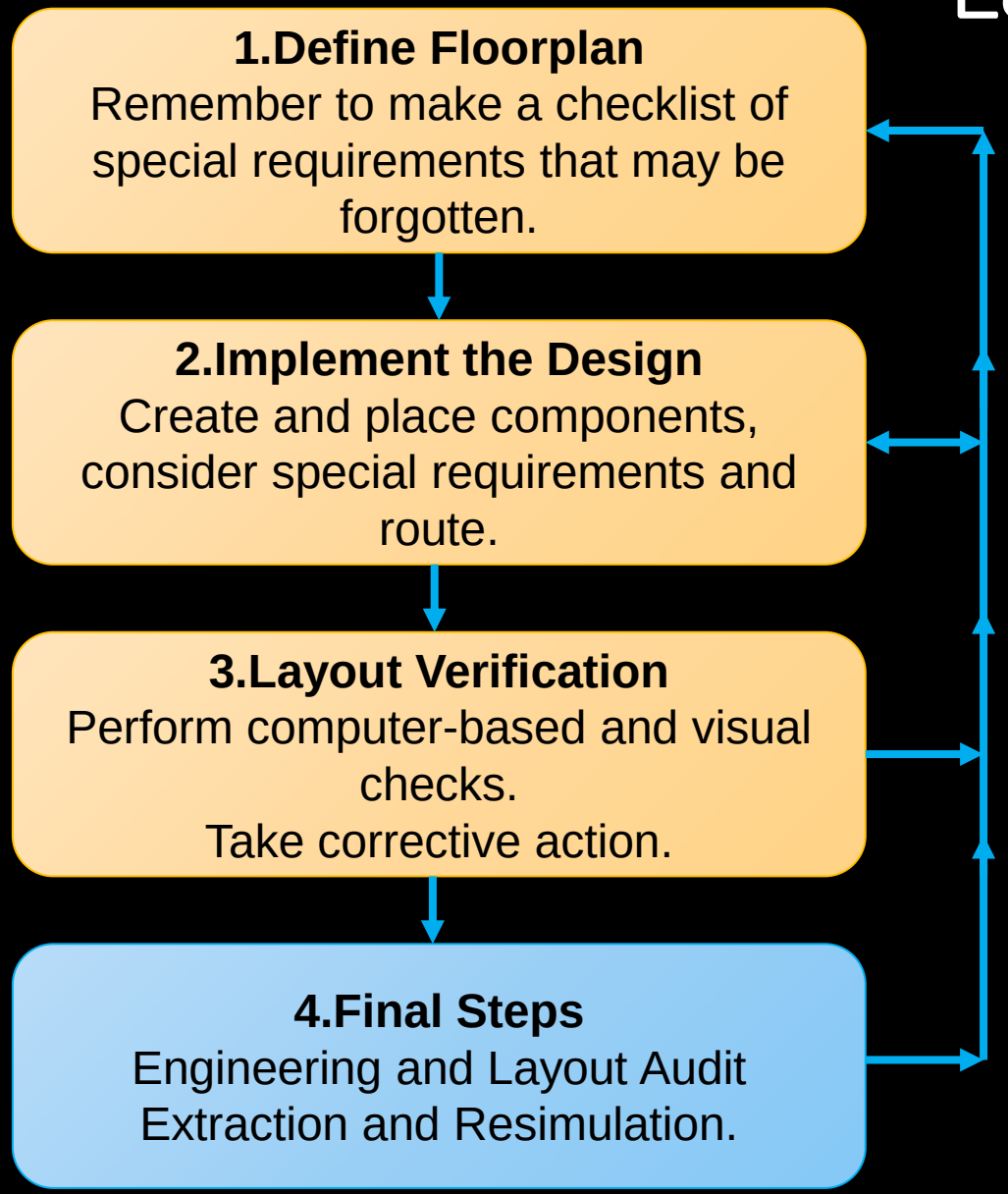
2. Audits:

- At this level audits have to be performed by an experienced person who has already passed through one or more tape-outs.
- As a baseline check, the layout designer can use the checklist provided earlier, adding any company- and process related questions.
- The other important issue is to audit the newly placed keys that may not conform to the DRC command file.
- A very important task, that is sometimes forgotten, is to re-audit the design if the command files for DRC and LVS include verifications for layers that are not designed in layout but generated using CAD software before mask making.

3. Tape-out Procedures:

- When people talk about tape out procedures they are referring to the steps detailed above plus specific documentation sign offs and release procedures.
- For each chip released to the mask shop, there are internal company procedures that have to be followed.
- For example, the division management, together with the project leaders and the circuit and layout designers, should review all audit reports, additional company standard sign off procedures, and sign and release the tape and the accompanying documents and data.
- It is a good practice to take care that all the macros, documents, verification results, audit reports, and command files related to the chip that has been taped out are filed for easy access in future releases.

Layout design procedure



Plan your work!

Implement

Verify

Get a second opinion

LAYOUT CONSIDERATIONS DUE TO PROCESS CONSTRAINTS

Why Layout Considerations is important? We can understand with these points.

There are layout techniques that must be used to address limitations or effects to the circuitry as a result of the manufacturing process.

- **Design Rule Compliance:** Ensure strict adherence to design rules for minimum widths, spacing, and other geometrical constraints.
- **Manufacturing Variations:** Account for variations in manufacturing processes that can affect device parameters and performance.
- **Thermal Management:** Consider heat dissipation and thermal gradients to prevent overheating and reliability issues.

•**Electromigration:** Avoid excessive current densities to prevent metal migration and potential failures.

•**Noise Immunity:** Implement measures to reduce noise sensitivity and ensure reliable circuit operation.

•**Power Integrity:** Maintain adequate power distribution to avoid voltage drops and fluctuations.

•**Timing Constraints:** Ensure that the layout meets timing requirements, such as setup and hold times.

•**Floorplanning and Routing:** Optimize floorplan and routing to minimize congestion and improve performance.

•**Signal Integrity:** Consider signal integrity issues, such as crosstalk and ringing, to ensure proper signal transmission.

Why we use design rules?

Interface between designer and process engineer

- Historically, the process technology referred to the length of the silicon channel between the source and drain terminals in field effect transistors.
- The sizes of other features are generally derived as a ratio of the channel length, where some may be larger than the channel size and some smaller.
- For example, in a 90 nm process, the length of the channel may be 90nm, but the width of the gate terminal may be only 50 nm.

TYPES

- Two major approaches:
  - "**Micron**" rules: stated at micron resolution.
    - All minimum sizes and spacing specified in microns.
    - Rules don't have to be multiples of λ.
    - Can result in 50% reduction in area over λ based rules
  - λ rules: simplified micron rules with limited scaling attributes.

- Design rules represents a tolerance which insures very high probability of correct fabrication
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

“MICRON” RULES

Micron rules are a set of design rules used in the layout of integrated circuits (ICs). These rules specify the minimum feature sizes and spacing in absolute dimensions, typically in micrometers (µm). Here are some key points about micron rules:

1.N-well Rules:
1. Width: 3 µm
2. Space: 9 µm

2.Active Area Rules:
1. Minimum size: 3 µm
2. Minimum spacing: 3 µm
3. N+ active to N-well: 7 µm

3.Poly 1 Rules:
1. Width: 2 µm
2. Spacing: 3 µm
3. Gate overlap of active: 2 µm
4. Field poly 1 to active: 1 µm

4.Contact to Poly 1 Rules:
1. Exact contact size: 2 µm × 2 µm
2. Minimum poly overlap: 1 µm
3. Minimum contact spacing: 2 µm

5.Contact to Active Rules:
1. Exact contact size: 2 µm × 2 µm
2. Minimum active overlap: 1 µm
3. Minimum contact spacing: 2 µm
4. Minimum spacing to gate: 2 µm

6.Metal 1 Rules:
1. Width: 3 µm
2. Spacing: 3 µm
3. Overlap of contact: 1 µm
4. Overlap of via: 2 µm

7.Metal 2 Rules:
1. Width: 3 µm
2. Space: 3 µm
3. Metal 2 overlap of via: 2 µm

λ LAMBDA-BASED DESIGN RULES

- *Lambda-based* (scalable CMOS) design rules define scalable rules based on (which is half of the minimum channel length)
- Lambda-based design rules are a simplified and scalable approach to defining layout constraints in VLSI design. These rules use a single parameter, λ (lambda), to represent distances and dimensions, making it easier to scale designs across different manufacturing processes. Here are some key points about lambda-based design rules:

1.Minimum Feature Size:

1. The minimum feature size is defined as (2λ). For example, if the minimum feature size of a technology is 0.5 µm, then (λ) is 0.25 µm.

2.Width and Spacing:

1. Minimum width of polysilicon: (2λ)
2. Minimum spacing between polysilicon: (3λ)
3. Minimum width of metal: (3λ)
4. Minimum spacing between metal lines: (3λ)

3.Overlaps and Contacts:

1. Minimum overlap of polysilicon over diffusion: (1λ)
2. Minimum overlap of metal over contact: (1λ)
3. Minimum contact size: (2λ \times 2λ)
4. Minimum spacing between contacts: (2λ)

4.Layer-to-Layer Spacing:

1. Minimum spacing between polysilicon and metal: (2λ)
2. Minimum spacing between diffusion regions: (2λ)

Layout Design rules & Lambda (λ)

- **Lambda (λ) :** distance by which a geometrical feature or any one layer may stay from any other geometrical feature on the same layer or any other layer.

All processing factors are included plus a safety margin.

- λ is used to prevent IC manufacturing problems due to mask misalignment or exposure & development variations on every feature, which otherwise could lead to :

- over-diffusion
- over-etching
- inadvertent transistor creation etc

- λ is the minimum dimension which can be accurately re-produced on the silicon wafer for a particular technology.

- Minimum photolithographic dimension (width, not separation) is 2λ.
- Hence, the minimum channel length dimension is 2λ.
- Where a 0 25μm 0.25μm gate length is quoted, λ is 0.125 microns (μm).
- Minimum distance rules between device layers, e.g., are used during layout.
    - polysilicon ↔metal
    - metal ↔ metal
    - diffusion ↔ diffusion and
    - minimum layer overlaps
- Layout design rule checker (DRC) automatically verifies that no design rules have been broken.

Design Rules

Minimum Width and Spacing Rules

Layer	Type of Rule	Value
Poly	Minimum Width	2λ
	Minimum Spacing	2λ
Active	Minimum Width	3λ
	Minimum Spacing	3λ
NSelect	Minimum Width	3λ
	Minimum Spacing	3λ
PSelect	Minimum Width	3λ
	Minimum Spacing	3λ
Metal1	Minimum Width	3λ
	Minimum Spacing	3λ

Where $\lambda = 1\ \mu m$

Design Rules

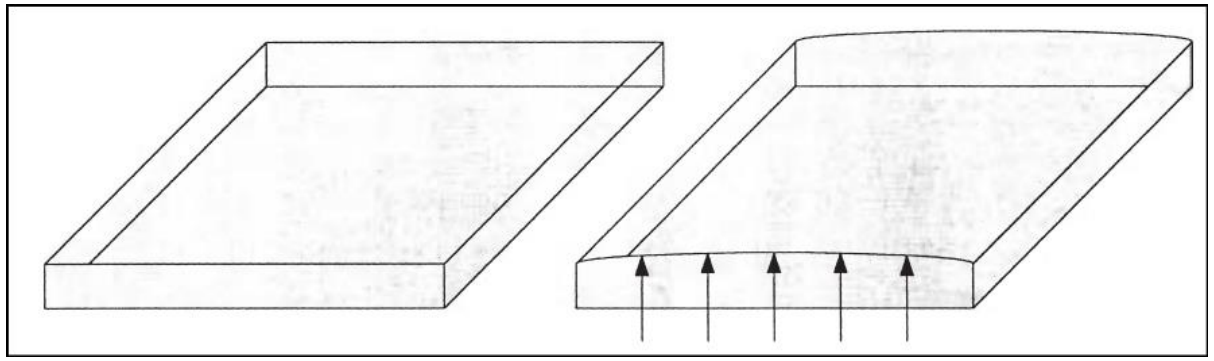
MOSFET Layout Rules

Rule	Meaning	Value
Poly Overlap	Minimum extension over ACTIVE	2λ
Poly-Active	Minimum Spacing	1λ
MOSFET Width	Minimum N+/P+ MOSFET W	3λ
Active Contact	Exact Size Minimum Space to ACTIVE Edge	2λ x 2λ | 2λ
Poly Contact	Exact Size Minimum Space to POLY Edge	2λ x 2λ | 2λ

Where λ = 1 μm

Wide metal slits

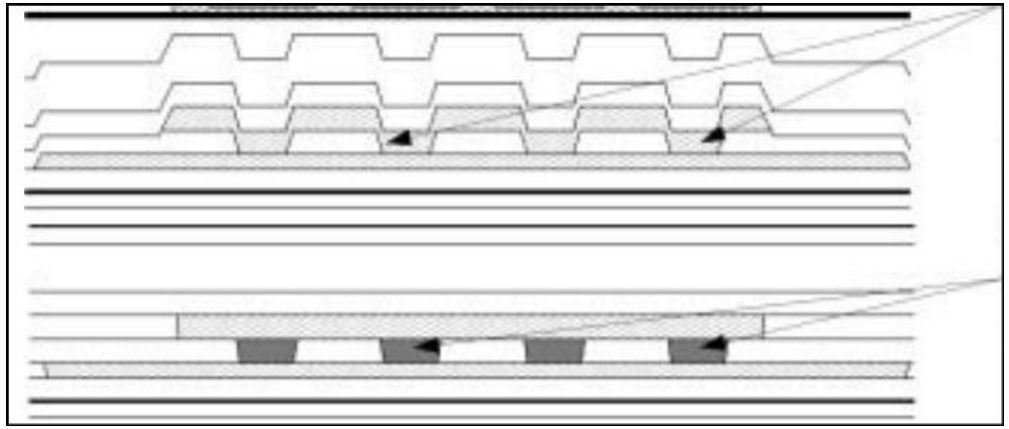
- Power supply lines in a chip are designed to be very wide so that electromigration and resistance effects are minimized.
- Are there maximum limits to the width of metal lines? In general the answer is no.
- However, there is one problem with very wide metal lines that occurs when the temperature of the chip rises high enough to cause the metal to expand significantly.
- As a result the expansion of the metal is in the center. This causes the center areas of the metal to expand upwards.



Metal expansion due to heat.

Large metal via implementations

- The vias are structures that lie directly in the current path between the two layers.
- Thus, the layout design of interlayer connections using vias should be well understood.
- It is most important in large metal lines because in general it is these lines that carry large currents.
- From a process point of view, vias are holes defined in the isolation layer between two layers: the top layer metal is required to fill the hole and connect to the lower layer.



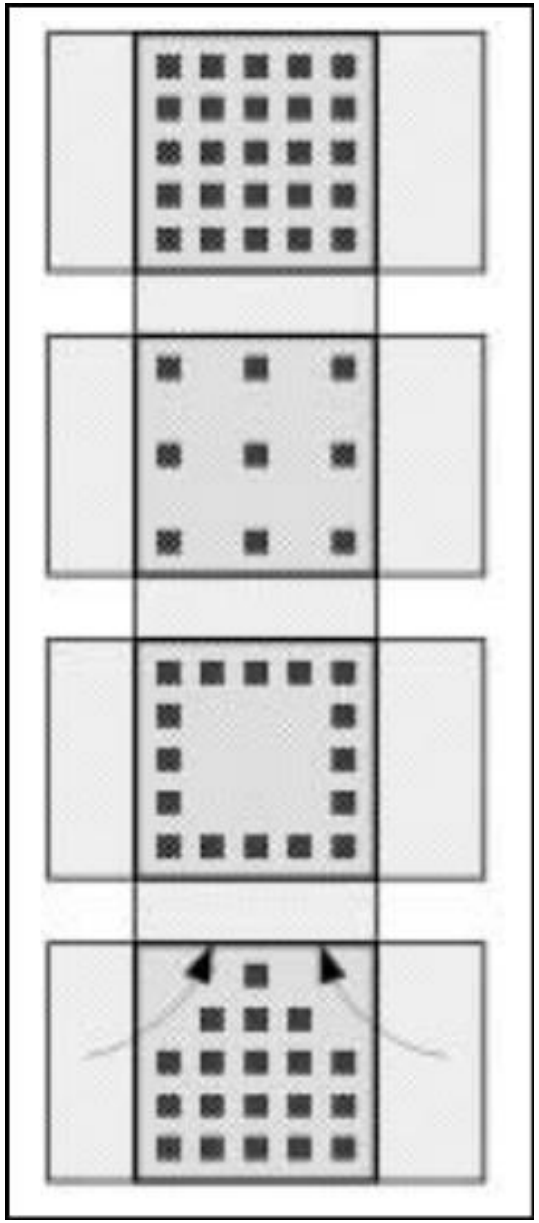
Cross-sectional view of via cuts.

Weaker Via:
Hole has angled sides, thus the connection to the lower layer is less than drawn.

Ideal Vias:
Hole is the same size as the via definition, so the connection is maximized.

Step coverage rules

- For each type of design, ASIC or DRAM, for example, the processes are very different, as we have already explained.
- Based on the purpose of the chip, market prices, design requirements, etc., companies are developing special processes.
- The variety of design rules for each of these processes continues to evolve.
- Layout designers are not involved in processing, but they have to take measures to prevent possible problems during the chemical and physical processing of the wafer.
- One problem that can be addressed with proper layout design techniques is the step coverage effect.



- **Fully Contacted Area**
- Maximum number of vias
- Minimum distance between them

- **Fully Contacted Area**
- Not maximum number of vias
- Relaxed distance between them

- **Only Ring Contacted Area**
- Not maximum number of vias
- Relaxed distance between them

- **T Junction (Current Flow)**
- Not maximum number of vias
- Minimum distance between them

VIA ARRAY CONFIGURATIONS FOR CIRCUIT PERFORMANCE

Multiple rule sets

- When working with ASIC processes, designers benefit from a relatively simple set of design rules compared to those used in DRAM or embedded memory processes.
- Here are some key points about why memory processes have significantly different rules and how multiple rule sets are managed:

1. Memory Cell Complexity:

1. Memory cells occupy 50-70% of the chip area.
2. They have unique rules and specialized layers.

2. Defining Design Rules:

1. Involves trade-offs among price, size, complexity, and reliability.
2. Collaboration between designers, layout experts, and process engineers is essential.

3. **DRAM Memory Rule Sets**:
    1) **Memory Cells**: Specific rules for densely packed cells.
    2) **Pitch-Related Logic**: Rules for logic interfacing with memory cells.
    3) **Periphery Layout**: Rules for areas outside the memory array, similar to ASIC rules.

4. **DRC Verification**:
    1. Layouts must be designed to verify different rule sets using DRC tools.
    2. Identifying areas for specific rule checks is crucial.

This ensures the design meets functionality and manufacturability criteria while maintaining reliability.

Antenna rules

- A side effect of the manufacturing process that leads to damaged parts is known as the **antenna effect**.
- Under certain conditions, plasma etchers or ion implanters induce charge onto various structures that connect to a gate of a transistor.
- The induced charge threatens to overstress and irreparably damage the thin gate oxides of the transistor, causing unreliable operation.

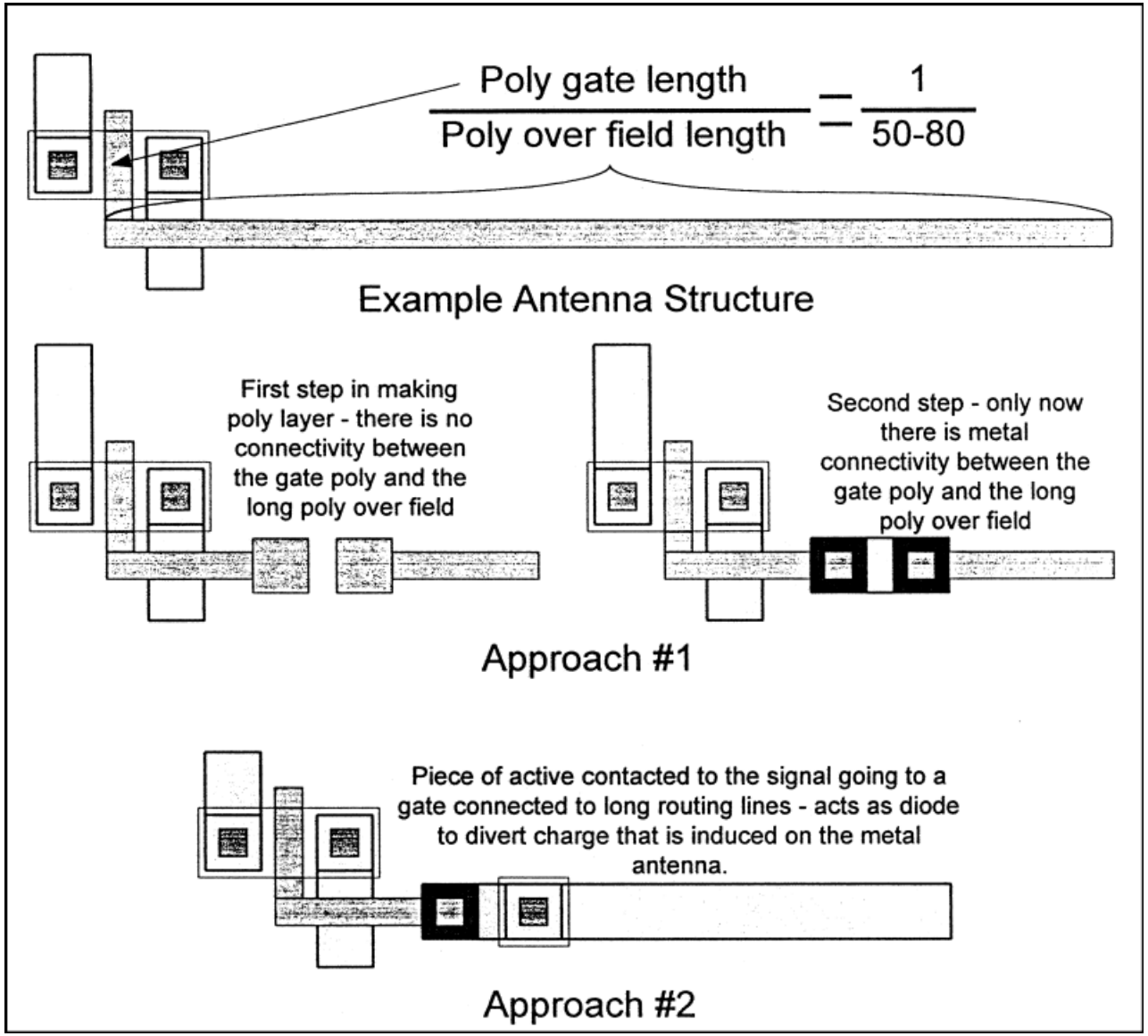
During the manufacturing process, charge can be induced if a structure acts like an antenna. This is particularly problematic as gate sizes shrink and more metals are added to chips, increasing the impact of the antenna effect on wafer yield.

Here are two approaches to mitigate this effect:

1.Breaking Up Long Poly

2.Using Diodes

ANTENNA RULES EXAMPLE AND SOLUTION



Special Design Rules

- In previous slides we learned the basics about process order flow and design rules related to process and circuit requirements.
- However, there are a few interesting exceptions to “general” design rules.

1. **Minimum Area Rule** : A rule that becomes more prevalent as geometry get smaller is the “minimum area” layer rule. Although design rules such as transistor gate length are shrinking, not all of the many layers in the manufacturing process shrink equally. One example of this is the definition of active areas, especially for small polygons. This limitation is typically specified as a minimum width and area
2. End Overlap Rule
3. Double Contacts

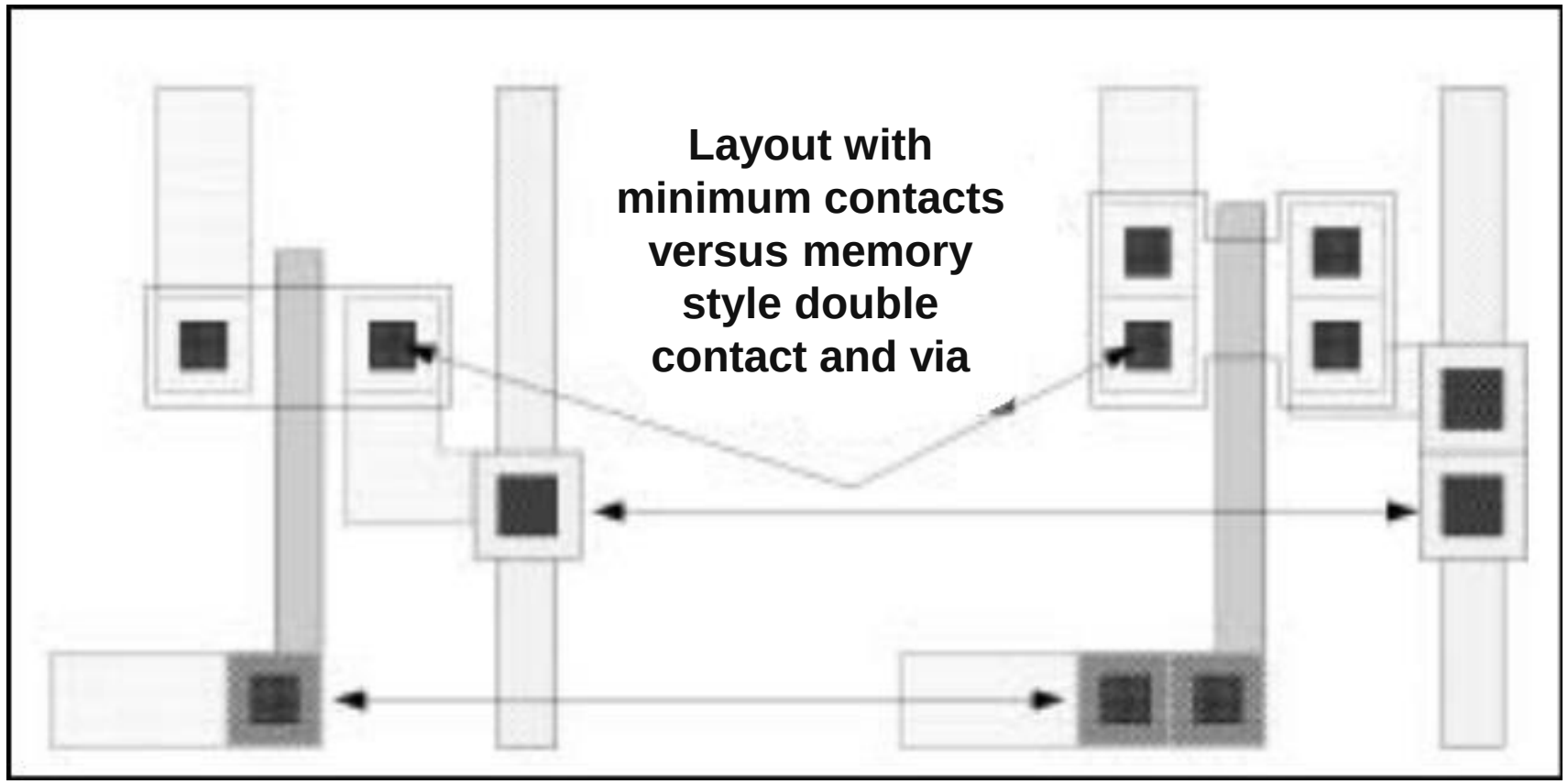
1. Minimum Area Rule
2. **End Overlap Rule :** We learned about a generic contact overlap rule in previous slides, but in some processes this rule is enhanced by a rule known as the **“end overlap”** rule.

- This rule applies when a contact is located at the very end of a line.
- Contacts that are placed at the very end of a line are in danger of not being filled as the metal is rounded in real silicon.
- This danger is increased if any amount of misalignment occurs during processing.

3. **Double Contacts :** Outside of the memory array, where the topology of the layout is not regular, more stringent design rules are enforced.

- One of these is the requirement for double contact and vias for every connection.
- This rule applies to transistor layout and general routing and signal connections.
- The double contact and/or double via not only improves the resistance of the connection; more importantly, it provides added reliability by having redundant contacts for every connection.

SINGLE AND DOUBLE CONTACT DESIGN STYLES



Latch-Up

- Conceptually, latch-up refers to the state of an IC when it is made inoperable by a parasitic shorting of VDD to VSS.
- Depending on the severity of the latch-up condition, the IC may be irreversibly damaged, or it may recover only after a complete power shutdown.

In summary, here are the very simple requirements for latch-up to occur that we have discussed:

- A large enough VBE generated (at least temporarily) to activate either bipolar transistor.
- This requires the combination of an abnormal current injected into the chip and parasitic resistance values large enough to generate this voltage difference by Ohm's law.
- Parasitic bipolar transistors of sufficient current drive strength to sustain the required VBE to keep the bipolar transistors on.
- **Latch-up** is a phenomenon that is well understood, as it has a long history in CMOS IC design. Many guidelines and design rules have been developed that inherently reduce the risk of latch-up and minimize the likelihood of meeting the requirements just listed.

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Thank You