1. I/O to Verilog Module:

   i. Reset : to reset the module (active low)

   ii. Reset1 : to be used for asynchronous reset from the Zynq processor

   iii. Clk : Clock from the Zynq System

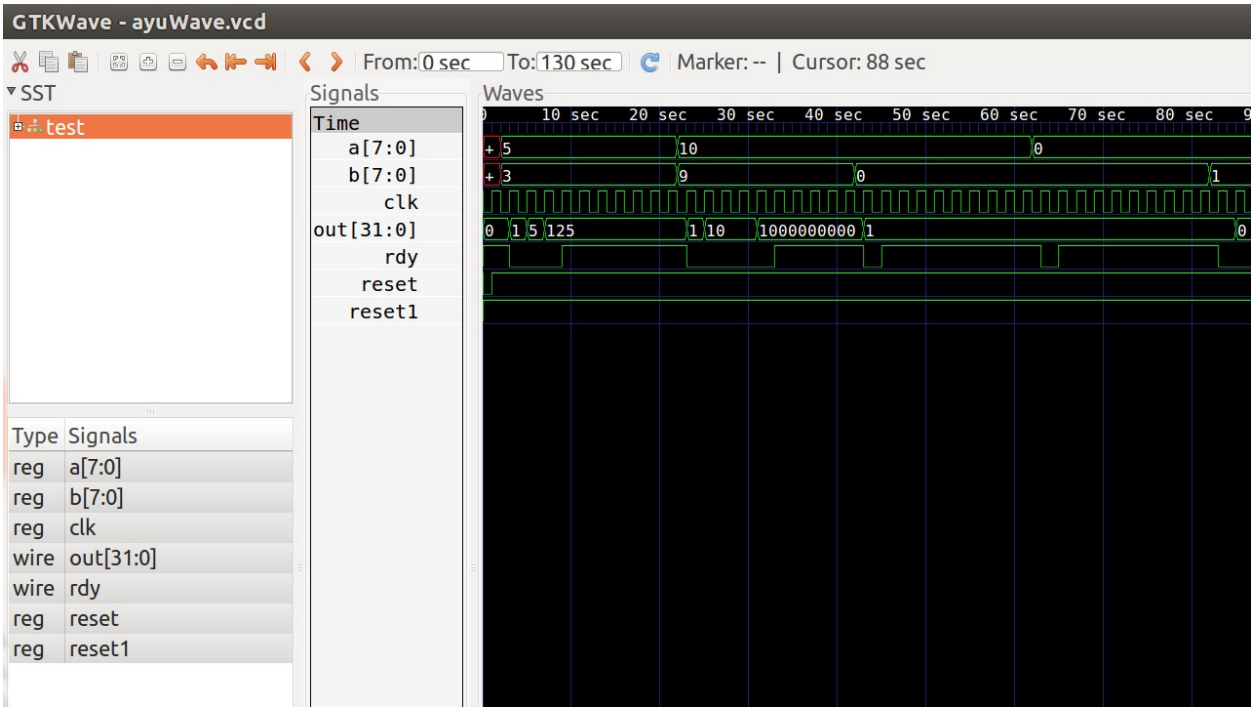
   iv. 8 bit a : First input to be taken as ‘x’ in x^n

   v. 8 bit b : Second input to be taken as ‘n’ in x^n

   vi. 32 bit out : The output Result

   vii. Ready : To check if computation is over and module is idle

2. Simulation Results :



3. Simulation Steps:

   Iverilog testbench.v q1.v

   Vvp a.out

   Gtkwave ayuWave.vcd