

VLSI ARCHITECTURE – 1
ASSIGNMENT – 1

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1.) 8 Tap Fir Filter Using Matlab

Code

```
function [y_out] = filter_func(data)

persistent b1 b2 b3 b4 b5 b6 b7 b8;
if (isempty(b1))
    b1 = 0;b2=0;b3=0;b4=0;b5=0;b6=0;b7=0;b8=0;
end

h = [-0.1 -0.08 0.2 0.4];

a1 = b1 + b8;
a2 = b2 + b7;
a3 = b3 + b6;
a4 = b4 + b5;

y_out = a1 * h(1) + a2 * h(2) + a3*h(3)+ a4 * h(4);

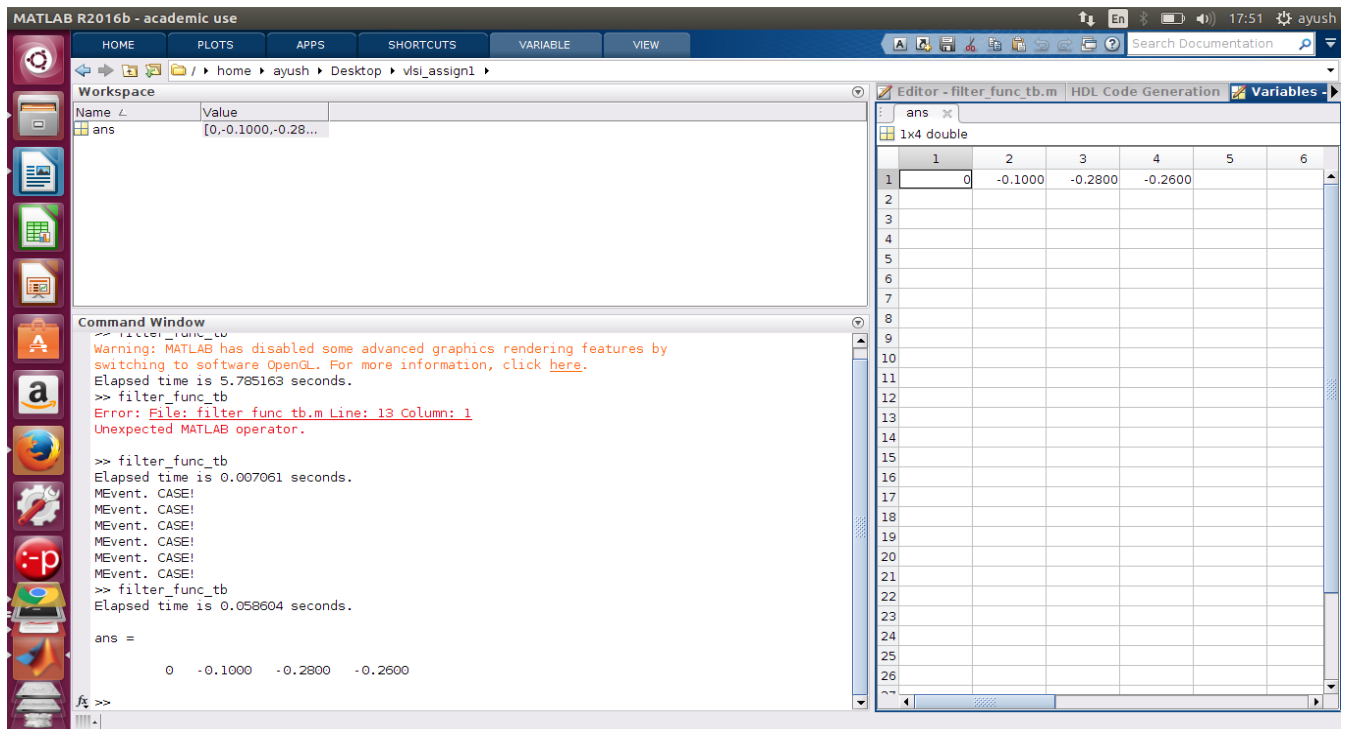
b8 = b7;
b7 = b6;
b6 = b5;
b5 = b4;
b4 = b3;
b3 = b2;
b2 = b1;
b1 = data;

end
```

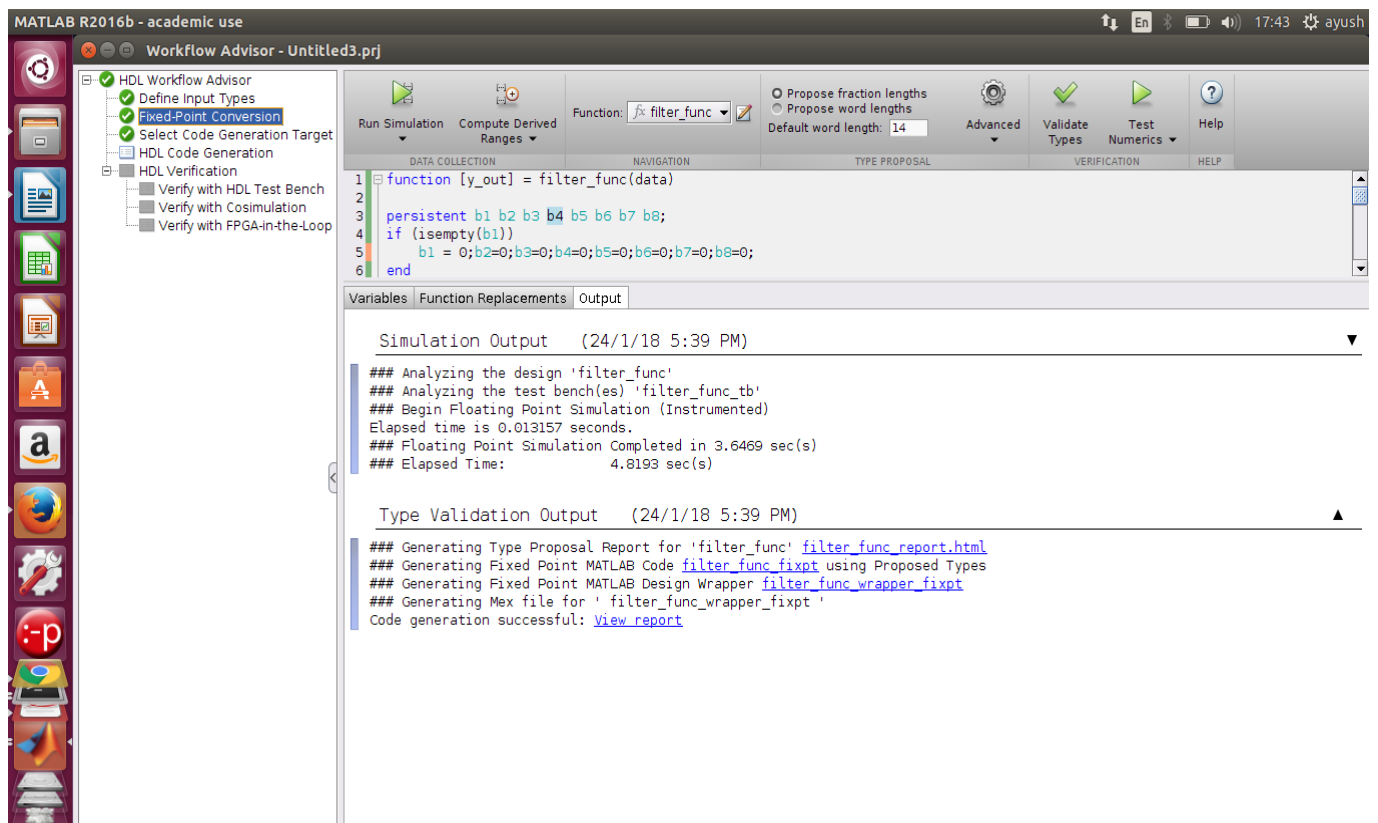
Testbench -

```
function [y_out] = filter_func_tb()
clear all;
close all;
tic;
%t := rtime()/1000
x_in = [1 2 3 4];
len = length(x_in);
y_out = zeros(1,len);
for ii=1:len
    [y_out(ii)] = filter_func(x_in(ii));
end
toc;
%%plot(1:len,y_out);
end
```

Output – [0 -0.100 -0.2800 -0.2600]



Performance



Adders/ Multipliers used

Web Browser - HDL Resource Utilization Report for 'filter_func_fixpt'

HDL Resource Utilization Report for 'filter_func_fixpt' x +

Location: file:///home/ayush/Desktop/Msi_assign1/codegen/filter_func/hdlsrc/resource_report.html

HDL Resource Utilization Report ('filter_func_fixpt')

Generated on 2018-01-23 15:29:50

Summary

Multipliers	2
Adders/Subtractors	6
Registers	8
Total 1 Bit Registers	12
RAMs	0
Multiplexers	2
I/O Bits	21
Shifters	0

Multipliers (2)

- 3x14-bit Multipliers : 2

Adders/Subtractors (6)

- 4x4-bit Adder : 1
- 3x3-bit Adders : 2
- 17x17-bit Adder : 1
- 18x18-bit Adder : 1
- 19x19-bit Adder : 1

Registers (8)

- 3-bit Register : 1

Web Browser - HDL Resource Utilization Report for 'filter_func_fixpt'

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Adders/Subtractors (6)

- 4x4-bit Adder : 1
- 3x3-bit Adders : 2
- 17x17-bit Adder : 1
- 18x18-bit Adder : 1
- 19x19-bit Adder : 1

Registers (8)

- 3-bit Register : 1
- 2-bit Registers : 2
- 1-bit Registers : 5

Flipflops (12)

- Total 1-Bit Registers 12

Multiplexers (2)

- 14-bit 2-to-1 Multiplexer : 2

I/O Bits (21)

Input Bits (6)

- clk : 1 bit
- reset : 1 bit
- clk_enable : 1 bit
- data : 3 bits

Output Bits (15)

- ce_out : 1 bit
- y_out : 14 bits

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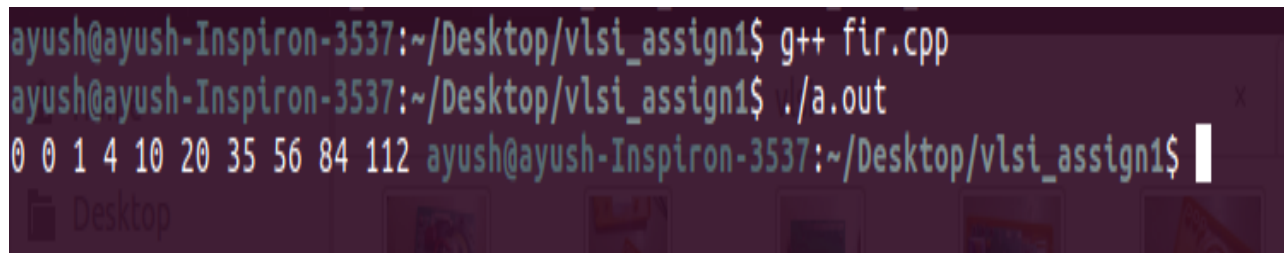
Cost will be around Rs 20 – 25.

2.) C - Code

```
#include<bits/stdc++.h>
typedef long long int lli;
using namespace std;
int main()
{
    lli i,j,sum;
    lli arr[10];
    lli h[8];
    lli ans[10];
    for(i=0;i<10;i++)
        arr[i] = i;
    for(i=0;i<8;i++)
        h[i] = i;
    for(i=0;i<10;i++)
    {
        sum = 0;
        for(j=0;j<=i;j++)
        {
            sum += arr[j]*h[i-j];
        }
        ans[i] = sum;
    }
    for(i=0;i<10;i++)
        cout<<ans[i]<<" ";

    return 0;
}
```

Output -



```
ayush@ayush-Inspiron-3537:~/Desktop/vlsi_assign1$ g++ fir.cpp
ayush@ayush-Inspiron-3537:~/Desktop/vlsi_assign1$ ./a.out
0 0 1 4 10 20 35 56 84 112 ayush@ayush-Inspiron-3537:~/Desktop/vlsi_assign1$
```

3.) Fir filter using verilog

code -

```
module dff(x,clock,out,reset);
input reset;
input [7:0]x;
input clock;
output [7:0]out;
reg out;
always @(posedge clock)
begin
    if(reset==1)
    begin
        out <= 0;
    end
    else
    begin
        out <= x;
    end
end
endmodule
```

```
module firfilter(x,clock,outvalue,reset);
input [7:0]x;
input clock,reset;
output [15:0]outvalue;
//reg outvalue;
wire [7:0] d11;
wire [7:0] d12,d13,d14,d15,d16,d17,d18;
wire [15:0] m1,m2,m3,m4,m5,m6,m7,m8;
wire [15:0] sum1,sum2,sum3,sum4,sum5,sum6;
parameter h1=4'b0001;
parameter h2=4'b0010;
parameter h3=4'b0011;
parameter h4=4'b0100;
parameter h5=4'b0101;
parameter h6=4'b0110;
parameter h7=4'b0111;
parameter h8=4'b1000;
dff d1(x,clock,d11,reset);
dff d2(d11,clock,d12,reset);
dff d3(d12,clock,d13,reset);
dff d4(d13,clock,d14,reset);
dff d5(d14,clock,d15,reset);
dff d6(d15,clock,d16,reset);
dff d7(d16,clock,d17,reset);
dff d8(d17,clock,d18,reset);
assign m1 = d11>>h1;
```

```

assign m2 = d12>>h2;
assign sum1 = m1+m2;
assign m3 = d13>>h3;
assign sum2 = sum1 + m3;
assign m4 = d14>>h4;
assign sum3 = sum2 + m4;
assign m5 = d15>>h5;
assign sum4 = sum3+m5;
assign m6 = d16>>h6;
assign sum5 = sum4+m6;
assign m7 = d17>>h7;
assign sum6 = sum5+m7;
assign m8 = d18>>h8;
assign outvalue = m8+sum6;
//initial begin
//$monitor("time=%d m1=%d m2=%d m3=%d", $time,d11,d12,d13);
//end
endmodule

```

Test bench -

```

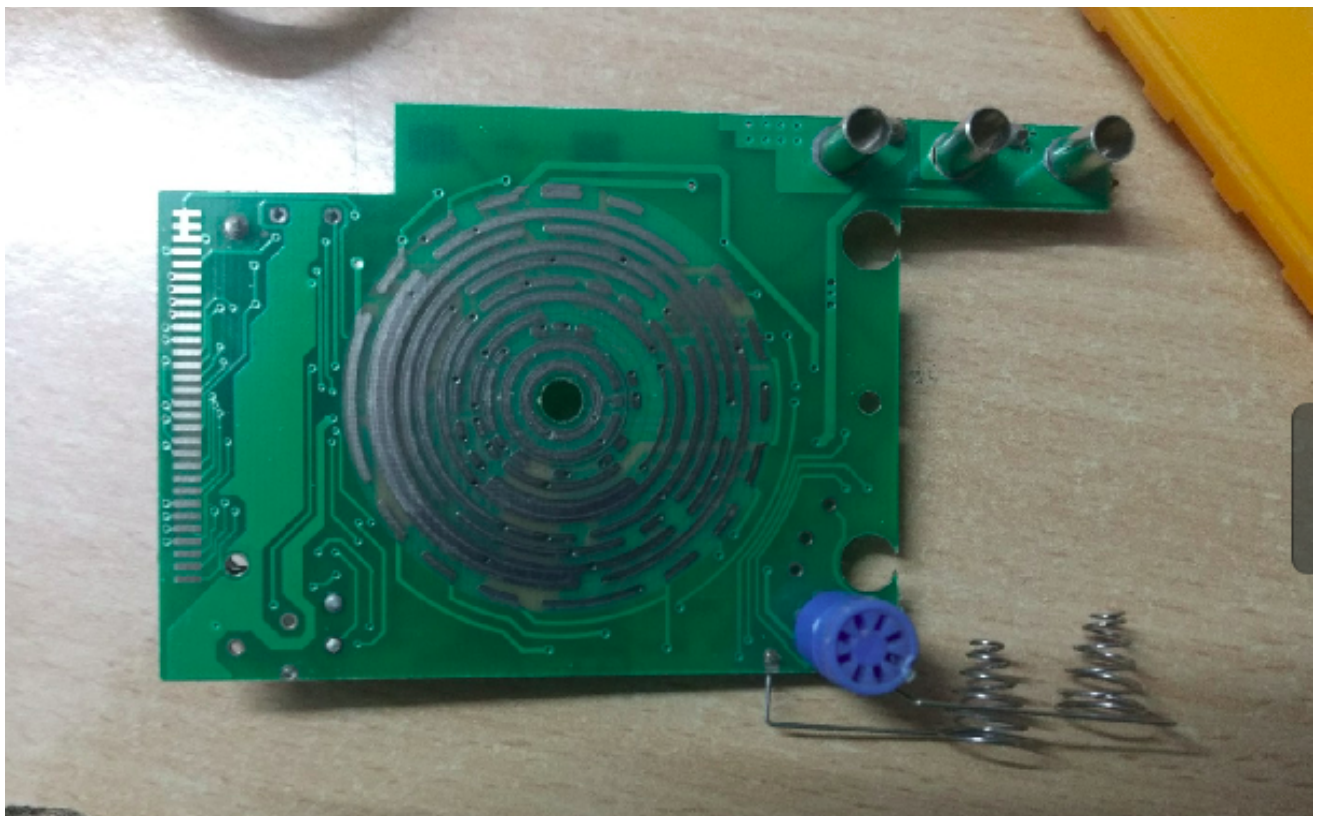
module test;
reg reset;
reg [7:0]x;
reg clock;
wire [15:0]out;
firfilter f1(x,clock,out,reset);
always
begin
    #10 clock <= ~clock;
end
initial
begin
    clock = 1;reset = 1;
    $monitor("time=%d input=%d output=%d", $time,x,out);
    #20 reset=0;x= 4 ;
    #20 x = 2 ;
    #20 x = 6 ;
    #20 x = 10 ;
end
endmodule

```

Output-

```
ayush@ayush-Inspiron-3537: ~/verilog/vlsi_assign
ayush@ayush-Inspiron-3537:~/verilog/vlsi_assign$ ls
a.out  dflipflop.v  df.v  out  tes.v
ayush@ayush-Inspiron-3537:~/verilog/vlsi_assign$ iverilog -o out dflipflop.v
ayush@ayush-Inspiron-3537:~/verilog/vlsi_assign$ vvp out
time=0 input= x output= 0
time=20 input= 4 output= 2
time=40 input= 2 output= 2
time=60 input= 6 output= 3
time=80 input= 10 output= 6
time=100 input= 10 output= 7
time=120 input= 10 output= 8
```

4.) Multimeter







Parts-

HFE – Hybrid parameter forward current gain, common emitter which measures the DC gain of a junction transistor. So it indicates a mode where the meter can measure, the HFE of a transistor.

Resistors – Around 22 resistors are used

8*1 lcd display

9 volts Dc battery

Capacitors

Ic – 7107 - Its a high performance, low power, 3.5 digit A/D converters. It includes seven segment decoders, display drivers, a reference and a clock. It is also designed to interface liquid crystal display(LCD) and includes a multiplexed backplane drive. It can directly drive an instrument size light emitting diode(LED) display

Small speaker – For denoting if there is any short circuit. It checks whether voltage on both sensors are same.

Voltage Regulator – Which converts 9V to 5V Dc.

Cost Calculation -

HFE – Around Rs 15.

Small speaker – It costs around Rs 8-10.

9 volts DC battery - Rs 20

Around 20 registers of range from 100 ohms to 10K ohms and capacitors – Rs 10

IC 7107 which costs around Rs 20.

Total Cost of Multimeter would be around Rs 80-85 of quality which normally cost around Rs 130-140 in market.