CS330 - Quiz 2

Total: 15 marks Duration: 20 mins

open books and notes, no mobile phones, friends disconnected during exam

Be precise, no marks for vague answers

Roll No:

Q1. Select the correct answer(s) for the following questions. No partial marks. (2×4)

(i) Which of the following statement(s) are true in virtual memory system with paging?

(a) Address of a variable in a program, if printed every time the program executes, *can be* same.

(b) Address of a variable in a program, if printed every time the program executes, *can be* different.

(c) Address of a variable *can be* changed by the OS during program execution.

(d) Address of a library function (e.g., printf), if printed by two applications, *can be* same.

(e) Address of a library function (e.g., printf), if printed by two applications, *can be* different.

Ans: a, b, d, e

(ii) In which of the following scenario(s), a page fault can occur?

(a) accessing a general purpose register like `RAX`

(b) executing a JMP (jump) instruction

(c) decrementing an unsigned integer value stored in a register beyond zero

(d) returning from a function

(e) writing to an allocated and accessed variable

Ans: b, d, e

(iii) Which of the following statement(s) are true?

(a) A superuser (e.g., root user in Unix) can execute all privileged instructions.

(b) If OS accesses a virtual address which is not mapped in the OS page tables, system will crash.

(c) If OS accesses a virtual address which is not mapped in the OS page tables, a page fault will occur.

(d) The OS page fault handler *may* terminate a process.

(e) The OS page fault handler *must* invoke swapping.

Ans: c, d

(iv) Which of the following statement(s) are true?

(a) For a TLB without ASID support, a full TLB flush is *always* required when switching between two applications

(b) For TLB without ASID support, a full TLB flush is *always* required on user to OS switch

(c) If the OS updates a page table entry, it must flush the corresponding TLB entry from the TLB (with ASID support)

(d) If the OS updates a page table entry, it must flush the corresponding TLB entry from the TLB (without ASID support)

(e) If OS swaps out a page, it must flush the corresponding TLB entry

Ans: a, c, d, e

Q2. Consider a paging system with 48-bit virtual address, 4-level page tables and page size of 4KB. At each level, 9-bits of virtual address are used to index into the page table entry location. An application allocates total 1GB of virtual address by allocating 4K aligned random and distinct virtual pages. Considering all the virtual addresses are mapped to physical addresses, calculate the best case and worst case memory usage (in KB) to maintain the page tables for this application. (1×7)

Ans:

L4 (9bits), L3 (9bits), L2 (9bits), L1 (9bits), page offset (12bits)
Virtual address size = 1GB = 2^{18} pages
$\Rightarrow$ # of entries required at L1 = 2^{18}

Best case (3 Marks)
L1: 2^{18} entries require 2^9 page table pages
L2: 2^9 entries require 1 page table page
L3: 1 entry require 1 page table page
L4: 1 entry require 1 page table page
Total page table memory = $(2^9 + 1 + 1 + 1) \times 4$ KB

Worst case (4 Marks)
L1: 2^{18} entries can be spread across 2^{18} different page table pages (max. page table pages = 2^{27})
L2: 2^{18} entries can be spread across 2^{18} different page table pages (max. page table pages = 2^{18})
L3: 2^{18} entries can be spread across 2^9 different page table pages (max. page table pages = 2^9)
L4: 2^9 entries require 1 page table page (max. page table page = 1)
Total page table memory = $(2^{18} + 2^{18} + 2^9 + 1) \times 4$ KB