Microprocessors and Interfacing

CS/EEE-F241

Design project on,

FUNCTION GENERATOR

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ACKNOWLEDGEMENTS

This project was not an individual effort but a group effort, and by group we not only mean the four team members, but all those people who helped us move forward, even if it was by an inch. Thus, we would like to thank the following persons:

a. Prof. KR Anupama, for giving us the opportunity to do this project, and for providing help in the form of various online resources like on the website https://www.edge.edx.org and providing educational videos that added greatly to our knowledge.
b. Instructor, Meetha V. Shenoy, who in the course of discoursing tutorials, taught us numerous techniques in reference to the various devices used in the project.
c. Our mentor, Rajalakshmi Kishore, who helped us all along the way, and pointed us in the general direction to work in.
d. The Goa campus of BITS Pilani, for providing us with resources like the library and the internet.
e. All the people that contributed in whichever way possible, to this project.

HARDWARE USED

1.	8086 MICROPROCESSOR	1 unit
2.	555 clock generator	1 unit
3	8284 P-clock Generator	1 unit
4.	8255	1 unit
5.	8253	1 unit
6.	2 KB RAM 6116	2 unit
7.	4 KB ROM 2732	4 units
8.	DAC 0830	1 unit
9.	OPAMP 741	1 unit
10.	74LS138	1 units

ASSUMPTIONS

1. User has to first press a function key (sine, triangle or square), then the frequency keys, then the amplitude key to enable the 1V key followed by the 1V key presses and then Generate key.
2. Look up tables are used to generate Sine, Triangle, and Square wave-forms.
3. If the user forgets to enter sine, triangle or square wave by default sin wave will be produced.
4. The jumps for each ISR to corresponding delay function are a near jump.
5. The clock given to 8253 is 90 KHz .
6. Addressing used in memory interfacing is incremental addressing.

MEMORY INTERFACING

Two 6116 2KB RAM chips and two 2732 4kB ROM chips. Here memory of the last locations is folded back to ROM. It is done because of the fact that the microprocessor executes instructions at memory location FFFF0h (which is a jump instruction), when reset.

ROM1 (00000-01fff)

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

RAM1 (02000-02fff)

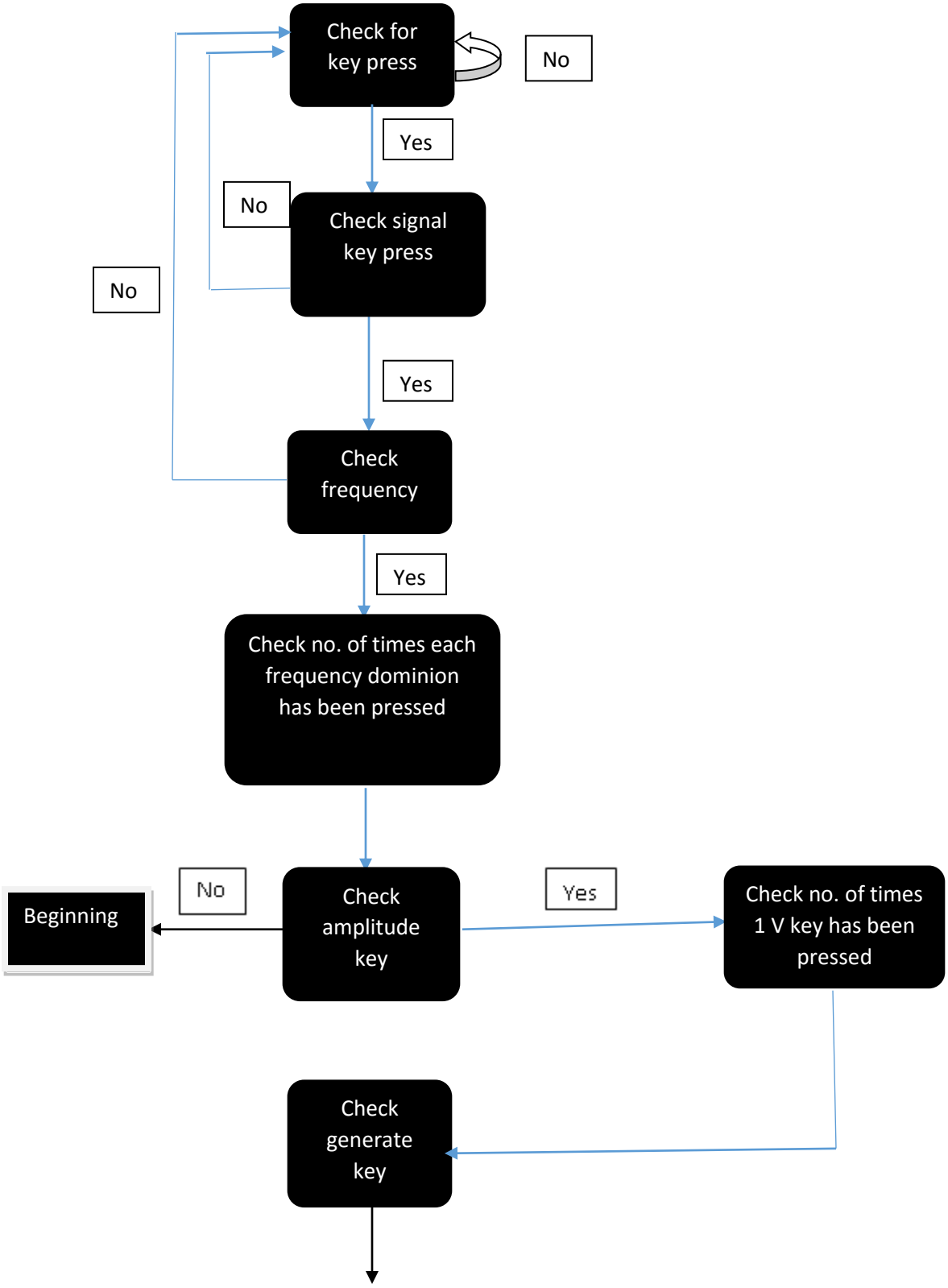
A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1

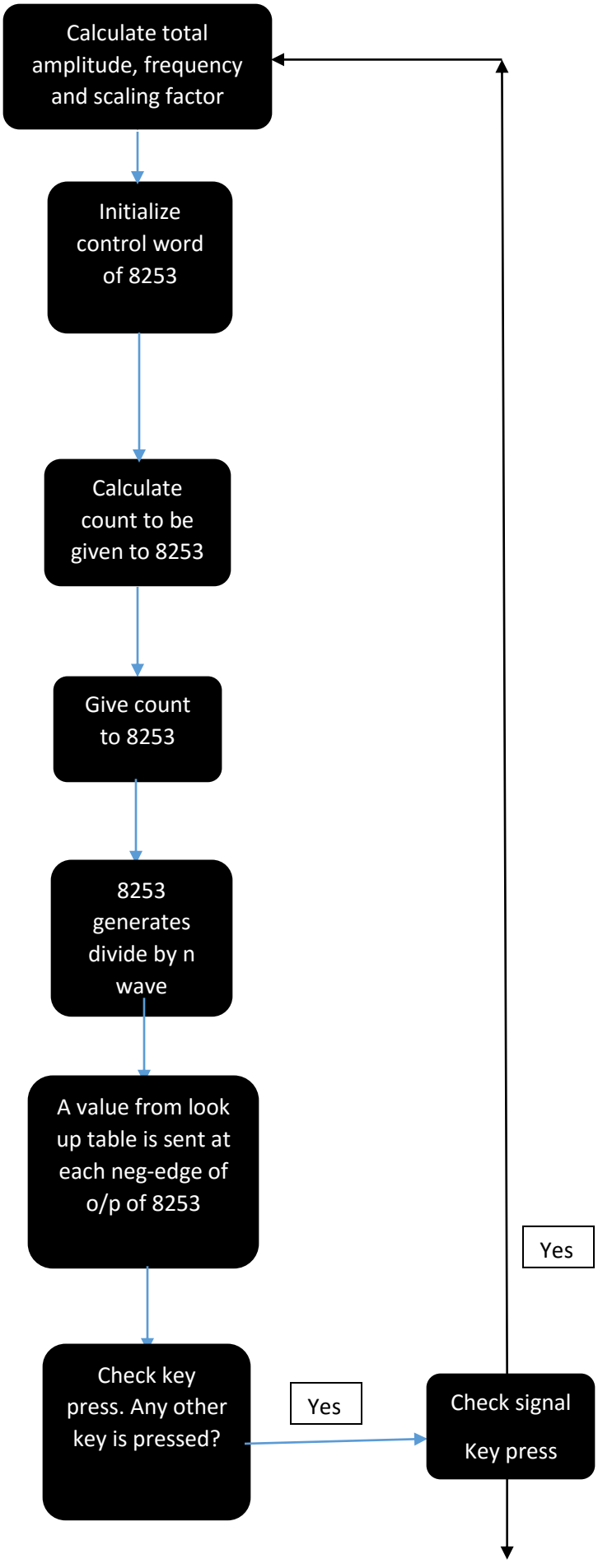
2 (FE000-FFFFF)

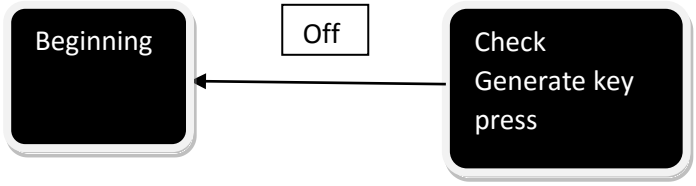
ROM

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Flowchart

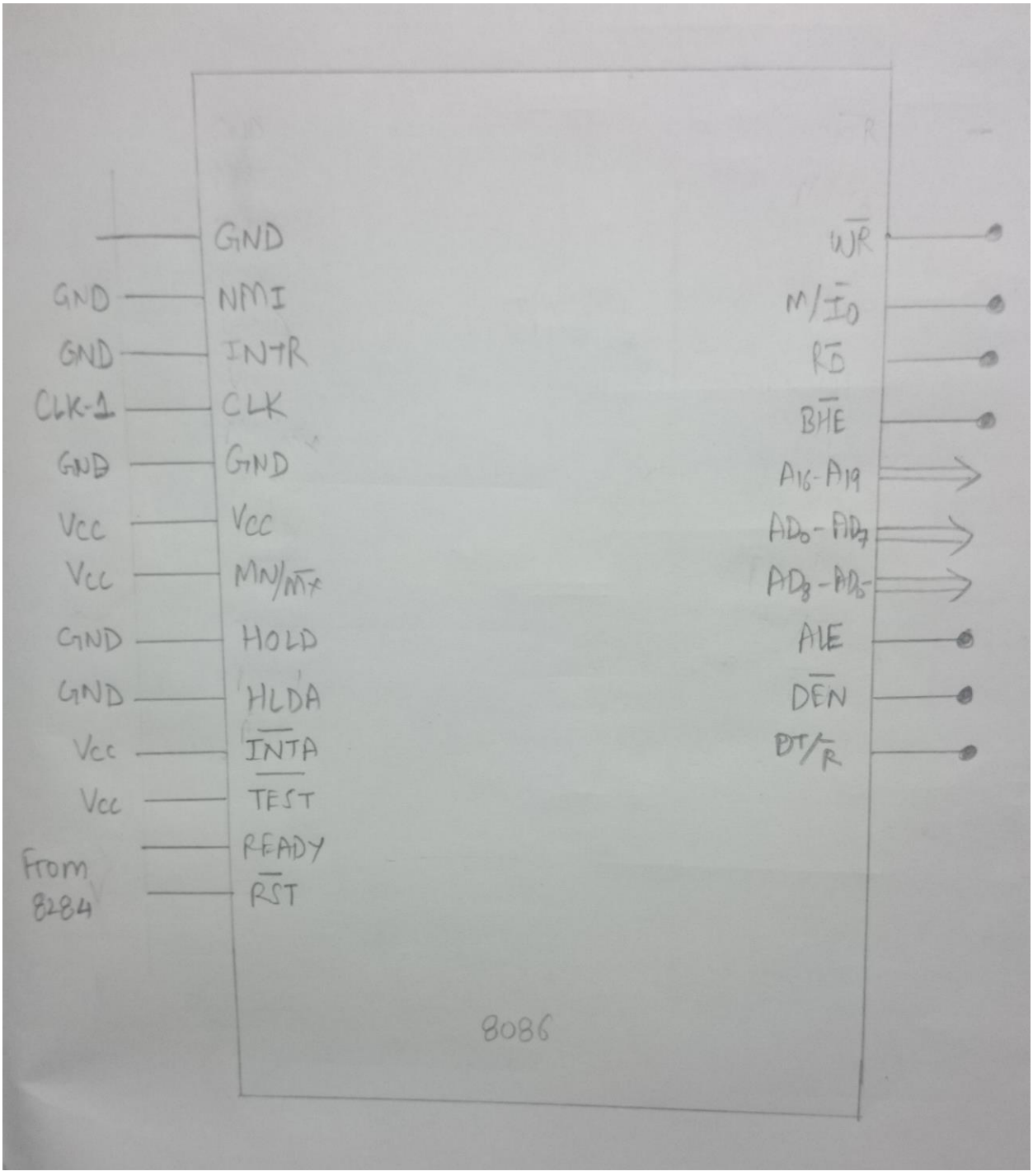

Check for key press
No
Yes
No
Check signal key press
No
Yes
Check frequency
Yes
Check no. of times each frequency dominion has been pressed
Beginning
No
Check amplitude key
Yes
Check no. of times 1 V key has been pressed
Check generate key

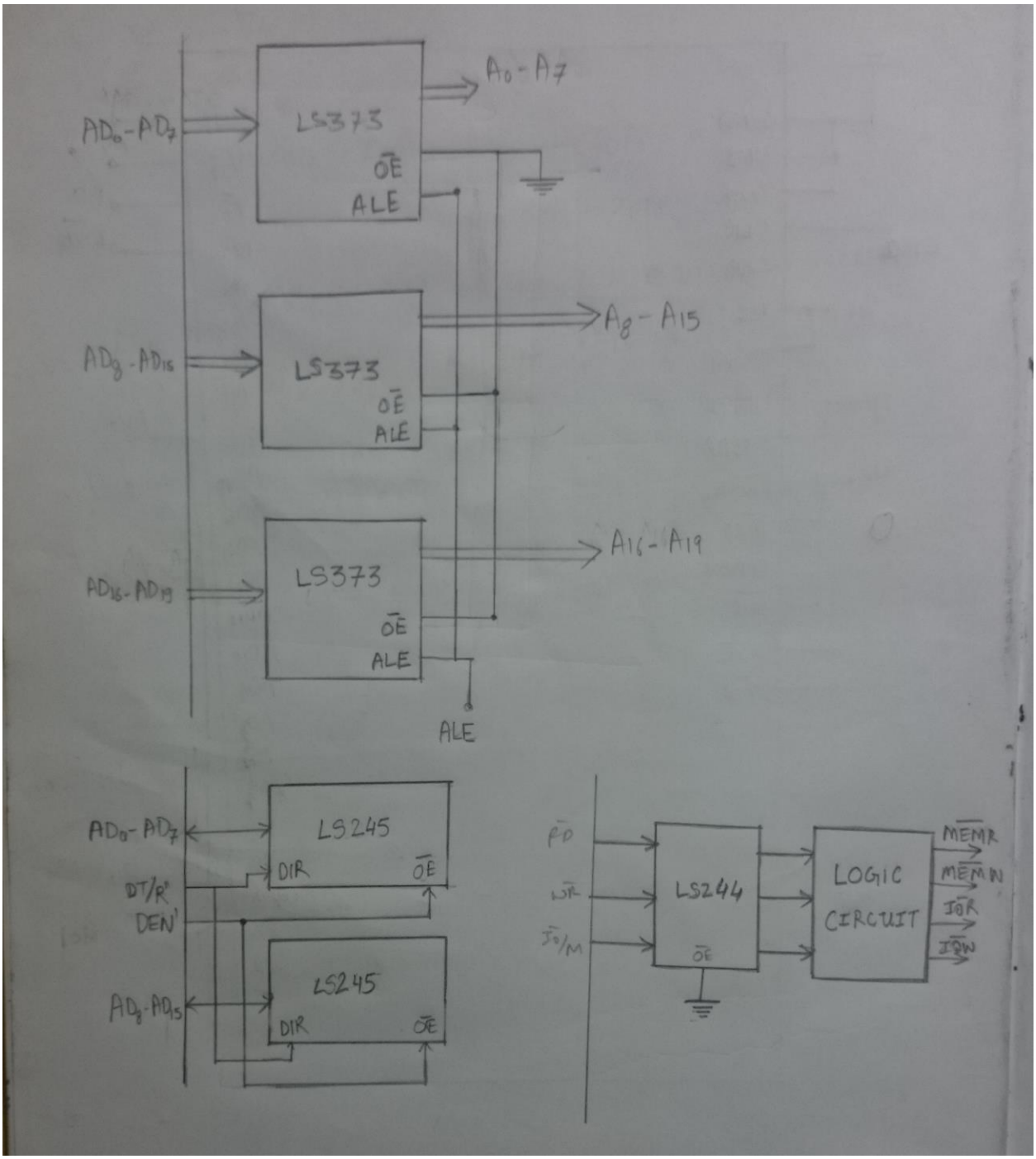

Calculate total amplitude, frequency and scaling factor
Initialize control word of 8253
Calculate count to be given to 8253
Give count to 8253
8253 generates divide by n wave
A value from look up table is sent at each neg-edge of o/p of 8253
Check key press. Any other key is pressed?
Yes
Check signal
Key press
Yes


Beginning
Off
Check
Generate key
press

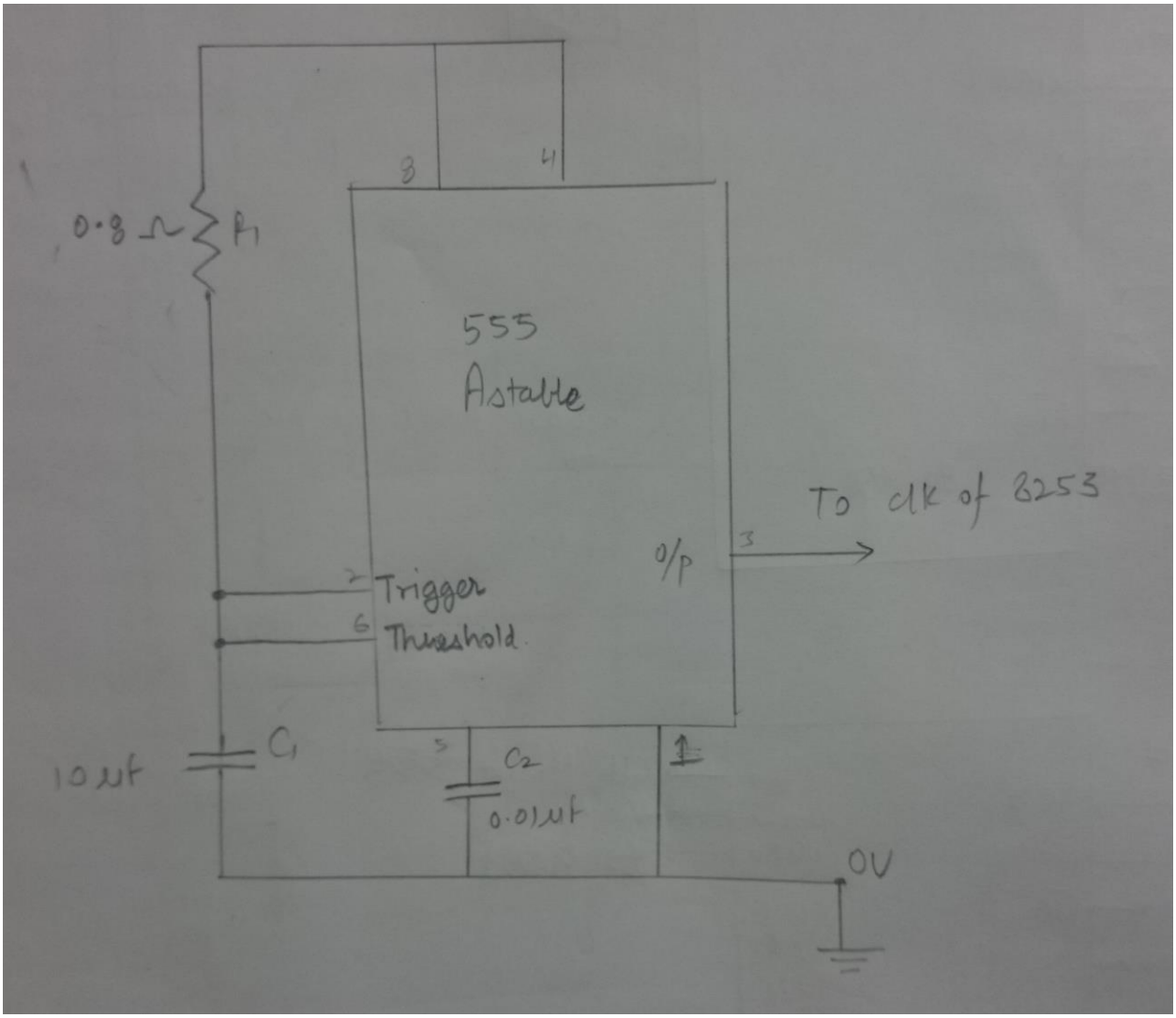
Hardware

8086

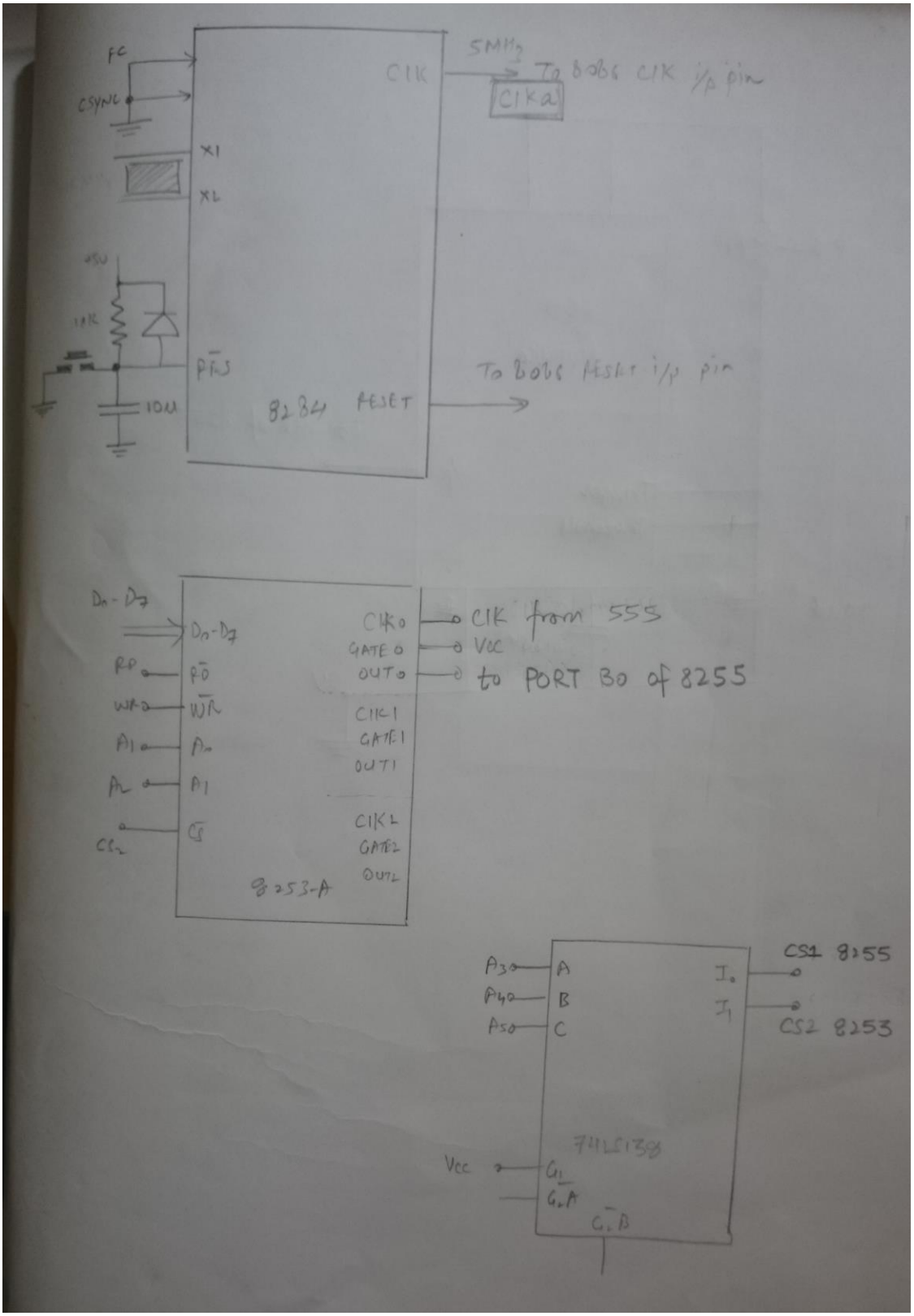



AD0 - AD7
LS373
OE
ALE
A0 - A7
AD8 - AD15
LS373
OE
ALE
A8 - A15
AD16 - AD19
LS373
OE
ALE
A16 - A19
ALE
AD0 - AD7
LS245
DIR
OE
DT/R'
DEN'
AD8 - AD15
LS245
DIR
OE
RD
WR
IO/M
LS244
OE
LOGIC CIRCUIT
MEMR
MEMW
IOR
IOW

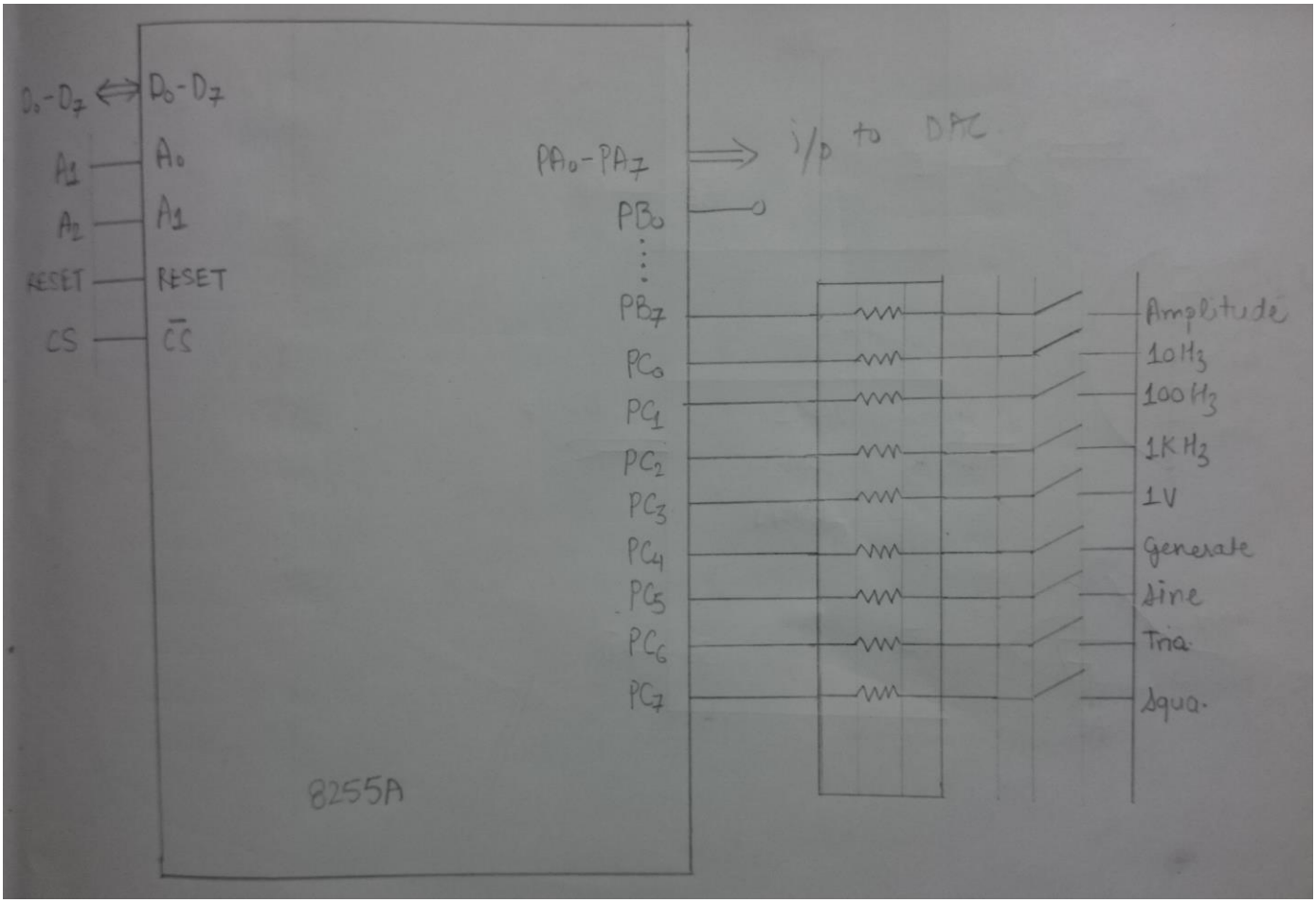
555

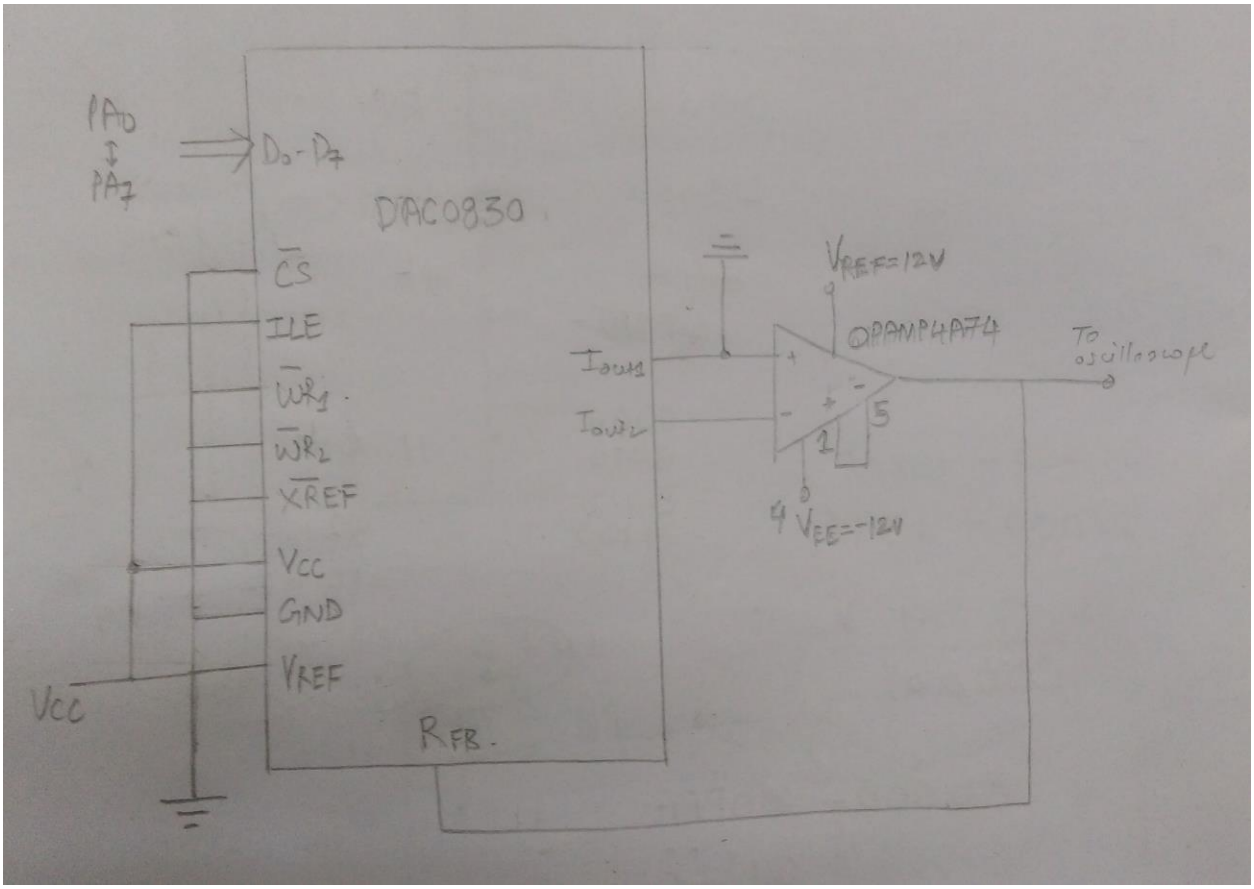

8
4
0·8 Ω
R1
555
Astable
To clk of 8253
3
O/P
2
Trigger
6
Threshold
10 μf
C1
5
C2
0·01 μf
1
0V

8253

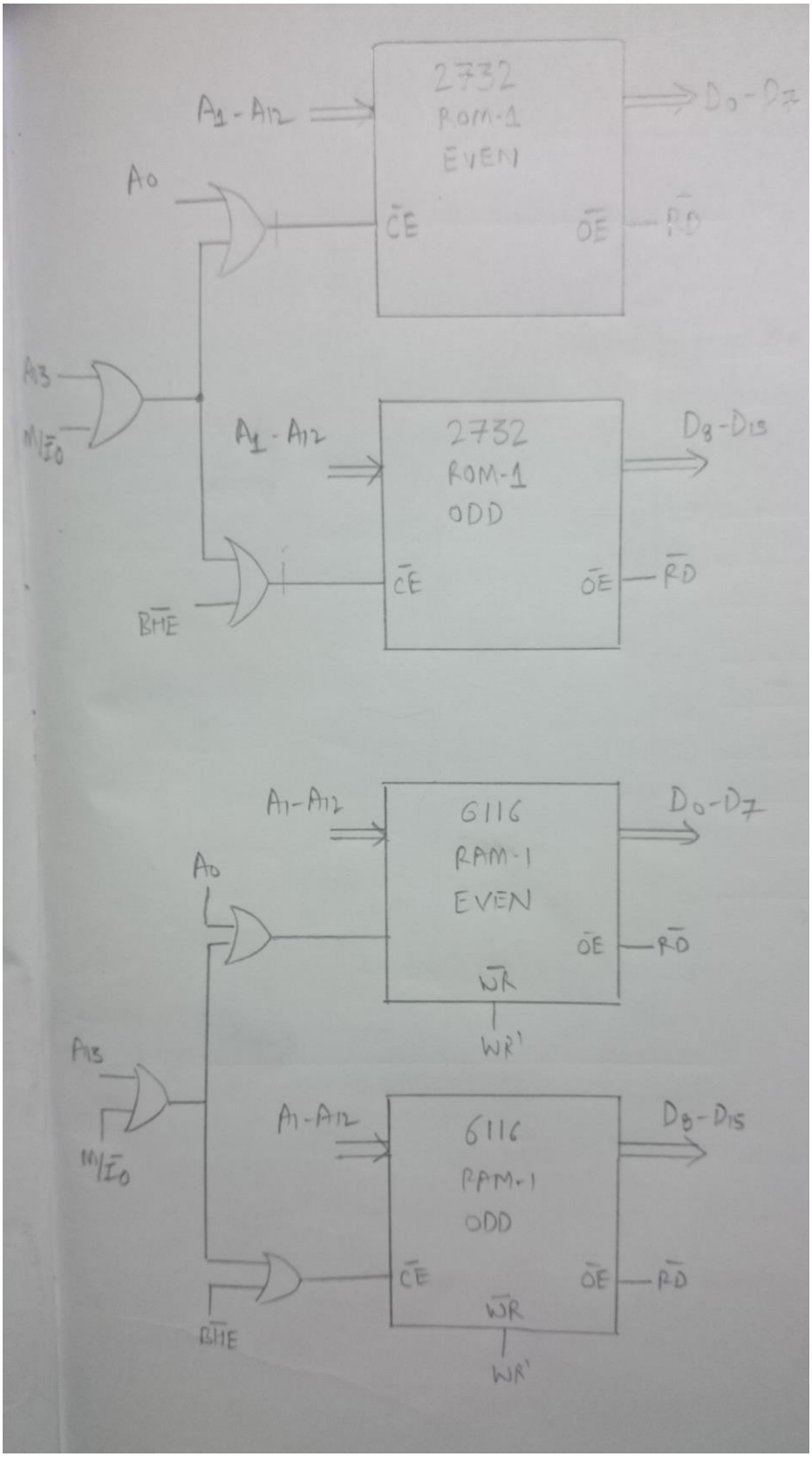

FC
CSYNC
X1
X2
+5V
1KΩ
10μ
PRES
8284
CLK
5MHz
To 8086 CLK i/p pin
CLK2
RESET
To 8086 RESET i/p pin
D0 - D7
D0 - D7
RD
RD
WR
WR
A1
A0
A0
A1
CS
CS2
CLK0
GATE 0
OUT 0
CLK from 555
Vcc
to PORT B0 of 8255
CLK1
GATE 1
OUT 1
CLK2
GATE 2
OUT 2
8253-A
A30
A40
A50
A
B
C
74LS138
Vcc
G1
G2A
G2B
Y0
Y1
CS1 8255
CS2 8253

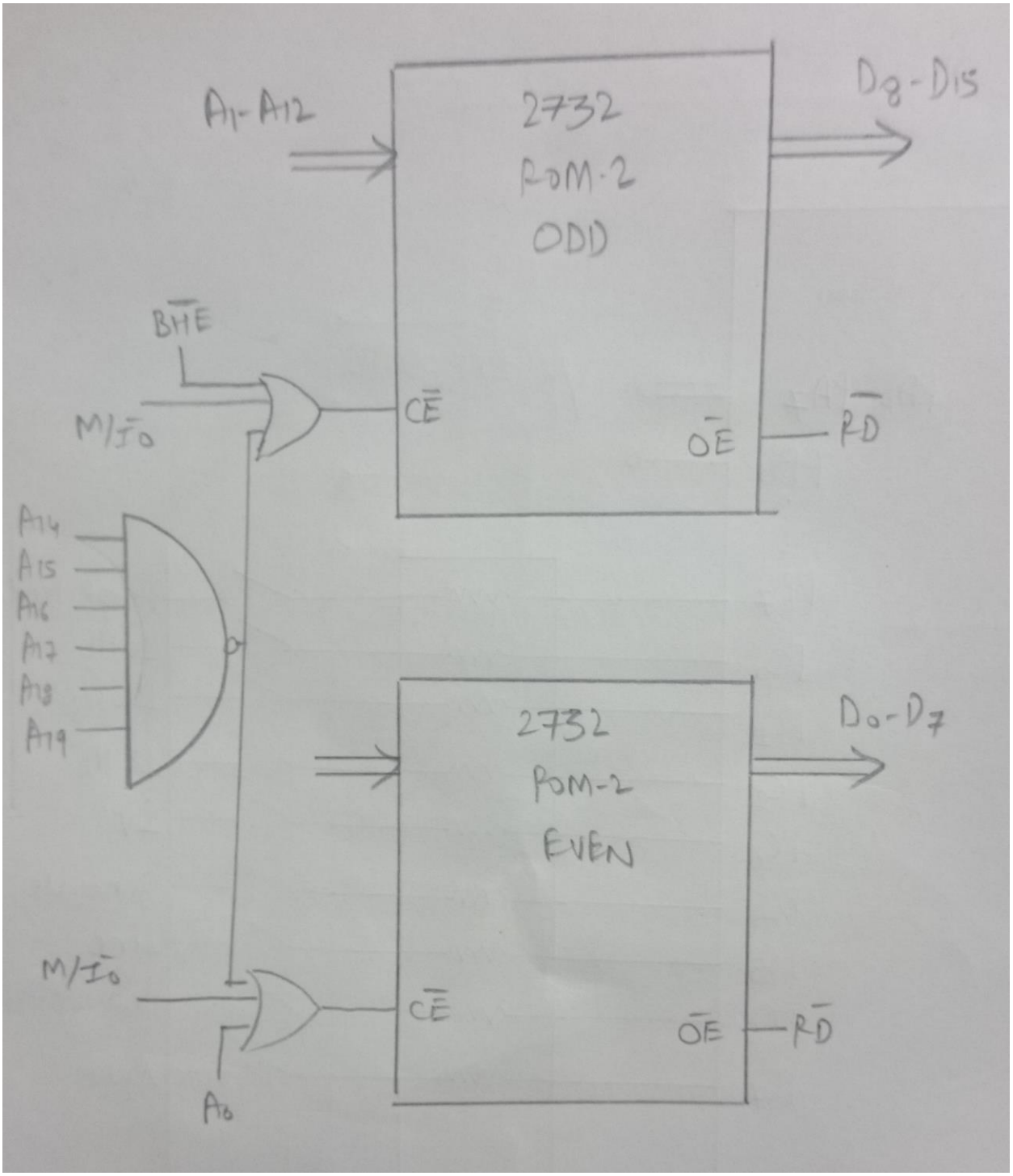
8255


D0-D7
D0-D7
A1
A0
A2
A1
RESET
RESET
CS
CS
PA0-PA7
i/p to DAC
PB0
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
Amplitude
10 Hz
100 Hz
1K Hz
1V
Generate
Sine
Tria.
Squa.
8255A


PA0
PA7
D0 - D7
DAC0830
CS
ILE
WR1
WR2
XFER
Vcc
GND
VREF
Vcc
RFB
Iout1
Iout2
VREF=12V
OPAMP4A74
To oscilloscope
5
1
4 VEE=-12V

MEMORY INTERFACING




A1-A12
2732
ROM-2
ODD
D8-D15
BHE
M/IO
CE
OE
RD
A14
A15
A16
A17
A18
A19
2732
ROM-2
EVEN
D0-D7
M/IO
CE
OE
RD
A0

We have included some samples of the Waves generated in the SAMPLES folder.

END