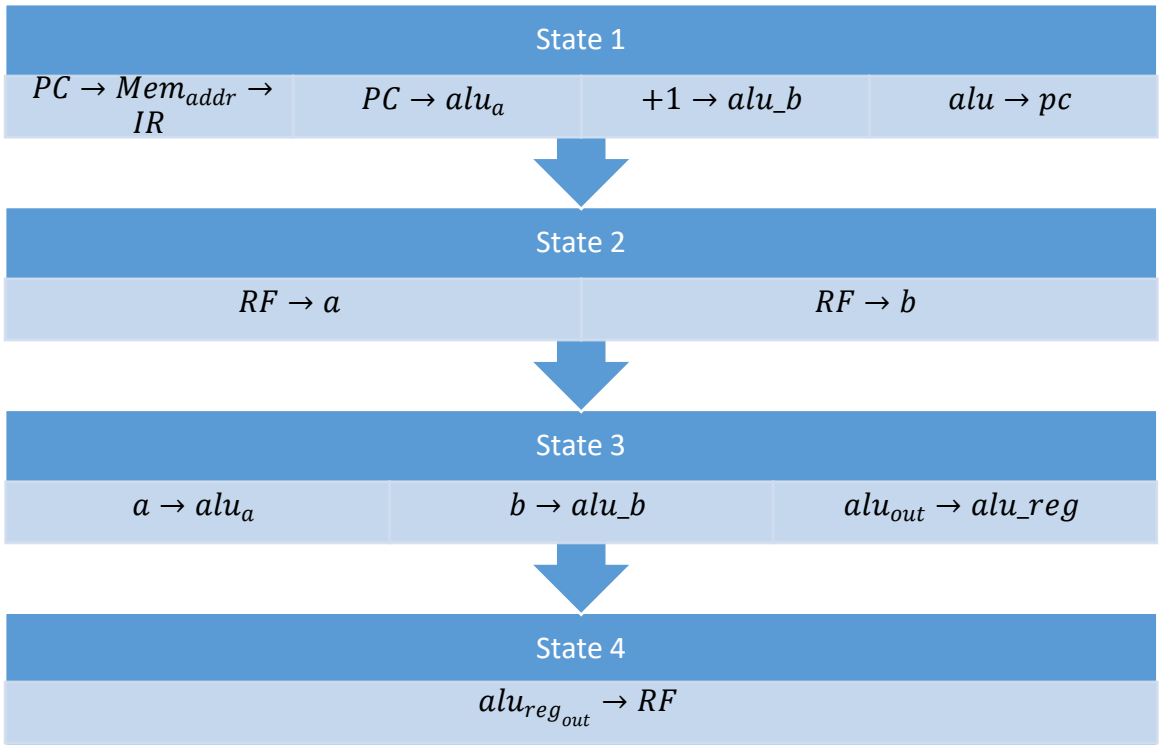
MICROPROCESSORS PROJECT 1: RISC DESIGN

The microprocessor designed IITB – RISC is an 8 – register, 16 bit system. It has eight general purpose registers (R0 – R7). R7 acts as the program counter (PC). All addresses are short word addresses. This architecture uses two conditional flags, carry flag and zero flag. It uses point-to-point communication.

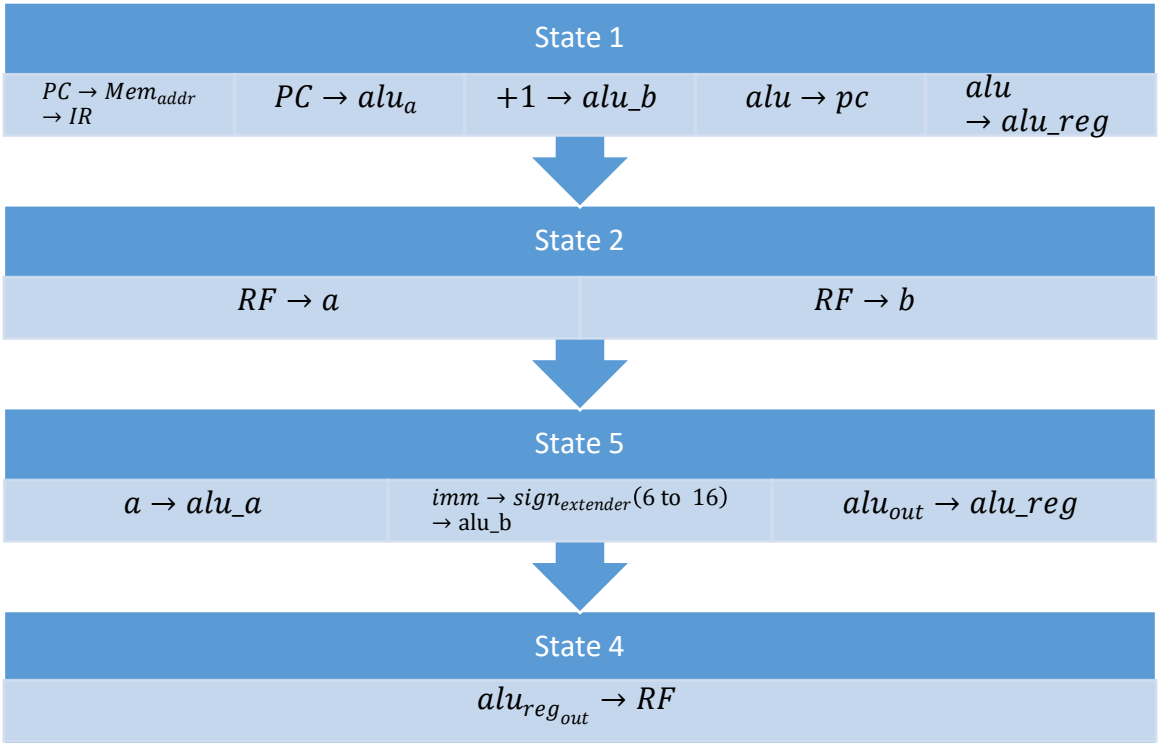
There are three machine – code instruction formats (R, I and J type) and a total of 14 instructions.

Flowcharts

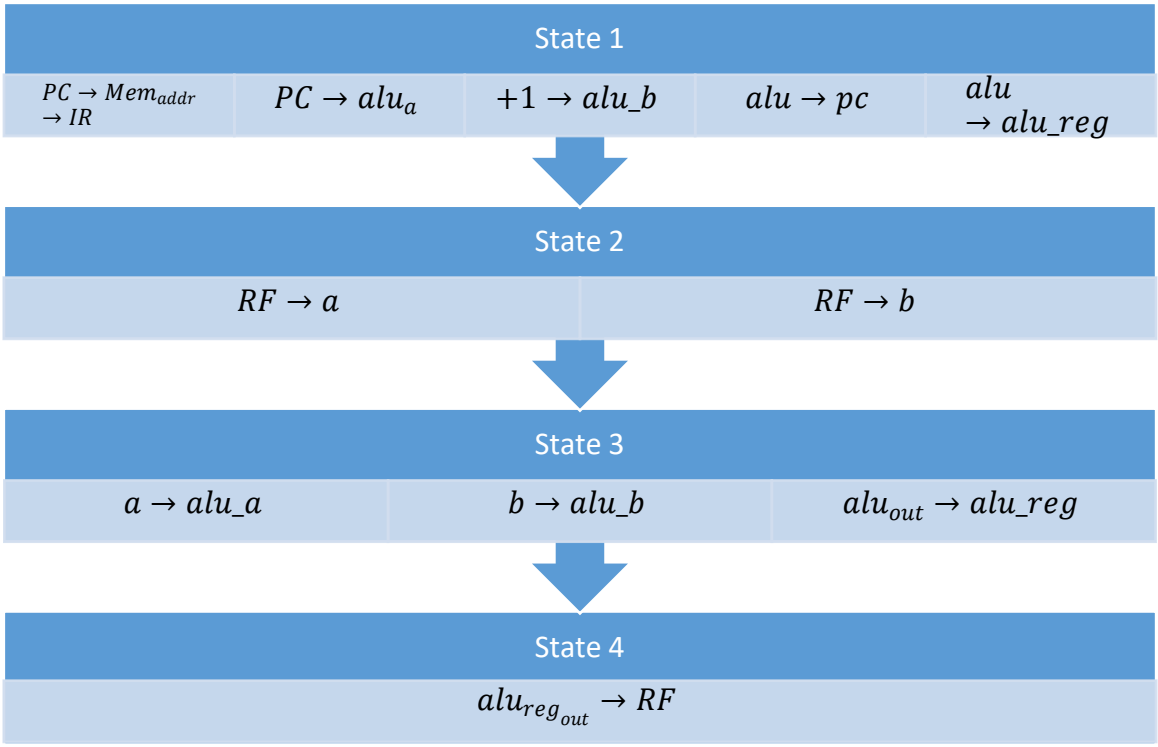
1. ADD/ADC/ADZ



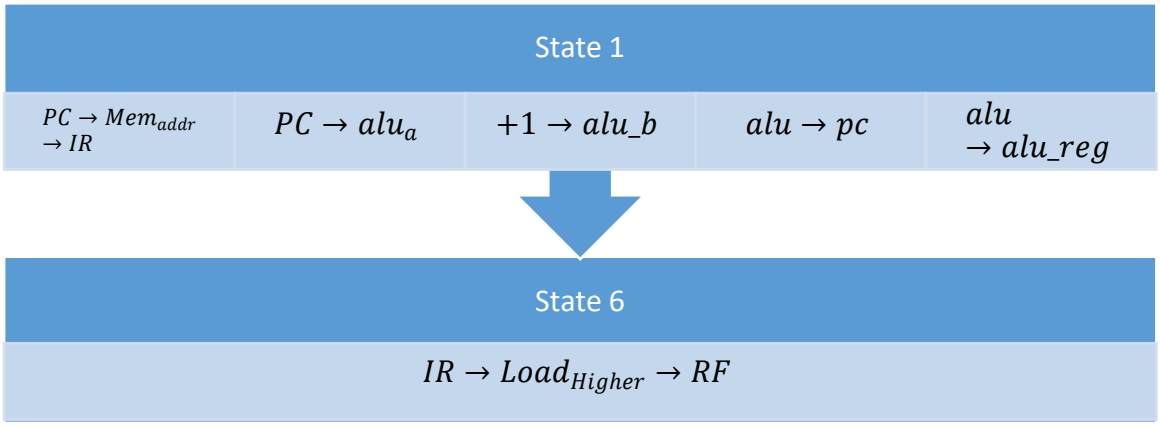
2. ADI



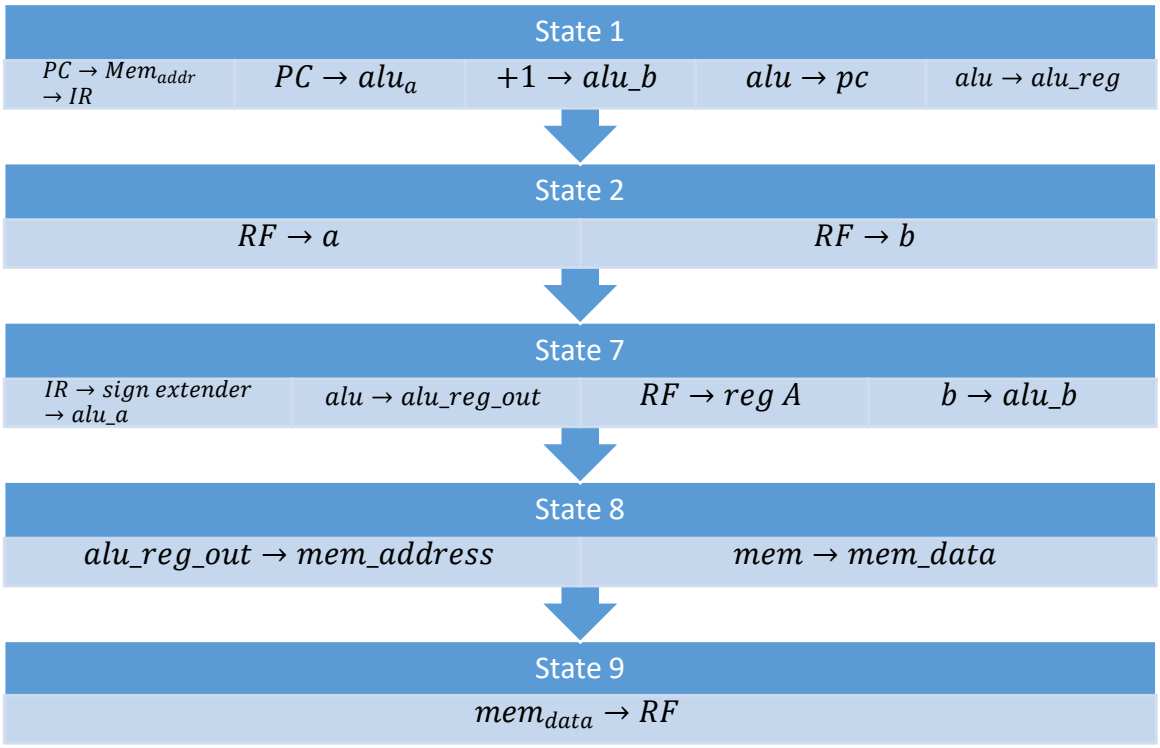
3. NDU / NDC / NDZ



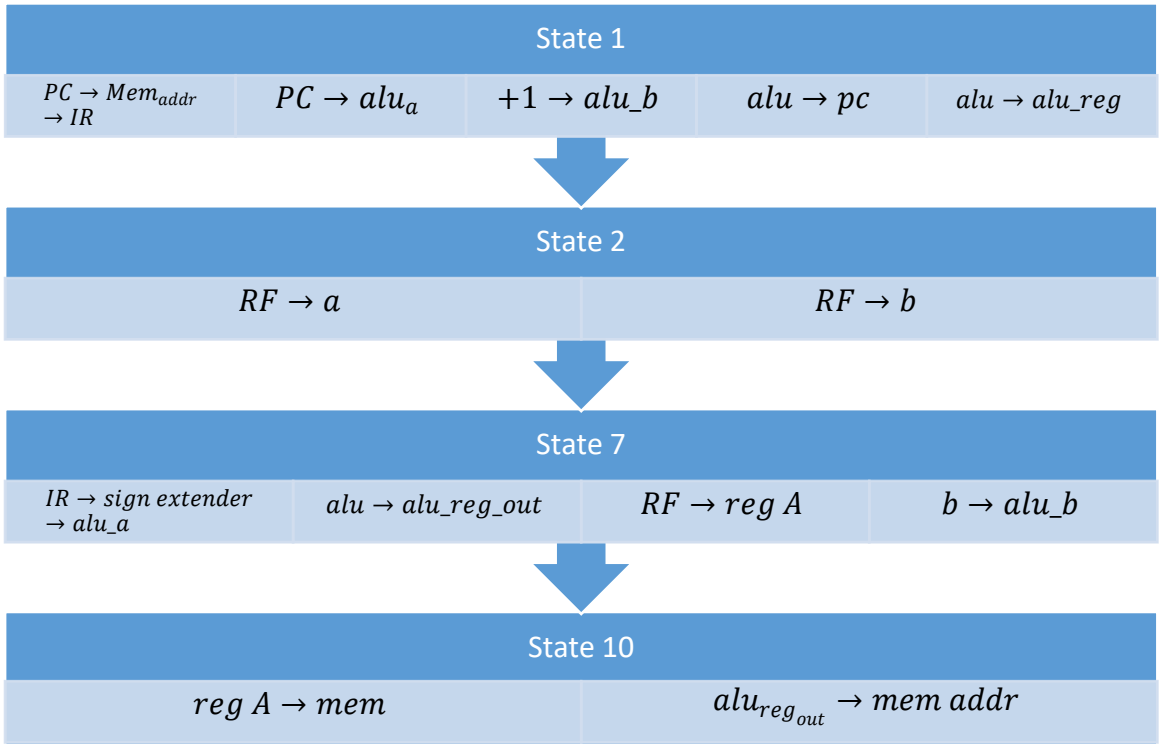
4. **LOAD HIGHER**



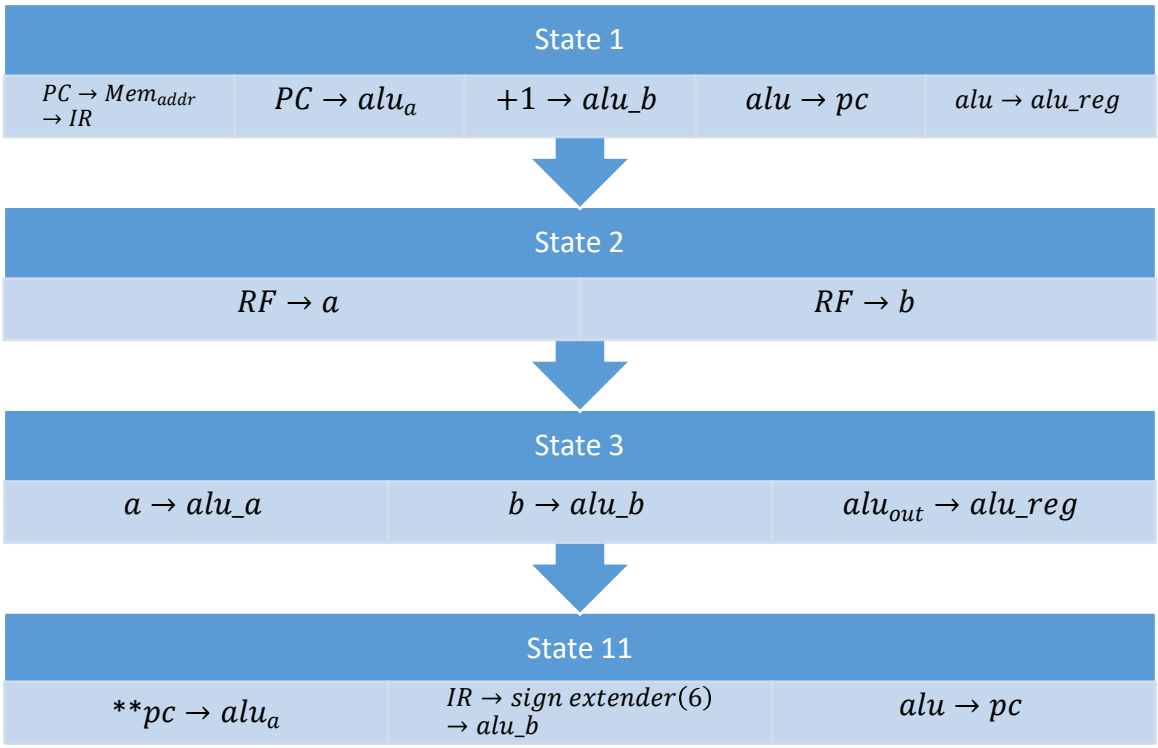
5. **LOAD**



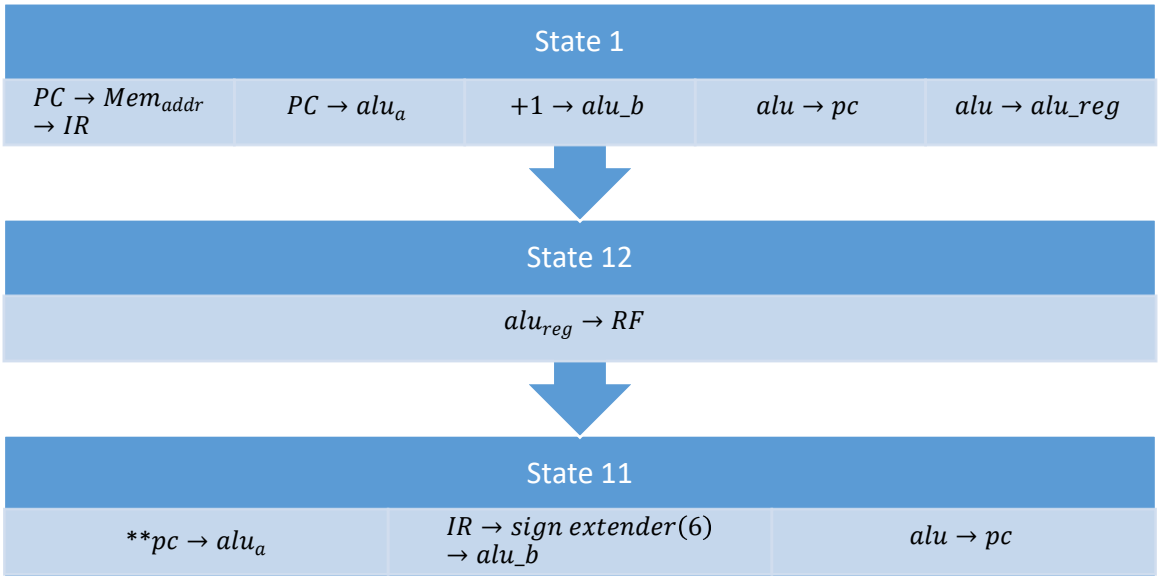
6. Store



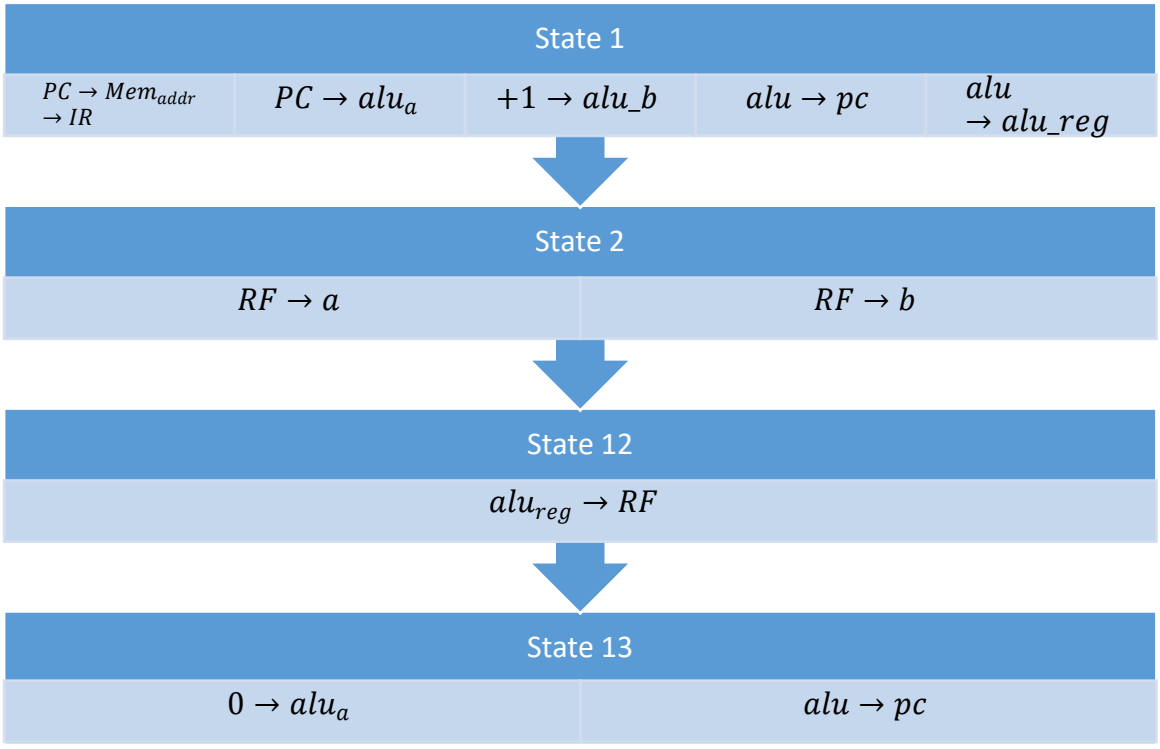
7. Branch on Equality



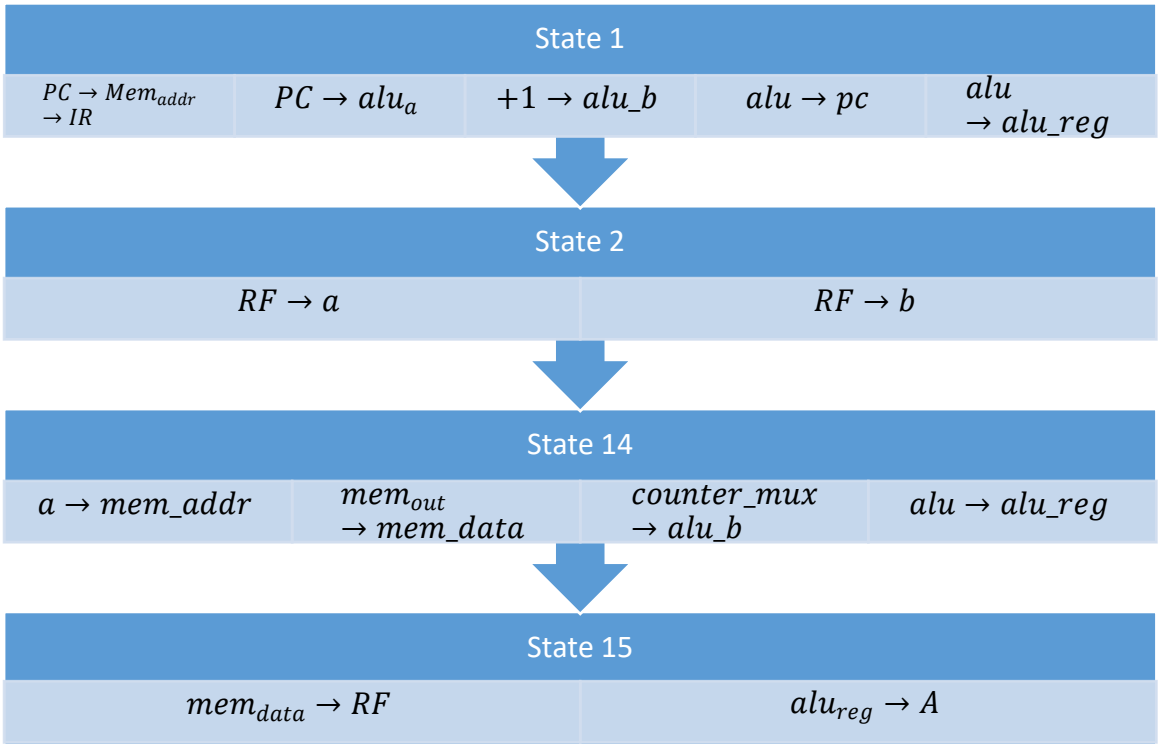
8. Jump and Link



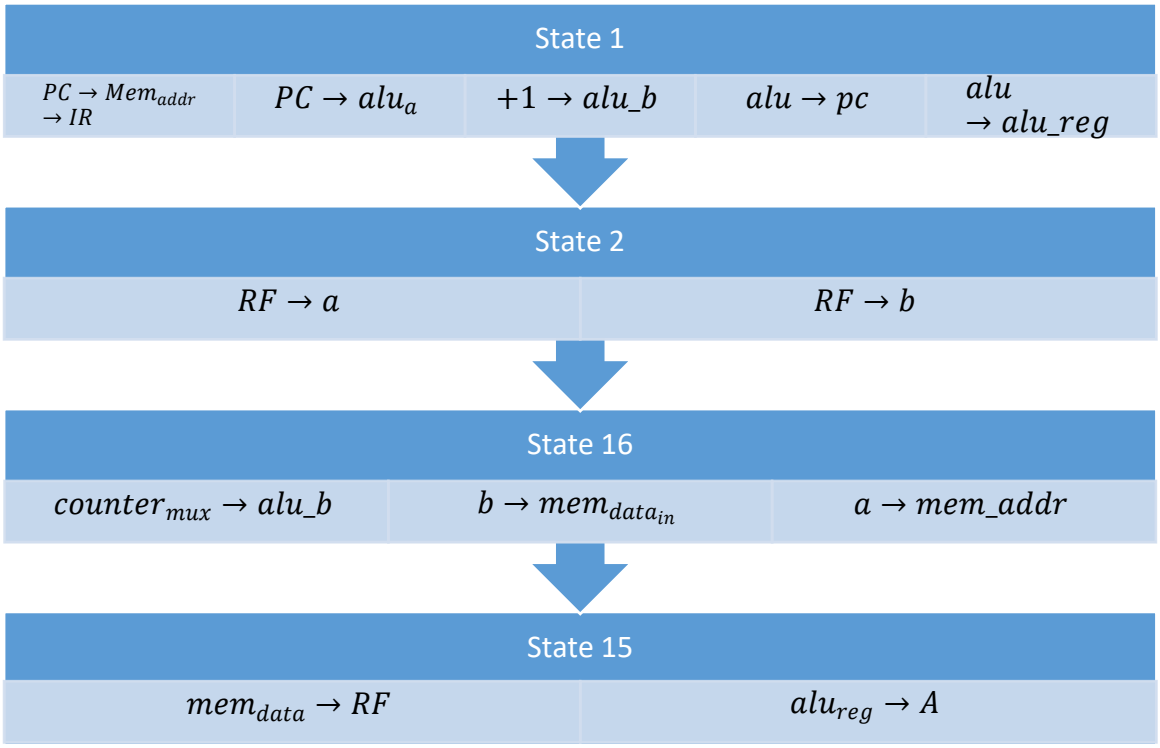
9. JUMP AND LINK TO REGISTER



10. LOAD MULTIPLE



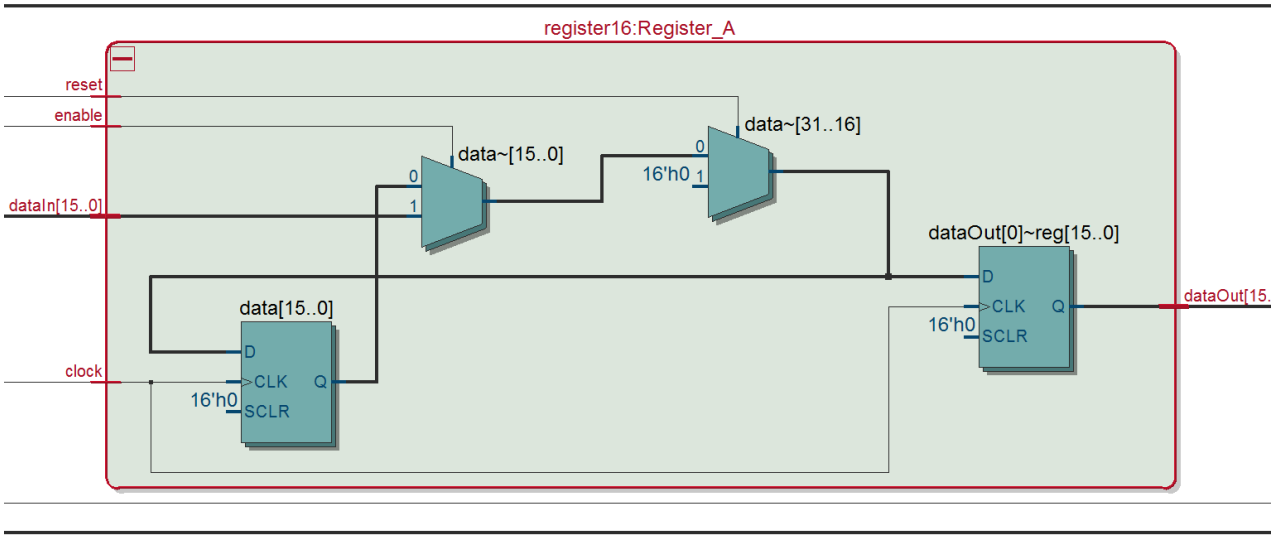
11. STORE MULTIPLE



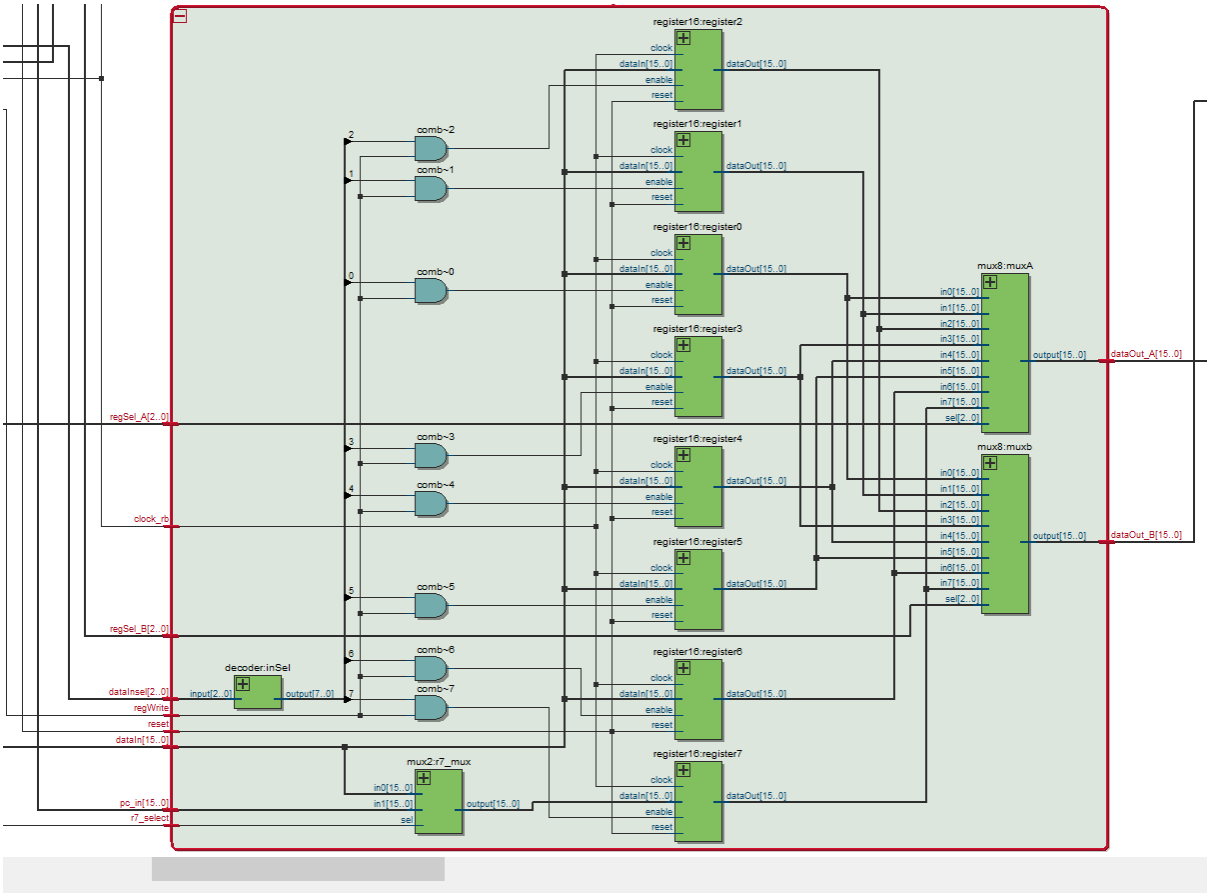
Datapath

Datapath Components

1) REGISTER



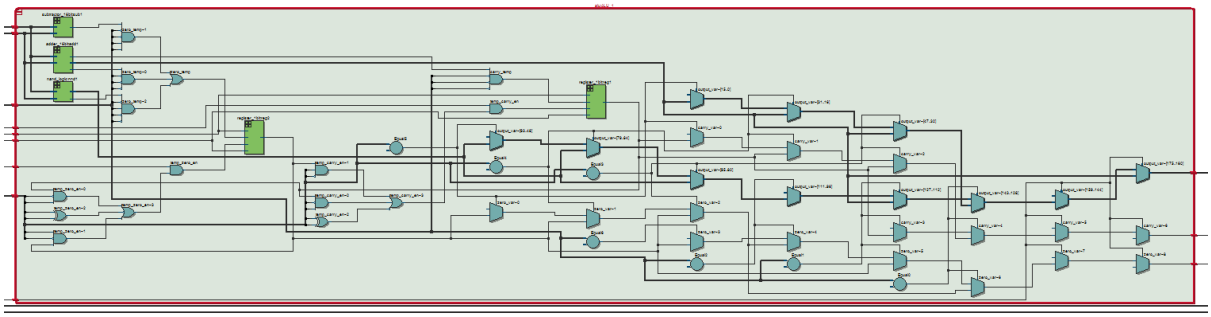
2) REGISTER BANK



3) MEMORY

4) ALU

(i) ADDER
(ii) SUBTRACTOR
(iii) NAND LOGIC CIRCUIT



5) MULTIPLEXERS

(i) GENERIC MUX

6) PROGRAM COUNTER (P.C.)

7) INSTRUCTION REGISTER

8) LOAD HIGHER

9) ALU_REG_OUT

10) SIGN EXTENDERS

(i) 6 TO 16 BIT

(ii) 9 TO 16 BIT

11) COUNTER