# Microprocessors Project 1: RISC Design

The microprocessor designed IITB – RISC is an 8 – register, 16 bit system. It has eight general purpose registers (R0 – R7). R7 acts as the program counter (PC). All addresses are short word addresses. This architecture uses two conditional flags, carry flag and zero flag. It uses point-to-point communication.

There are three machine – code instruction formats (R, I and J type) and a total of 14 instructions.

## Flowcharts and Control Signals

1. **ADD /ADC /ADZ**

4

3

2

1

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**2) ADI**

5

4

2

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**3) NDU / NDC / NDZ**

3

2

1

4

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**4) LOAD HIGHER**

6

1

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| --- | --- |
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|  |  |

**5) LOAD**

8

9

7

2

1

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**6) STORE**

10

2

7

1

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**BRANCH ON EQUALITY**

11

3

2

1

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**8) JUMP AND LINK**

12

1

|  |  |
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|  |  |
|  | , add, |

11

**9) JUMP AND LINK TO REGISTER**

13

12

2

1

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|  | , add, |

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**10) LOAD MULTIPLE**

1

2

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**12) STORE MULTIPLE**

# Datapath

# Datapath Components

1. REGISTER
2. REGISTER BANK
3. MEMORY
4. ALU
5. ADDER
6. SUBTRACTOR
7. NAND LOGIC CIRCUIT
8. PRIORITY ENCODER
9. MULTIPLEXERS
10. 2 TO 1 MUX \_ 16 BIT
11. 4 TO 1 MUX \_ 3 BIT
12. 3 TO 1 MUX \_ 16 BIT
13. PROGRAM COUNTER (P.C.)
14. INSTRUCTION REGISTER
15. LOAD HIGHER
16. ALU\_REG\_OUT
17. SIGN EXTENDERS
18. 6 TO 16 BIT
19. 9 TO 16 BIT