Eclectronics Mini-Project 1 Report

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1 Introduction

The purpose of Mini-Project 1 was to design a USB-powered LED flasher circuit while only using analog circuit components. In addition, iterating through the design process during this project should develop skills and familiarity with KiCAD6 and LTspice. The full github repository containing all relevant source code for this project can be found here.

2 Design Specifications

The designed LED flasher had to meet the following requirements:

1. The circuit must flash a surface-mount LED within $\pm10\%$ of 1s period.
2. The circuit must run on a single-ended 3.3V supply that is derived from a 5V VBUS supply in a type-A USB port.
3. The circuit may only use parts from the provided parts list, which includes two operational amplifier models, resistors, LEDs, capacitors, and a linear regulator.
4. All integrated circuit components need adequate bypass and bulk capacitors, as specified by their data sheets.
5. The designed PCB must be a two-layer design with all components on the surface of the first layer. The minimum allowable via size is 24 mils with a 12-mil drill hole. The minimum allowable trace width and spacing is 6 mils. All power lines must be at least 15 mils.
6. Minimize PCB size, particularly in terms of height, in order to optimize price and usability.

3 Design Process

While designing this PCB, the following design process was followed:

1. Designed hysteretic oscillator in LTspice.
2. Ran parameter sweep to determine optimal resistor and capacitor values to produce 1s period.
3. Conducted worst case analysis to ensure circuit period remains within specified bounds.
4. Designed full circuit schematic in KiCAD.
5. Designed full layout in KiCAD.

More detail is provided on the details of each step in the process below.

4 Hysteretic Oscillator

The first step was to design the Hysteretic Oscillator in LTspice. The Hysteretic Oscillator is an application of operational amplifiers that produces a digital signal bounded by the operational amplifier's operating voltage and ground point. A schematic of the Hysteretic Oscillator is shown below.

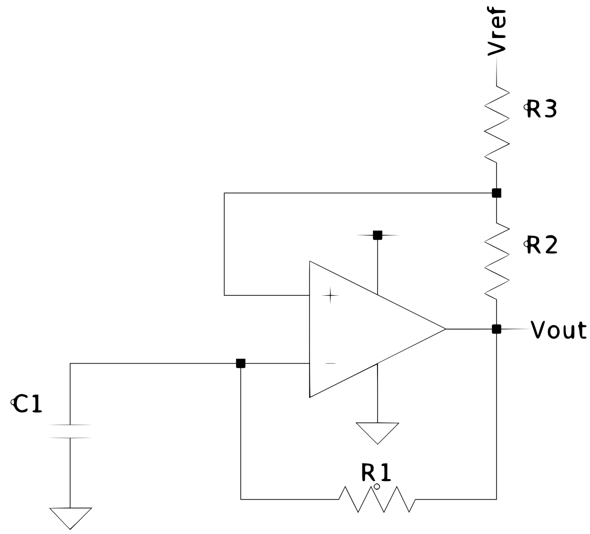

Figure 1: Schematic layout of Hysteretic Oscillator

For this implementation of the Hysteretic Oscillator, 3.3V was used for the voltage supply of the operational amplifier and 0V was used for the ground point. The non-inverting feedback aspect of the operational amplifier is a voltage divider. This voltage divider is used to define the hysteresis window, which is the voltage range that the voltage input to the non-inverting input of the operational amplifier oscillates between. For this design, both resistors of the voltage divider (R2 and R3) are 10kΩ. By setting them equal, the hysteresis window becomes 50%, meaning that the non-inverting voltage input ranges between $\frac{1}{4}$Vdd and $\frac{3}{4}$Vdd. The hysteresis window affects the the period of oscillation as a larger window requires a larger time between oscillations. The decision to establish a 1:1 ratio between resistors was in order to reduce the amount of parameters that needed to be swept through in order to determine the final circuit configuration. Additionally, setting a 50% hysteresis window is a typical design decision when establishing a hysteretic oscillator. The reference voltage of the voltage divider, this was set to $\frac{Vdd}{2}$, which sets the duty cycle of the outputted wave to 50%, which would make the blinking of the LED as apparent as possible.

As for the inverting feedback aspect of the schematic, this is a simple RC circuit. This is used to fluctuate the input voltage to the inverting signal, which in turn, adjusts the period of the outputted wave. While not directly equivalent, the time constant of this low pass filter is directly proportional to the period of oscillation. For this design, the capacitor (C1) was set to .1μF. This was because the provided parts list only featured capacitors from 10 pF to 10 μF, at 10 multiples. The highest two capacitors had a ±10% error, which is why the next lowest was selected, which had a lower error at ±5%.

5 LTspice Parameter Sweep

Once C1, R2, and R3 were established, the main mechanisms of the LED flasher circuit were designed in LTspice in order to determine an optimal value for R1 that would yield an output wave with an oscillation period of 1s. The full schematic is shown below.

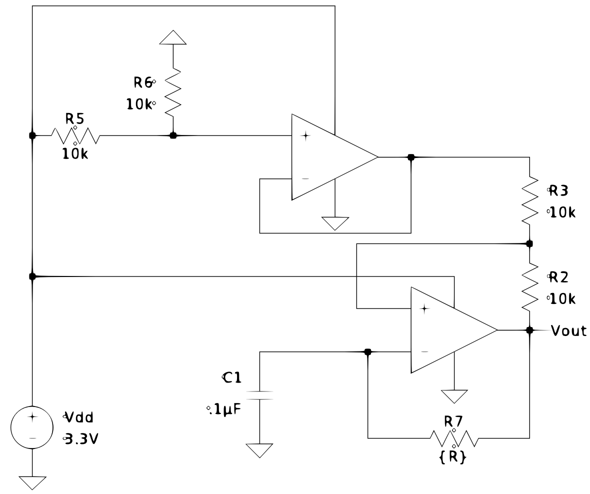

Figure 2: LTspice schematic of LED flasher

In addition to the hysteretic oscillator described above, the main circuitry includes a voltage source and a voltage divider. The voltage source of 3.3V is an abstracted version of the expected input coming from the linear regulator of the actual circuitry. The voltage divider is implemented in order to establish Vref. As mentioned earlier, the desired Vref is $\frac{Vdd}{2}$, or 1.65V. In order to achieve this voltage, a voltage divider with a 1:1 resistor ratio (each 10kΩ) was implemented. However, the voltage divider could not be directly connected to the hysteretic oscillator as Vref as this connection would mean that the second resistor is in parallel with the rest of the circuitry, interfering with the 1:1 resistor ratio, which would produce a skewed Vref and impact the duty cycle of the outputted oscillation. Thus, the voltage divider was connected to the non-inverting signal of the operational amplifier, with negative feedback. This allows for a reliable 1.65V output, which was used as the Vref of the hysteretic oscillator.

Once the circuit was designed, the only value that needed to be experimentally determined was R7. This was done by running a transient analysis of the circuit under different values of R1. This was done in two phases: an initial parameter sweep and a more fine-tuned parameter sweep. The initial parameter sweep was conducted by stepping the value of R1 from 10kΩ to 10MΩ to establish a decade range for the optimal value that would yield a 1s period. In order to run a parameter sweep, the following commands were run in LTspice:

```
.step param R list 10k 100k 1000k 10000k
.tran 4 startup
```

The first line establishes the range of values to sweep through for R. In the second line, tran signifies the transient analysis, 4 is the time (in seconds) that the analysis should be run for, and startup specifies that the voltage sources should start at 0V and quickly ramp up to their specified supply voltage. One iteration of this parameter sweep generates the following oscillation:

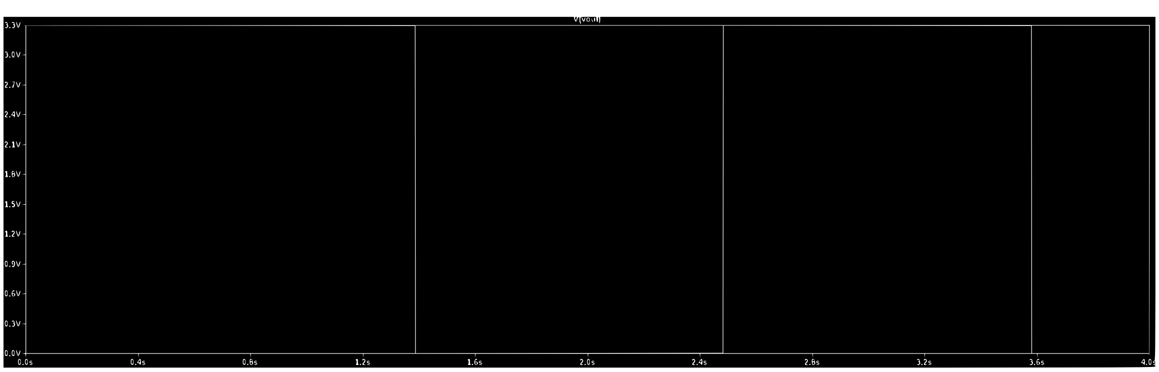

Figure 3: One Iteration of LTspice Parameter Sweep

The first period is longer than all subsequent oscillations as rather than the voltage input of the inverting signal rising from $\frac{1}{4}$Vdd to $\frac{3}{4}$Vdd, it must rise from 0, which requires more time. For this reason, only oscillations after the first period were considered when analyzing the period. The results of each parameter sweep was exported as a text file. This file was then loaded into python in order to analyze each signal for its period. At a high level, the code sweeps through the entire text file, analyzing each iteration of the parameter sweep. For each iteration, the algorithm skips the first oscillation and searches for the next time the signal switches from low to high and records the time of that switch. Then, it searches for the next time the signal switches from low to high and records the corresponding timestamp. The difference between the two timestamps becomes the period for that specific circuit setup. Once the analysis is complete, the script outputs the period that each resistor value yielded. The results of the initial sweep are shown below:

Resistor kΩ	Period (s)
10	0.00337
100	0.0225
1000	0.220
10000	2.20

Figure 4: Calculated Periods of Initial Parameter Sweep

This sweep suggests that the optimal value for the resistor is between 1MΩ and 10MΩ. This led to a second parameter sweep with a more fine-tuned parameter range, which was run with the commands below:

```
.step dec param R 1000k 10000k 20
.tran 4 startup
```

In this case, the sweep of R was a decade sweep of 20 values between 1MΩ and 10MΩ. This yielded the following results:

Resistor MΩ	Period (s)
1	0.220
1.122	0.247
1.259	0.277
1.413	0.310
1.585	0.346
1.778	0.391
1.995	0.438
2.239	0.492
2.511	0.552
2.818	0.619
3.162	0.695
3.548	0.779
3.981	0.874
4.467	0.981
5.012	1.101
5.623	1.235
6.310	1.386
7.079	1.555
7.943	1.744
8.913	1.957
10	2.195

Figure 5: Calculated Periods of Fine-Tuned Parameter Sweep

Based on these results, 4.467MΩ yielded the closest period to the desired period of 1s. However, since exact resistor values were not available, the combination of 3 resistors (604kΩ, 953kΩ, and 3.01MΩ) were used, which totalled an equivalent resistance of 4.567MΩ. Under these conditions, the theoretical period of the output oscillation is 1.002 seconds.

6 Worst Case Analysis

Since there was error associated with the capacitance and resistance of the ordered manufactured parts, a worst case analysis was conducted in order to determine whether the outputted oscillation period would fit into the specified bounds (1s ±10%), even given the worst case for manufactured parts. This was done by running transient analysis on every possible combination of worst case devices. The worst case of a device is the highest and lowest value it is expected to have given its error threshold. This was applied to every analog circuit component with a published tolerance band on its data sheet, meaning all 7 resistors and 1 capacitor. This yielded 256 different iterations of device combinations. Once the transient analysis was run, the data was analyzed using the same python script as above. This yielded a maximum period of 1.0739s and a minimum period of 0.9295s, both of which are within the given bounds for the period.

7 KiCAD Schematic Diagram

Once the nominal values for each circuit component was determined, the next step was to implement the full schematic in KiCAD. The final schematic layout is shown below:

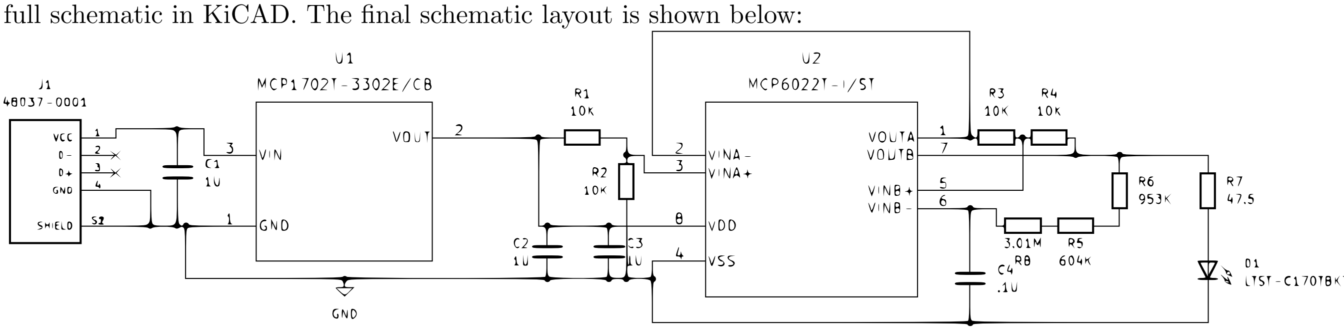

Figure 6: Full Schematic Diagram of LED Flasher

The additions made from the LTspice to KiCAD are the linear regulator, a different schematic symbol for the operational amplifier, the type-A USB connector, and bulk and bypass capacitors. The LTspice model had abstracted away the linear regulator and type-A USB connector. In this layout, the USB serves as the VBUS source, along with providing a ground reference point for all other circuit elements to reference. The VBUS of the USB is set to 5V, which needs to be step down to 3.3V for the rest of the circuit components. This is done using the linear regulator. Additionally, the linear regulator requires a 1μF bulk capacitor (C1 and C2) at its Vin and Vout, as specified by its data sheet, which are specified in the layout. Additionally, the operational amplifier requires a .1μF bypass capacitor (C3) to be placed within 2mm of its Vdd and a 1μF bulk capacitor (C2) be placed within 100 mm of its Vdd to preserve signal integrity. The data sheet also specified that the bulk capacitor can be shared with other ICs as long as it remains within the specified distance. In this case, the operational amplifier shares a bulk capacitor with the Vout of the linear regulator.

The other additional component included on the schematic is the LED and resistor limiting current to the LED. This was connected to the output of the hysteretic oscillator, which would yield a flashing LED at a period of 1s at a 50% duty cycle. The specific value of the resistor was calculated based on the voltage and current requirements of the LED. The minimum voltage drop across the LED, as according to the data sheet, is 2.8 V. The output of the operational amplifier, when high, is 3.3V, meaning the the voltage drop across the resistor must be .5V. Additionally, the typical forward current across the LED is 20 mA. Using Ohm's Law, this equates to a resistance of 25Ω. However, to ensure that too much current was not drawn by the LED, this was increased slightly to 47.5Ω.

8 KiCAD Layout

To generate the layout, the overall PCB size was minimized, especially by constraining the height of the board to just fit the footprint of the USB. This involved multiple iterations in order to develop optimal connections. Additionally, careful consideration had to be made when working with power lines, which were designed with larger (15 mils) trace sizes.

9 Bill of Materials

Item	Quantity	Reference(s)	Value
1	2	C1, C2	1μF
2	2	C3, C4	$.1\mu$F
3	1	D1	LTST-C170TBKT
4	1	J1	48037-0001
5	4	R1, R2, R3, R4	10kΩ
6	1	R5	604kΩ
7	1	R6	953kΩ
8	1	R7	47.5Ω
9	1	R8	3.01MΩ
10	1	U1	MCP1702T-3302E/CB
11	1	U2	MCP6022T-I/ST

Figure 7: Bill of Materials for PCB