# EXPERIMENT - 1

→ **TITLE** : Verification of Sampling Theorem

→ **AIM OF THE EXPERIMENT** :
① To obtain the sampled output for given modulating signal output
② Verifying the sampling theorem for different modulating frequencies $f_s < 2f_m$, $f_s = 2f_m$ and $f_s > 2f_m$
③ Reconstruct original signal from sampled signal.

→ **APPARATUS REQUIRED** :
- Sampling theorem training kit.
- Digital storage Oscilloscope (100 MHz)
- Power Supply
- Probes
- Patch Cord
- Connecting Wires

→ **THEORY** : Sampling is the process of conversion of analog signal to discrete signal. Sampling theorem shows that a continuous time & band limited signal may be represented perfectly by its samples at uniform intervals of T-seconds, if T is small enough. In other words, the continuous time signal may be re-constructed perfectly from its samples

sampling at high enough rate is information-
-loseless.

Sampling theorem states that →

① The band limited signal of finite energy, which has no-frequency component higher than w-hertz, is completely described by specifies the value of signal at instant of time separated by $1/2w$ second.

② The band limited signal of finite energy, which has no-frequency component higher than w hertz, must be completely recovered from knowledge of its samples taken at rate 2w per second.

$$F_s >= 2 f_m$$

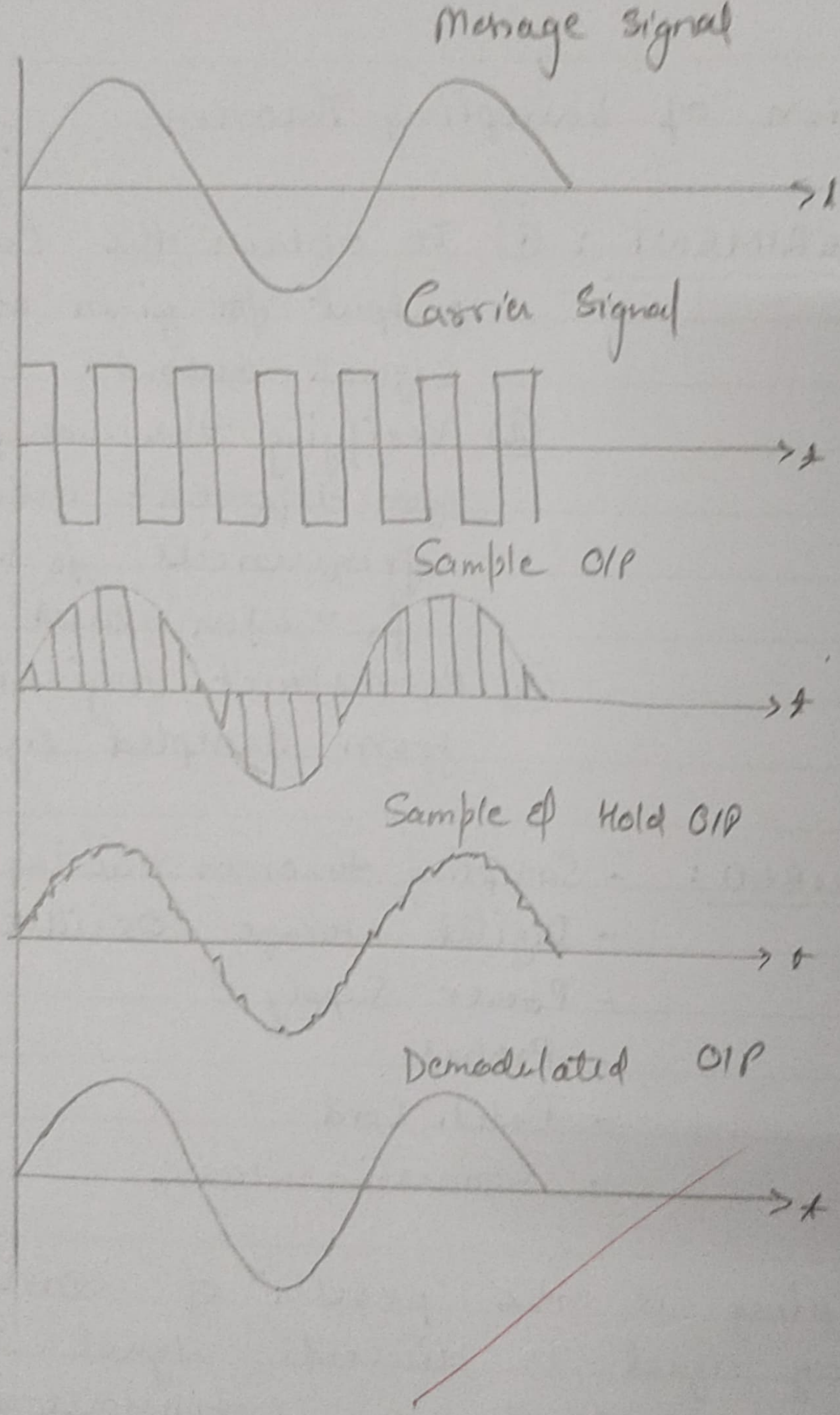
If sampling frequency is less than Niquist Rate then distortion is called aliasing.

$$g_\delta(t) = \sum_{n=-\infty}^{\infty} g(nT_s)\,\delta(t - nT_s)$$

$g_\delta(t)$ = the ideal sampled signal.

$f_s = \frac{1}{T_s}$ : sampling rate.

$T_s$ = Sampling Period.



Message Signal
Carrier Signal
Sample O/P
Sample & Hold O/P
Demodulated O/P

→ PROCEDURE : 1 → Connections are given as per diagram.
2 → Take the sine wave as input of 1 KHz from signal generator Block.
3 → Observe the carrier waveform & note down the amplitude & time-period of signal.
4 → Observe the sampled signal & note down the amplitude & time-period of signal.
5 → Observe the sampled & hold signal and note down the amplitude & time period of the signal.
6 → Then the ~~amplitude~~ sampled signal is given as an input to low pass filter & then re-constructed waveform is obtained in output of lowpass filter.
7 → Plot the graph for the sampled signal & Sample & hold signal.

# EXPERIMENT - 02

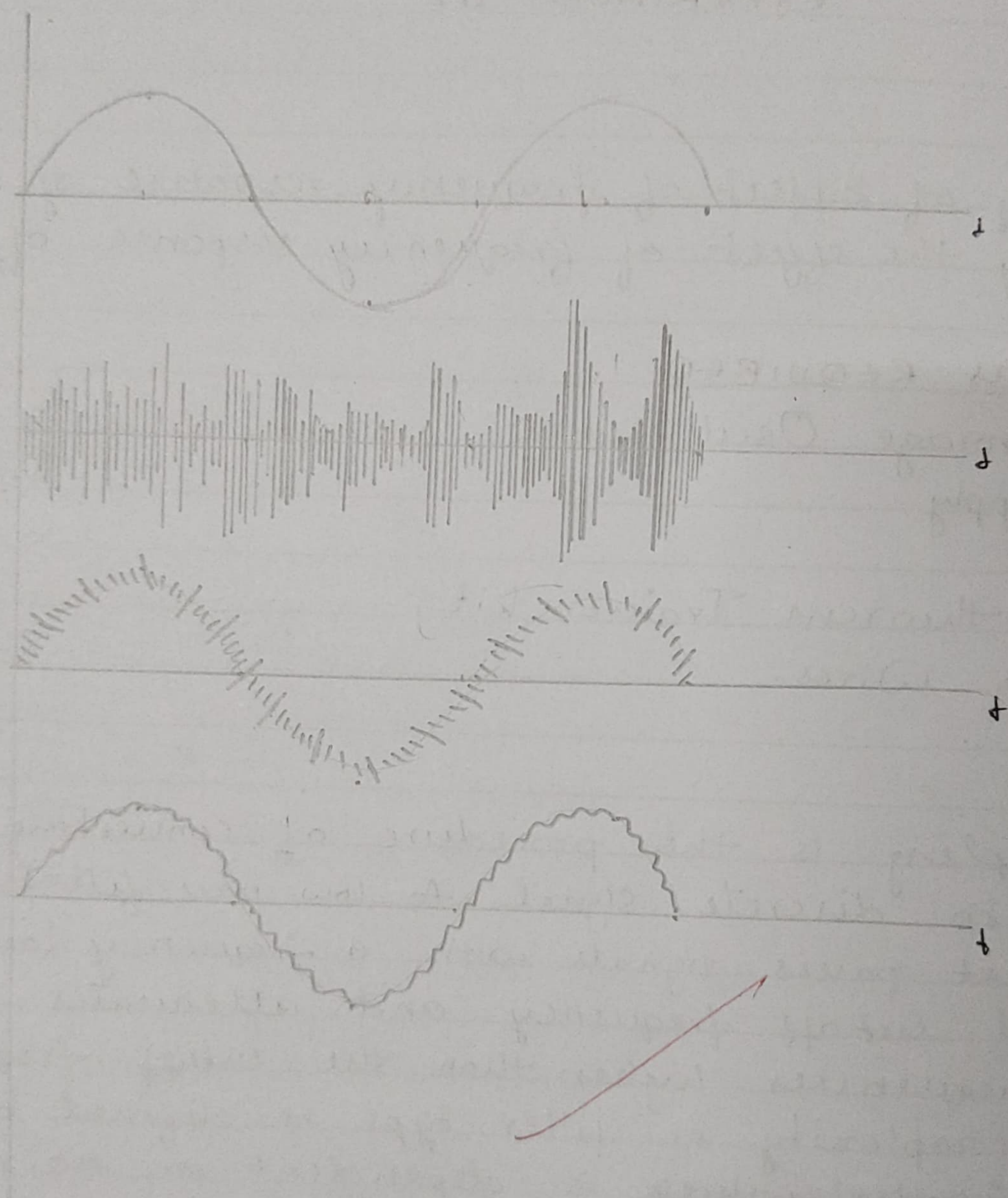
→ AIM
- The Study of Effect of frequency response of $2^{nd}$ order.
- To study the effect of frequency response of $4^{th}$ order.

EQUIPMENTS REQUIRED
1. Digital Storage Oscilloscope
2. Power Supply
3. Probes
4. Sampling theorem Trainer kit
5. Connecting Wires.

→ THEORY
- Sampling is the procedure of converting analog signal into discrete signal. A low pass filter is a filter that passes signals with a frequency lower than a selected cutoff frequency and attenuates signals with frequencies higher than the cutoff frequency.
The complexity or filter type is defined by the filters "order" which is dependent on no. of reactive components within the design. Rate of roll-off and therefore the width of the transition band depends on the order number of the filter.

PROCEDURE

1- Connect the mains plug into the mains board. keep the power switch in OFF position.
2- Ensure that the 'EXT / INT' SAMPLING SELECTOR switch is in 'INTERNAL' position.
3- Put the Duty Cycle Selector switch in position 5.
4- Link 1 KHz sine wave output to ANALOG INPUT.
5- Turn "on" the trainer.
6- Link 1 KHz afterwards add sample output to input of the second order low pass filter & to the input of fourth order low pass filter. Observe the output of two filters on the oscilloscope. Vary the sampling frequency with duty cycle at 50%. Compare the ~~output~~ output of filter in each case. Note that the output of fourth-order filter always exhibits less distortion than second-order filter has a sharper roll-off and thus rejects more unwanted frequency components caused by sampling.
7- Also compare the phase lag between input & output for each filter.
8- Repeat the above procedure with sample and hold circuitry.
9- Dis-connect all the links
10- Using the function generator of 600 Ω impedance apply the sine-wave of 2V peak at 100 Hz. O/P to second order filter input.



label the diagram

11- Repeat the above steps with fourth order filter.

→ RESULT

We can see the output of $2^{nd}$ & $4^{th}$ order low pass filter. We have also studied about butter worth's low pass filter.

# EXPERIMENT- 3

## AIM -
To study the time division multiplexing.

## EQUIPMENTS REQUIRED -
1. ST2103 trainer with power supply Card
2. Oscilloscope with connecting probe.
3. Correction Chords.

## THEORY
Time division multiplexing is a method of putting multiple data streams in a signal by separating the signal into many segments, each having a very short duration. Each individual data streams is resembled at the recieving end based on timing.

The circuit that combines signals at the source end of a communication link is known as multiplexer. It accepts the input from each individual end user, breaks each signal into segments and assigns the segments to the composite signal in a rotating, repeating sequence.

## PROCEDURE
A. Initial setup for trainer ST2103.
- Made switch position : fast position
- DC1 & DC2 amplitude controls : Fully Clockwise direction.
- 1kHz to 2kHz signal levels: 10V peak to peak.
- Pseudo random, synch code.

- Generator Switch : OFF position.

→ ERROR CHECK CODE SELECTION

Switches A & B mode - A=0 & B=0 position (OFF mode)

All switched faults - OFF position.

1- Connect the 1 kHz output to CRO.
2. Turn on power supply & oscilloscope. Check that the PAM output of 1kHz sine wave is available at TP is of the ST2103.
3- Connect channel 1 of the oscilloscope to TP10 & Channel 2 of the oscilloscope of TP15. Observe the timing and phase rotation between the sampling signal TP10 & sampled waveform at TP15.
4- Turn off the power-supply. Now Connect also the 2kHz ~~supply to~~ CH1
5. Connect channel 1 of the oscilloscope to TP12 & channel 2 of oscilloscope of TP15.
6- Observe & explain the timing rotation between the signals at TP10, 5, 6, 12 & 15.

→ Conclusion — Proper selection of voltages as i/p gives o/p in form of binary sequence.

# EXPERIMENT-4.

→ AIM-
Study of Delta-Modulation Demodulation.

→ EQUIPMENT REQUPRED-
1→ Power Supply
2- Delta modulation board. kit (&) connecting wires
3- Probes

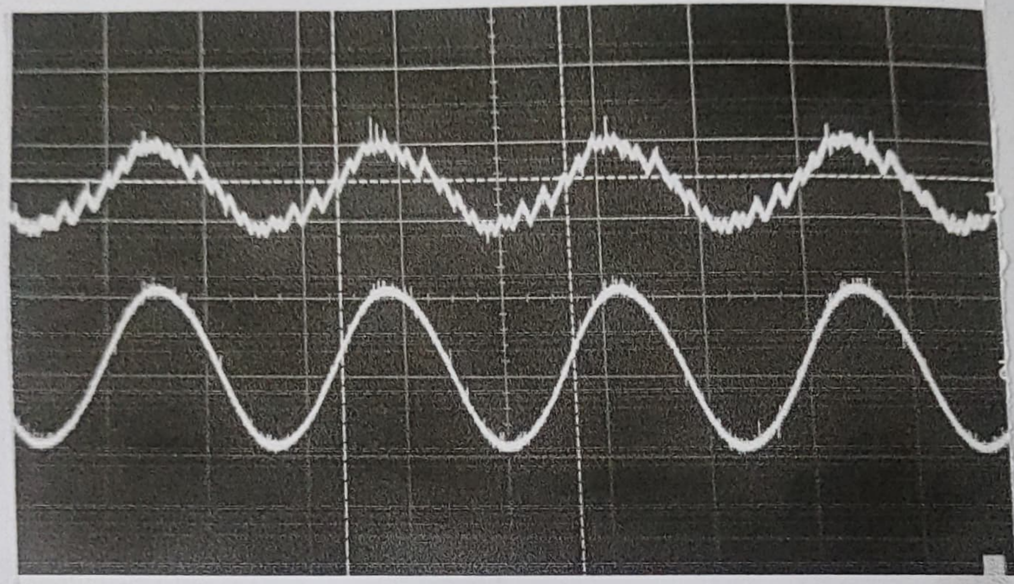
→ THEORY
The type of modulation where the sampling rate is much higher, and in which the step size is of a smaller value Δ, such a modulating is known as Delta Madulation.

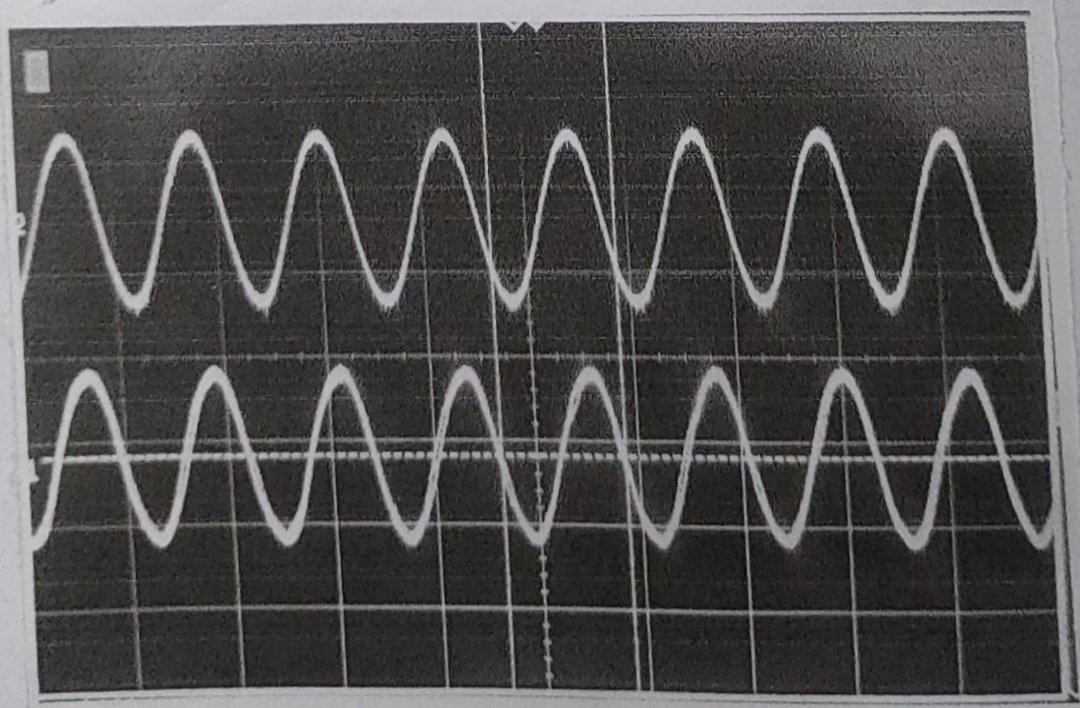
Drawbacks of DM system-
i) It's practical usage is limited.

ii) Slope overload distortion

iii) Granular or idle noise

→ PROCEDURE
- Connect the o/p of unipolar. Bipolar converter to the integrator block.
- Connect the o/p of integrator to i/p of Comparator along with a transmitter clock. (sinsoidal wave of 1kHz.)





# Transmitter and Reciever Block waveform for Delta Modulated Signal.

3- Connect the output of comparator to Bistable block, along with a transmitter clock

4- Give the output of Bistable block to the reciever bistable block input along with a reciever clock. This is connected to UB converter.

5- Connect UB of of UB converter to input of integrator block.

6- Connect the output of integrator and pass it via LPF block. It gives us the demodulated message signal.

7- Connect two probes to CRO, one from the input message signal & other as the output of LPF. Observe waveforms.

→ RESULT & CONCLUSION -

The modulation & demodulation of message signal using Delta modulator Block has been successfully verified.

# EXPERIMENT - 5

→ AIM -
Study of Adaptive Delta modulation (ADM) and Demodulation

→ EQUIPMENT REQUIRED.
- Power Supply
- Delta modulation kit
- CRO
- Probes
- Connecting wires

→ THEORY.
In DM, there is problem of slope over-load and granular noise, where step-size Δ is constant. High step size increases quantization noise. Hence, A new method is developed by using a logic block. We can increase the integrator gain for fast charging input & to use normal gain for small amplitude signals.
The idea is to increase integrator gain when slope overload occurs, if it is still unable to catch up, integrator gain is doubled.

ADM is similar to DM, except the counter & control circuit. Input to control circuit is latched data from D-flip-flop. Counter is reset whenever 'high' occurs at output of control circuit.

Both counter and control circuit are clocked by same Tx clock.

| Control word | Integrator Gain |
|---|---|
| 00 | standard |
| 01 | standard ×2 |
| 10 | standard ×4 |
| 11 | standard × 8. |

→ PROCEDURE-

1- Connect the main supply.
2- Connect the board as per circuit diagram.
3- To Ensure clock switches are in A=0 and B=0 position
4- Ensure TX clock in both counter and control circuit.

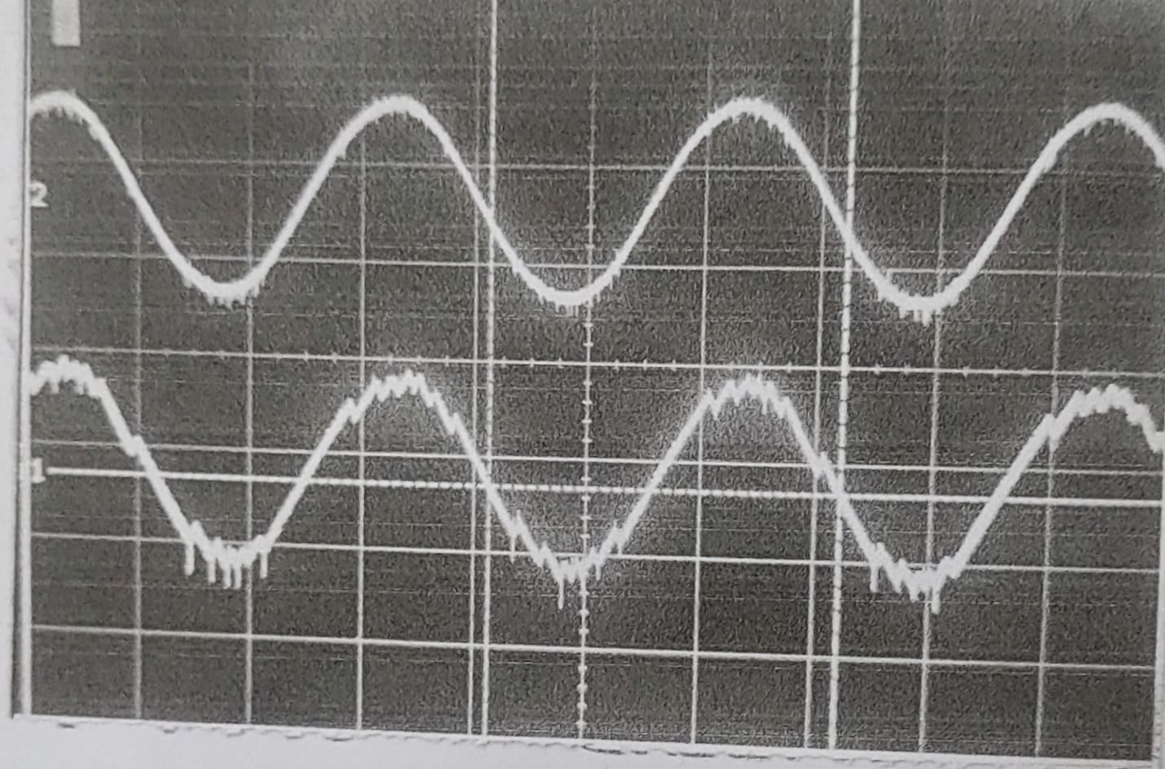
5. Turn all potentiometers and function generators fully clock-wise

6. Turn on the supply.

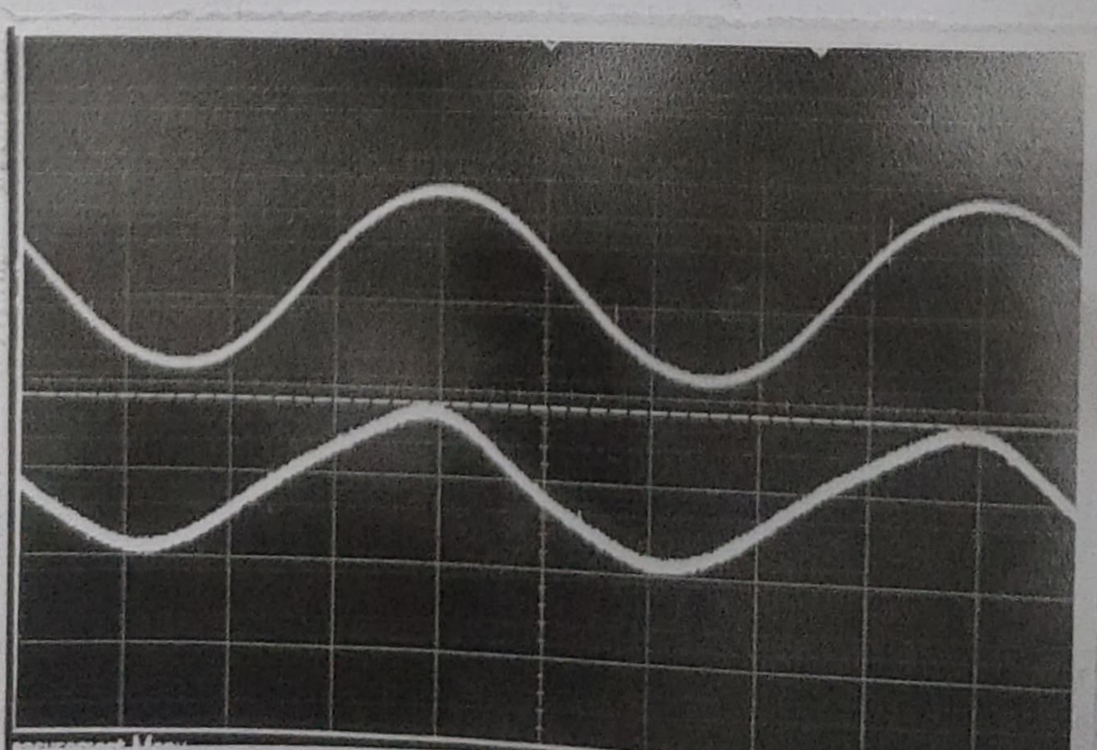
7 Connect comparators +ve to 0V.

8. Change clock A=1 & B=1.

9. Connect supply frequency 1kHz to comparator + and integrator o/p to comparator.



# Transmitter and Reciever Waveform of Adaptive Delta Modulation



10- Connect UBC output to integrator I/P.

11- Connect A & B of integrator and adaptive control unit respectively

12- Connect output of comparator to input of Bistable circuit.

13- Connect O/P of BC to ADC input & Reciever BC input

14- Connet BC output to ADC input of Reciever end.

15- Connect A ~~*~~ B of ADC to integrator input respectively

16- Connect integrator output to LPF input. Check LPF output on the CRO.

→ RESULT & CONCLUSION

We have successfully conducted & verified the adaptive Delta Modulation of given input signal.

# EXPERIMENT-6

## AIM

Study of Delta Sigma Modulation & Demodulation.

## APPARATUS REQUIRED

STO1 lab Trainer kit.
Batch Chords
Power Supply
wires & probes
Cathode Ray Oscilloscope

## THEORY

DM and ADM suffer from two limitations.

1. Not able to pass DC level information
2. (S/N) ratio decreases as freq. increases.

A DSM generally compromices of a delta sigma modulator, followed by a decimation filter. It is one of the most effective forms of conversion in convertor world. The goal of DSM is used to achieve transmission efficiency by transmitting only the changes ($\Delta$) in value b/w consecutive samples, rather than actual samples themselves. ADC & DAC use delta-sigma modulation techniques.

A first order DSM acts as a sub-ADC, comprising of a comparator, an integrator and a sub DAC. Latch operation is usually embedded in comparators

The input signal is sent to difference block, where feedback signal is being subtracted from it. The resulting signal is sent to an integrator and a comparator. Comparator compares a reference voltage with integrations output, and generates a 'HIGH' or 'LOW' accordingly.

In turn, the sub DAC uses the output of sub-ADC and generates one of the two available reference voltages. This reference voltage is passed to difference block to be subtracted from input again. This feedback forces the DAC's output average to be equal to to input signal. The DAC's output is an analog representation of its input, which is the demodulators output.

— PROCEDURE

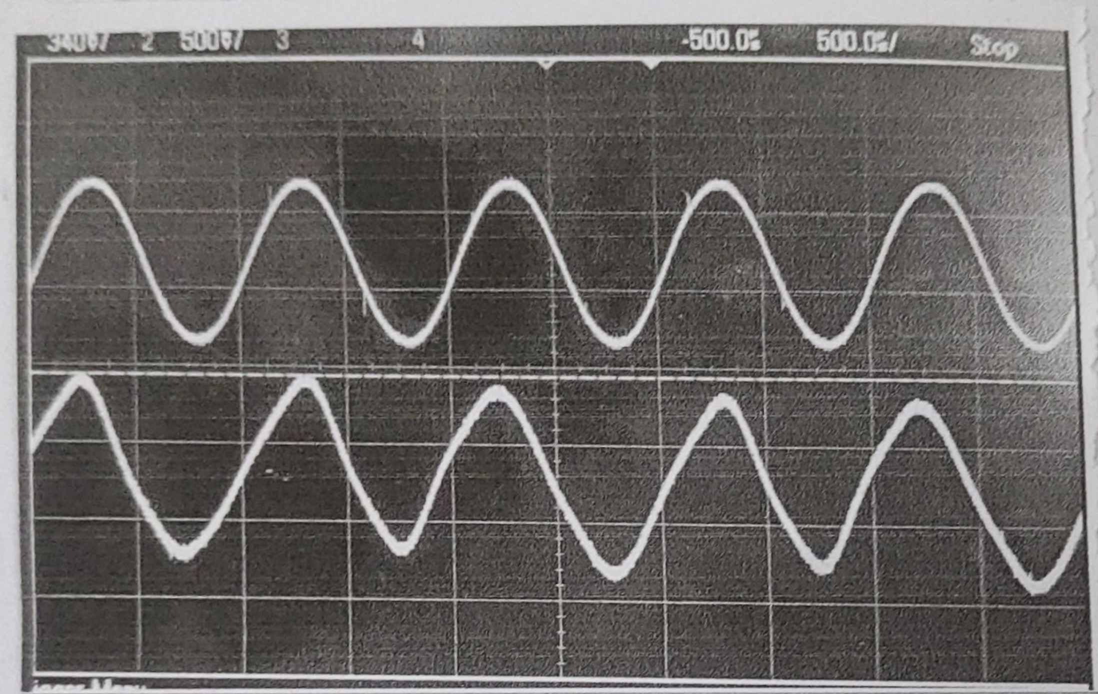
- Connects mains supply
- Makes the connections as per block diagram
- Make A=1 & B=1 freq. selector.
- Turn ON power supply
- Set the freq at 256 KHz.
- Examine analog input (tp5), DA output (tp8), integrator output (tp 17), comparator output (tp1)
- At demodulator, examine BS output, level changes output (tp 34) & LPF output (tp51
- Return AMP of analog input signal to 5V

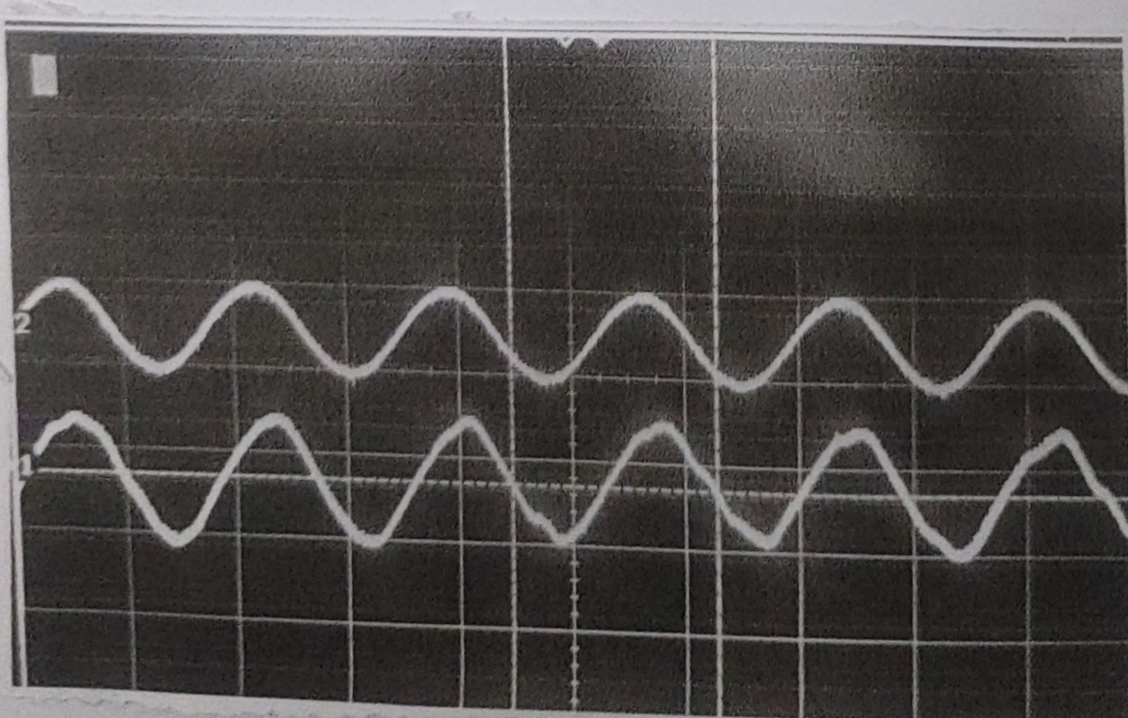
- Remove DA's ⊕ input from function generator's 250 kHz & reconnect with other frequencies.

- Finally connect DA's ⊕ input to function generators DC level. Hence, delta sigma can handle DC input as well.

→ RESULT & CONCLUSION

The observation & verification of Delta - sigma modulation in different levels of AC & DC input functions is successfully conducted.



# Transmitter and Reciever Waveform of DSM modulation.

# EXPERIMENT-07

→ **AIM**

Study of Amplitude shift keying (ASK) modulation & Demodulation.

→ **APPARATUS REQUIRED**

ST 2103 Trainer kit
ST 2104 Trainer kit
ST 2103 Trainer kit.
Power Supply
Probes
Patch Chords

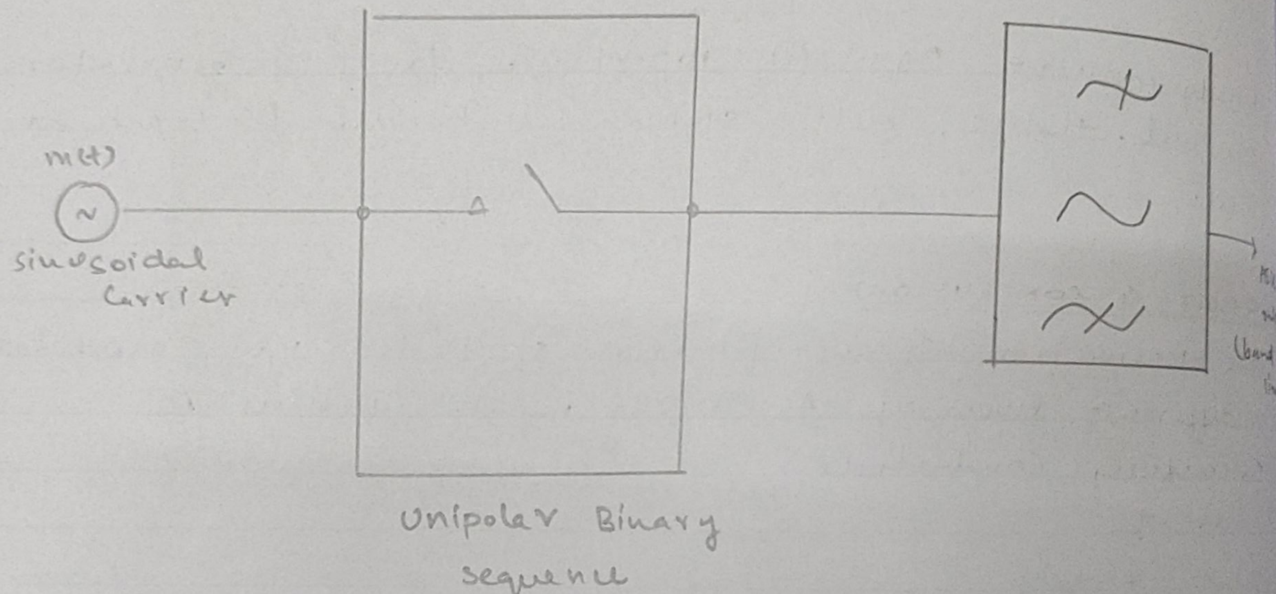
→ **THEORY OF ASK**

ASK is a type of amplitude modulation scheme which represents binary data in form of variations in the amplitude of a signal.

Any modulated signal has a high frequency carrier. The binary special, when ASK modulated gives a zero value for low input while it gives carriers output for high input.

ASK modulator Block comprises of carrier signal generator, binary frequency from message signal and a band-pass filter. The carrier generator sends a continuous high freq. carriers. Binary sequence from message signal makes unipolar input either high or low. High

× ASK Generator



High signal doses the switch, allowing a carrier wave
Hence, the output will be carrier signal or high input.
when there is low input, switch opens, allowing no-voltage
to appear. Hence, output will be low.

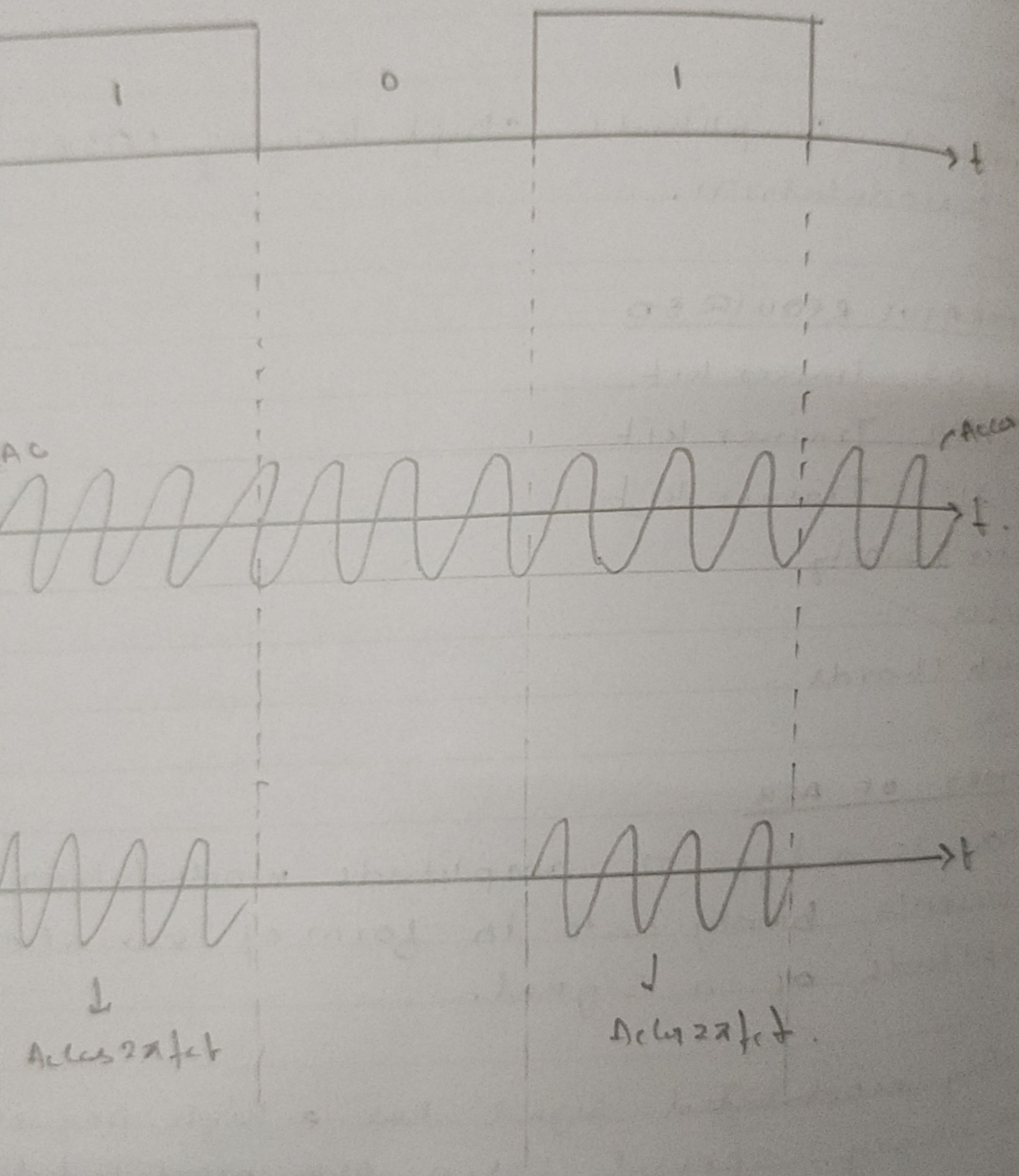
The bandshaping filter, shapes the pulse depending upon
amplitude & phase characteristics of band pass filter.

- ASK Demodulators.
  - → ASK Asynchronous Detector
  - → ASK Synchronous Detector.

## PROCEDURE

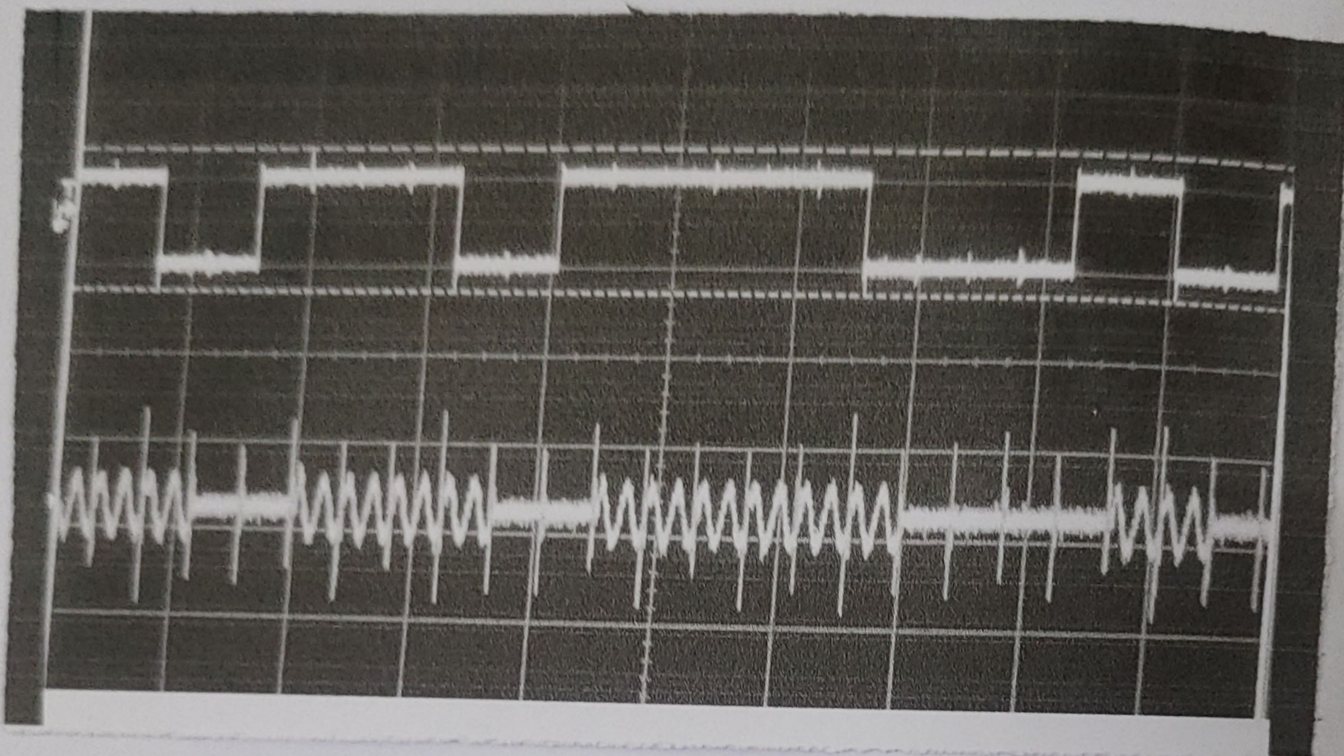
- Follow steps 1-13 from experiment 1.
- Switch off power. Connect additional board as shown in fig.
- Connect ST2106 trainer & ST2107 circuit as per the given circuit diagram.
- Connect ST2104 trainer as per the given circuit diagram

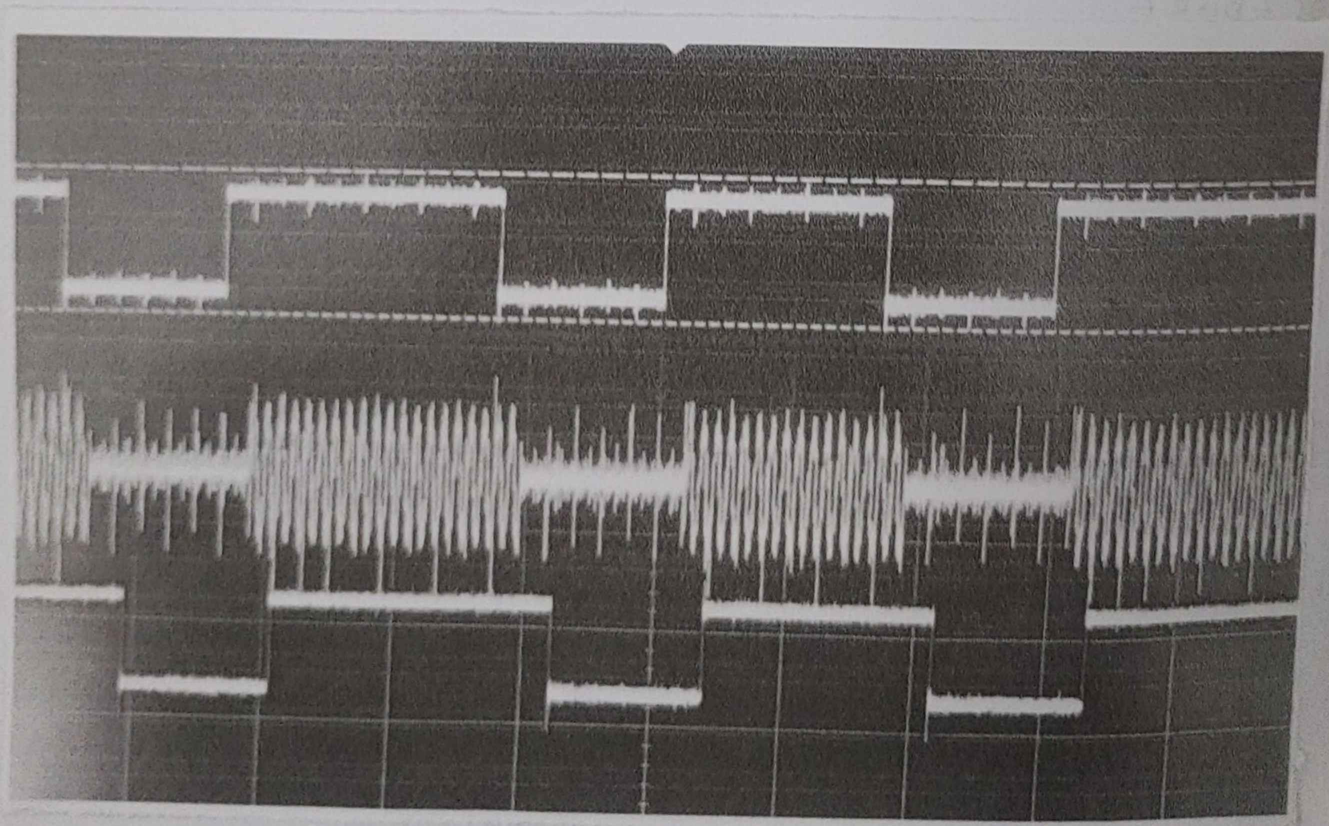
Modulation



→ RESULTS AND CONCLUSION

The modulation of a given bitstream using ASK (Amplitude Shift Keying) has been successfully inducted using a cathode Ray oscillator (CRO).





# Transmitter and Reciever Waveform of ASK modulation.