Design of Class F Power Amplifier for 433 MHz

I.S. Akila, A. Sankar Kalidas, S. Satheesh Kumar, T. Kavi, P. Sujithraj

Abstract: ***The proposed work focuses on the design of a class F power amplifier for 433 MHz which can be used for RFID applications. Power amplifier requires high efficiency and low power dissipation, especially in wireless base stations. In this work, class F amplifier is employed to achieve high efficiency by wave shaping the drain terminal waveforms with suitable harmonic termination networks. At the drain terminal, the voltage and current waveform is shaped into square and half sinusoidal waveforms by employing a harmonics control circuit. The designed class F power amplifier using Advanced Design Software (ADS) simulator has yielded the output power of 44.5 dBm in harmonic balancing for the given input power of 30 dBm at the fundamental frequency with the gain of 14.5 dBm. It was evident from the work that the added harmonic control circuit has suppressed all other harmonics except the third harmonic frequency.***

Keywords: Class F Power Amplifier, GaN HEMT, Harmonic Control Circuit, ADS

I. INTRODUCTION

The amplifier is a device that amplifies the input power to the required output power. Amplifiers are the major power consumers on the transmitting chain since they use DC power for amplification process. So, the power consumption of these devices must be set on optimal levels, considering the requirements. Amplifiers have been divided into various types based on their frequencies and modes of operation. Based on frequency, the amplifiers have been divided into two types, namely, audio power amplifiers and radio power amplifiers. Other classifications include biasing class amplifiers and switching mode amplifiers. Class A, B, AB, and C belong to biasing class amplifiers and Class D, E, and F belong to switching class amplifiers. In class A power amplifiers, the operating point will be in the mid of the load line which gives 50% efficiency because the transistor was ON for the entire range of operation and the conduction angle is 360^0.These types of amplifiers were very useful in audio amplification applications. In class B amplifiers, the operating point is adjusted in such a way that the conduction angle is 180^0. Class B amplifiers introduce phase distortion, and it will be overcome by class AB amplifiers where the bias point is selected slightly above class B. In class C amplifiers, the bias point is adjusted in such a way that the conduction angle is less than 180^0. In switching mode amplifiers, the transistor drives the circuit by either being in ON and OFF conditions. i.e., it will be driven either into saturation or cut-off region. In class F amplifiers, wave shaping networks are used at the drain terminal to shape the voltage and current waveforms. In this wave, shaping is used at harmonic frequencies to yield higher efficiency. The power dissipation occurs when there is an overlap between voltage and current waveforms and using nonoverlapping waveforms are obtained to achieve 100% efficiency ideally. The rest of the paper is organized as follows. Chapter 2 discusses works done in the literature across their pros and cons. Chapter 3 presents the proposed system design. Chapter 4 presents and analyses the results of the proposed work. Chapter 5 concludes the findings of the work and addresses the future scope of the work.

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***** Correspondence Author

Dr. I.S. Akila, Assistant Professor, Department of ECE, Coimbatore Institute of Technology, Coimbatore, (Tamil Nadu), India. E-mail: akila@cit.edu.in

A. Sankar Kalidas*, UG Scholars, Coimbatore Institute of Technology, Coimbatore, (Tamil Nadu), India.

S. Satheesh Kumar, UG Scholars, Coimbatore Institute of Technology, Coimbatore, (Tamil Nadu), India.

T. Kavi, UG Scholars, Coimbatore Institute of Technology, Coimbatore, (Tamil Nadu), India.

P. Sujithraj, UG Scholars, Coimbatore Institute of Technology, Coimbatore, (Tamil Nadu), India.

II. LITERATURE SURVEY

In [1], the class F power amplifier was designed for the base station applications. This work depicts selection of operating frequency at 850 MHz and Gallium Arsenide Field Effect transistor (GaAs FET transistor) is used.Also, it describes various design procedures such as bias point selection, bias circuit design, load pull simulation, and input and output matching network design in ADS Software. The proposed design yielded 61.22% of PAE at 1 dB compression with maximum output power of 22.31 dB. The paper [2] discusses various material properties and device properties of GaN material. It was inferred that GaN has high output power density, helps in size reduction, less circuit complexity, higher efficiency, and wider bandwidth. The paper also depicts that the output power increases four times than the usage of GaAs. The Doherty power amplifier, envelope tracking, and linearity enhancement techniques increases the efficiency and digital pre-distortion technique were also discussed. In [3], Thevenin impedance is used instead of load-pull analysis to find the optimum load condition. In this method, open circuit voltage and short circuit current is measured to calculate the load impedance. The load impedance value obtained from the Thevenin impedance method deviated more from the load condition obtained from load-pull analysis if the circuit was biased nearer to the class F region and the load impedance of Thevenin impedance was close to the results of load-pull analysis if it was biased nearer to class A region. In this bias point is modified between class A and class F, to yield optimum efficiency.

The final circuit yielded PAE of 79.6% with output power of 23.2 dBm for 21.8dBm of input power. The work in [4] presents a load-pull approach to find the optimum load impedance. In ADS, the tone load-pull design guide is used to find the load impedance and it calculates various output values iteratively by varying input sources. Also, a substitute technique of deriving reflection coefficients instead of using large signal S parameters was explained for the matching network. The proposed circuit yielded 78% of Power Added Efficiency (PAE) at 30 dBm of output power. The work in [5] concentrates more on reducing the size of the output matching network. Meandered Line Compact Microstrip Resonant Cell (MLCMRC) was suggested as a harmonic control circuit (HCC) size reduction technique. In this paper, resonator size reduction has been carried out in two phases. Initially, the long open stubs were replaced as shorter folded stubs (folded with calculations) and then the centre strip is also folded to yield a more compact size and it suppressed the third and fifth harmonics correctly. It reduces the size of the resonator by 82% compared to its primitive resonator. It not only resulted in size reduction, but also resulted in the improvement of gain by 5% and PAE (Power Added Efficiency) by 10%. Also, this resonator size reduction has resulted in a 36% of size reduction in the overall circuit of the class F power amplifier. The circuit yielded 74% of PAE under 15 dBm of input power.

In [6], the author proposed a class F amplifier to the fundamental frequency of 433 MHz. The paper focused on the input and output matching network and considers the usage of second and the third harmonics for matching network. It was inferred that an optimum efficiency is yielded for the input power of 13 and 18 dBm. The paper [7], discusses about Switch Mode Power Amplifiers (SMPAs) which offers higher efficiency and can be used for wide frequency applications. The author proposed bandpass filter for the output matching network with microstrip lines to offer 11.6 to 14.5 dB gain and an output power of 41.15 to 41.9 dBm for the frequency band of 850 MHz to 1.8 GHz. In [8], the authors have harmonic control circuit for class F amplifier using FCTCMRC which acts as the short and open for second and third harmonics for 1.1 GHz. It was inferred that class F power amplifier yielded 86% PAE for 10 dBm input power. [9], depicts the design of class F power amplifier for the GSM applications. The author proposed SMLCMRC technique proposed for harmonic control circuit and was designed for 1.8 GHz and the experimental results was observed that 16.5% PAE improvement and 1.33 dB increase in gain.

From the literature survey, it is inferred that there is a need for designing an optimal amplifier for meeting the requirements of RFID applications across various performance parameters.

III. SYSTEMDESIGN

Fig 3.1 depicts the structure of class F power amplifier. The Class F power amplifier is a switching mode amplifier that achieves 100% ideal efficiency based on suppressing harmonic frequencies at the drain terminal. A harmonic control block is used to suppress all harmonic frequencies except fundamental frequency. In the proposed work Class F power amplifier design CGH40025 - GaN transistor was chosen operating at 28V, 30W saturation power, 62 % efficiency at saturated output power and 6 GHz of operation. The system consists of the following subsystem

- Input Matching Network
- Stability Network
- Harmonic Control Circuit
- Output Matching Network

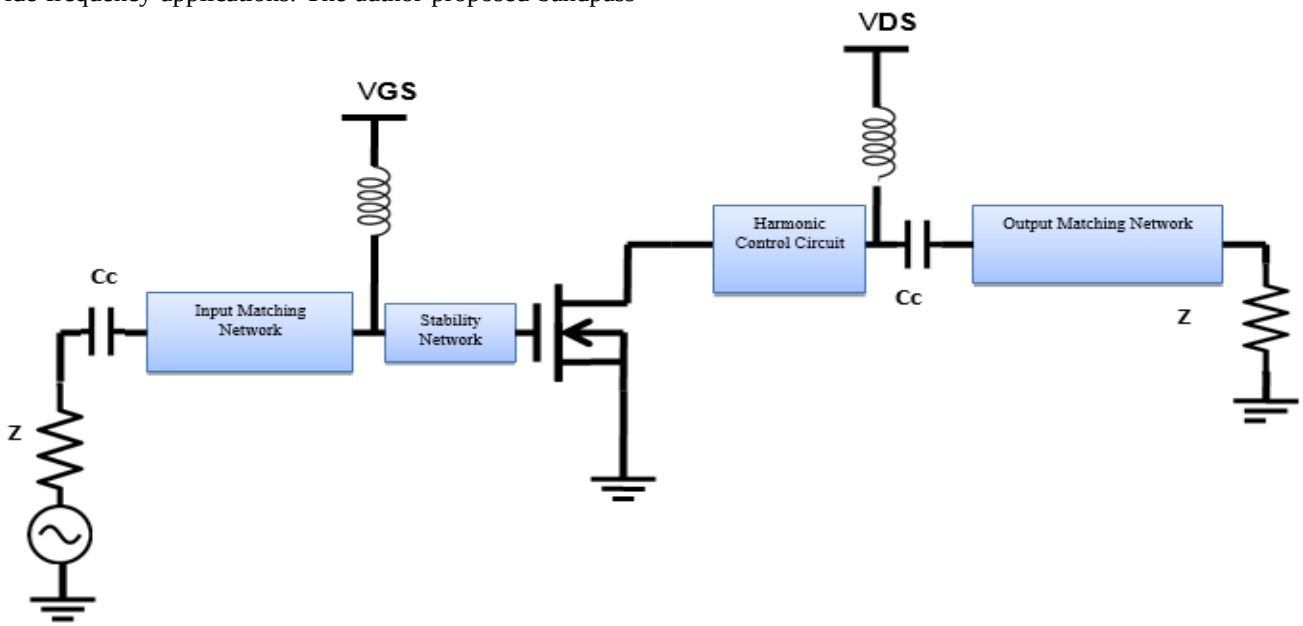

Fig 3.1 Class F Power Amplifier

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A. Dc Iv Simulation

The transistor needs to be biased at a certain point for its proper operation and depending upon the circuit output requirement the transistor can be biased at any class such as A, B, AB, etc. for its operation. The DC IV simulation gives the drain and gate voltage sources values i.e., VDS and VGS respectively as shown in Fig 3.2.

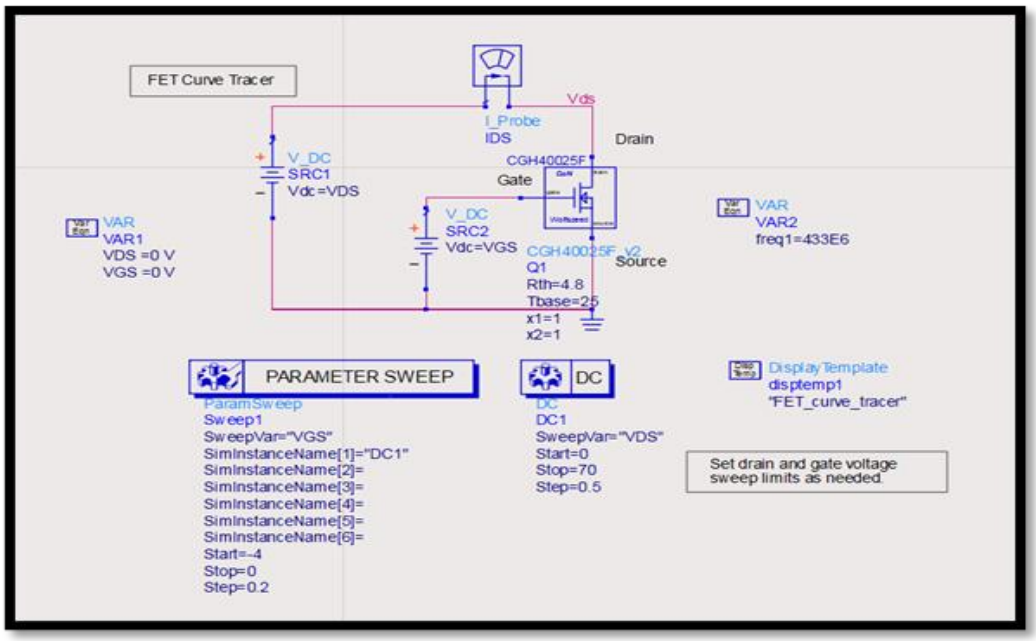

Fig. 3.2 FET Curve Tracer

B. Stability Analysis

The class F amplifier needs to be stable for the entire range of operation. The Rollet Stability Factor defines the condition for stability. It uses S parameters for the calculation and the result should be greater or equal to unity.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + \Delta^2}{2\,|S_{12}||S_{21}|} \qquad \ldots\ldots\ldots [1]$$

where Δ = S11S22 – S12S21 and K ≥ 1.Eqn. [1] depicts the Rollet stability condition and if the condition fails i.e., K<1 then the circuit might lead to oscillation. **Initially** in the design, the K factor was less than one for the transistor CGH40025 at 433 MHz hence, a series resistor of 20 Ω was added in series to make the transistor stable as shown in Fig 3.3.

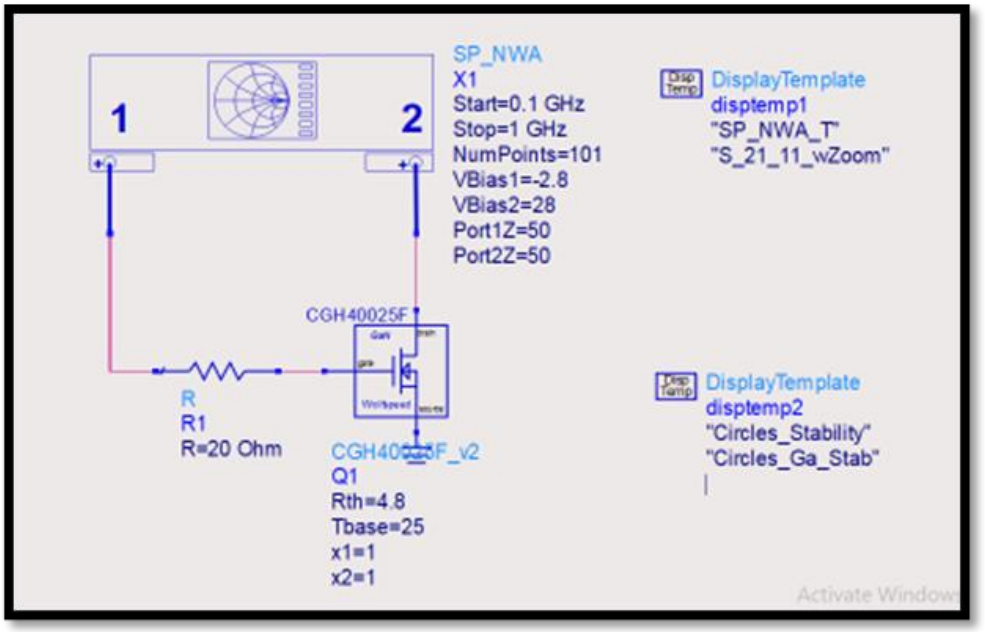

Fig 3.3 Stability Analysis

C. Load-Pull Analysis

The optimum load and source impedances should be determined for efficient operation. The load impedance and source impedance should be optimized for maximum power to be at the load terminal. One tone load-pull simulation template in ADS software as shown in Fig. 3.4gives load and source impedances and plots various power contours and PAE contours for various load and source impedance.

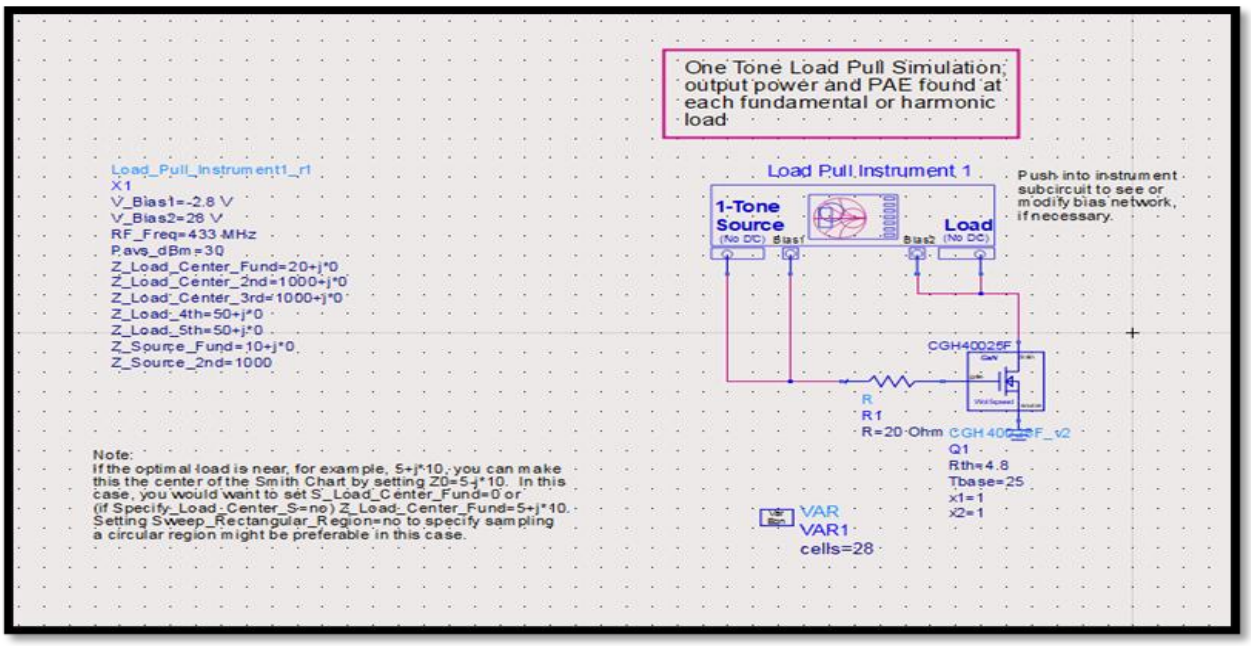

Fig 3.4 Load Pull Analysis

D. Output And Input Matching Network

The load impedances obtained from load-pull analysis should be matched to avoid power losses. Similarly, source impedance matching should also be done to match source impedances. Impedance matching as depicted in Fig. 3.5 & 3.6is done based on Smith chart utility for both source and load impedances and transmission lines were used for matching the impedances. The input or source impedance should be synchronized with the output impedance.

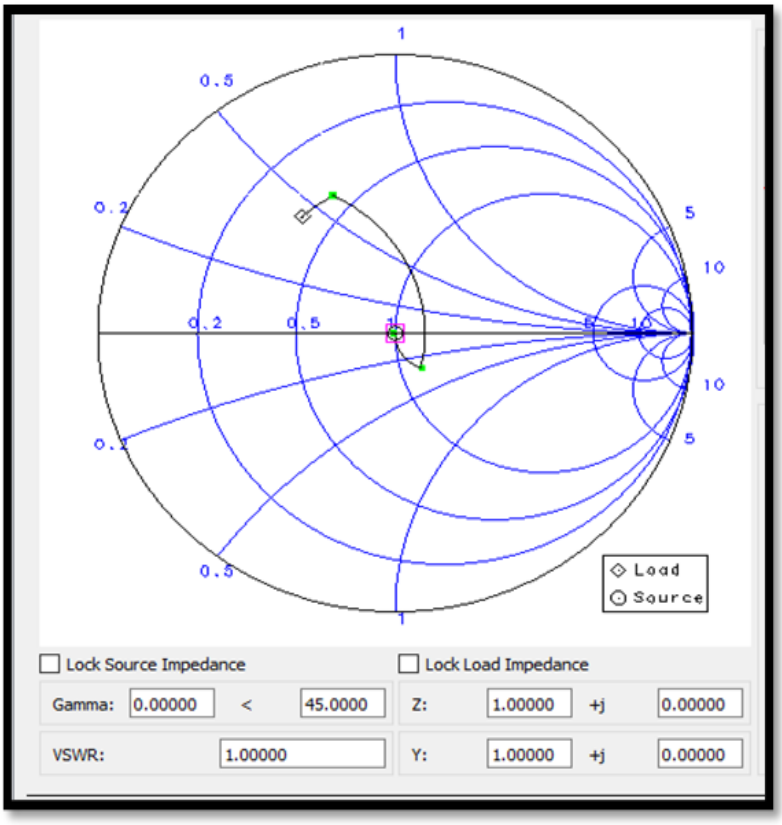

Fig 3.5 Input matching using smith chart

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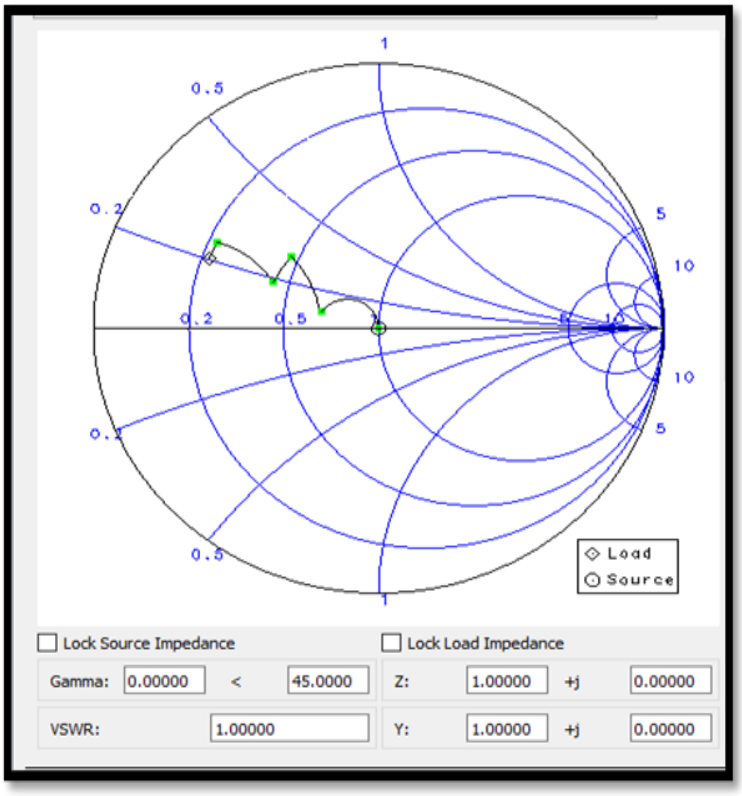

Fig 3.6 Output matching using Smith chart

E. Harmonic Balancing

Harmonic balancing simulates the power levels available at various harmonic frequencies through which we can optimize and simulate the circuit. The harmonic control circuit is added in addition to the input and output matching network and biasing voltages in the circuit. The added harmonic control circuit suppresses the harmonics to a good extent and delivers good power at the fundamental frequency.

IV. RESULTS AND DISCUSSION

A. Dc Iv Characteristics

In DC IV Simulation, DC IV Characteristics of a CGH40025are plotted for various values of VDC and VGS voltages by sweeping the parameters iteratively as shown in Fig 4.1. The load line has been and then, marker m_1 is adjusted as per the need. In this design, the bias point is selected slightly above the cut-off region and the selected bias voltages were VDS = 28V and VGS=-2.8V.

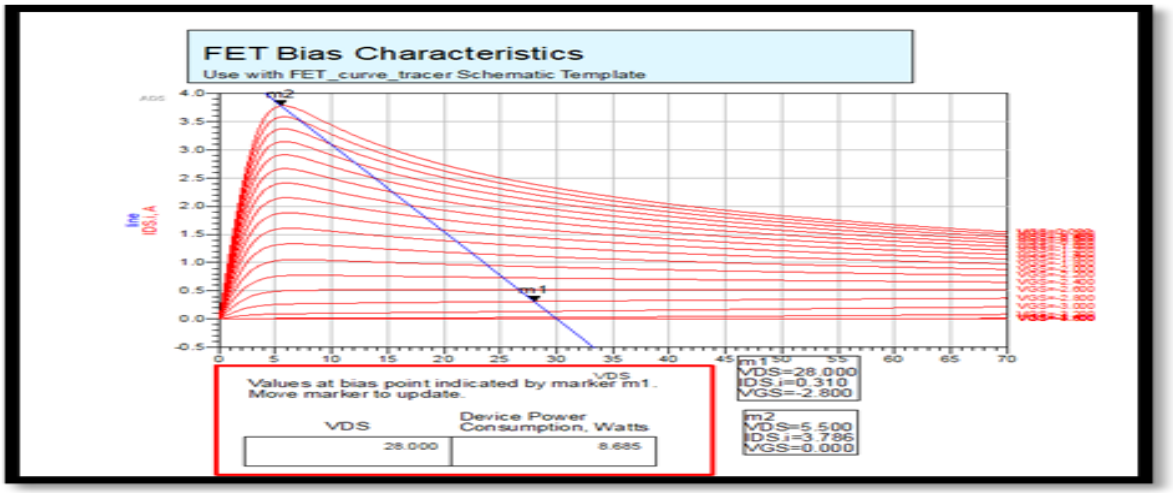

Fig 4.1 DC IV Characteristics

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B. Stability Circles

The stability analysis ensures the stability of the selected device at the operating frequency. Initially, the circuit was not stable at 433 MHz and a series resistor of 20 Ω was added to make the device stable. The stability analysis gives the value of the Rollet stability factor (K) along with some additional parameters such as maximum gain possible, stability circles, etc. The stability value of 2.496 is achieved with the maximum gain of 22.51 dBm as shown in Fig. 4.2.

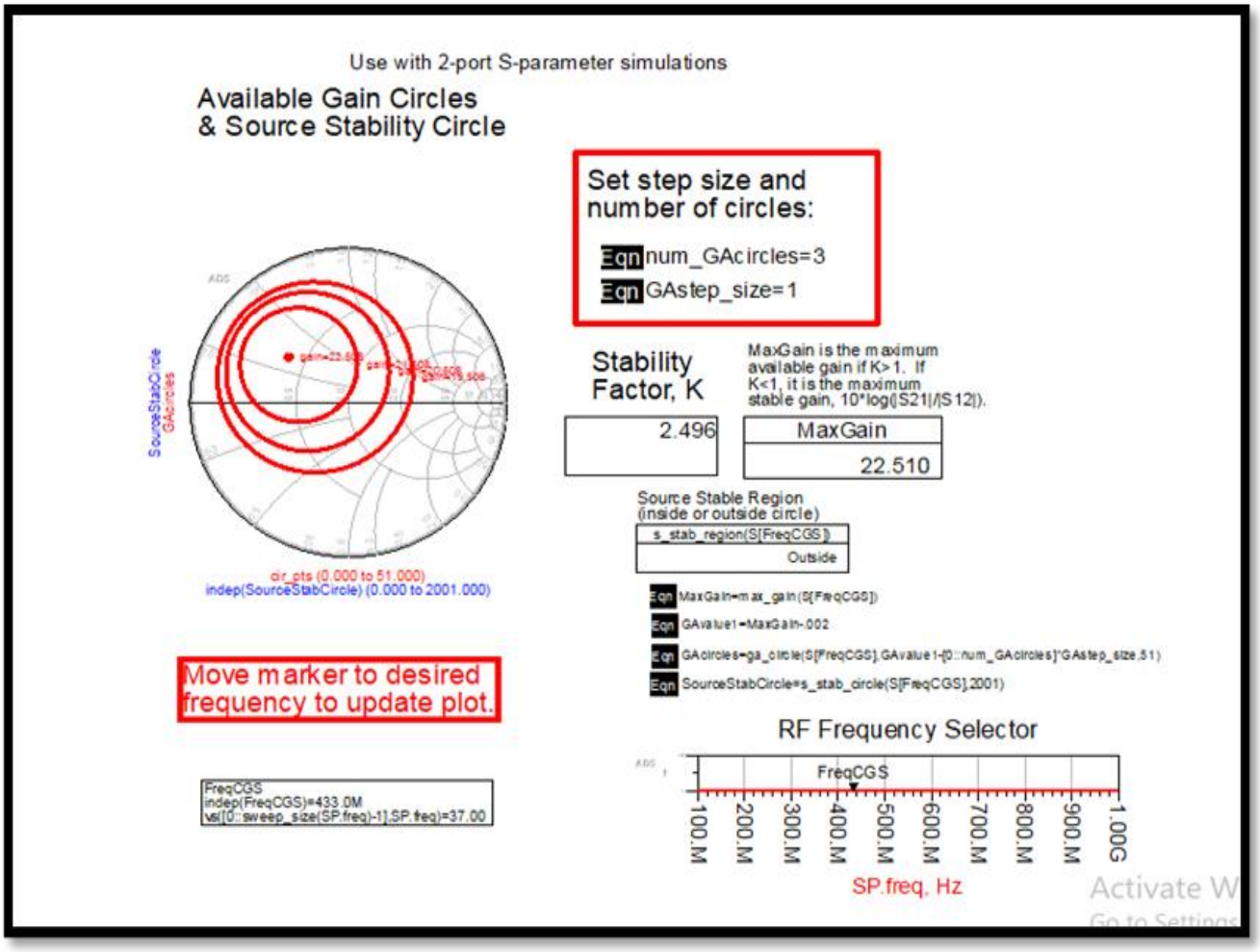

Fig 4.2 Stability Circles

C. Load-Pull Analysis

Load-pull analyses were performed to find optimum load impedance and source impedance. Any suboptimum load and source values may collapse the gain of the entire design. Load pull simulations generate power contours and PAE contours of various values in the smith chart and the calculated the load and source impedances for maximum power as shown in Table 1.

Table 1. Summary of Load pull results

Input Power: 30 dBm	
Parameter	**Obtained Values**
Z_L	11.069+j10.224
Z_{in}	18.892-j22.146
Maximum Gain	15.5 dBm
Maximum Power Delivered	45.5 dBm

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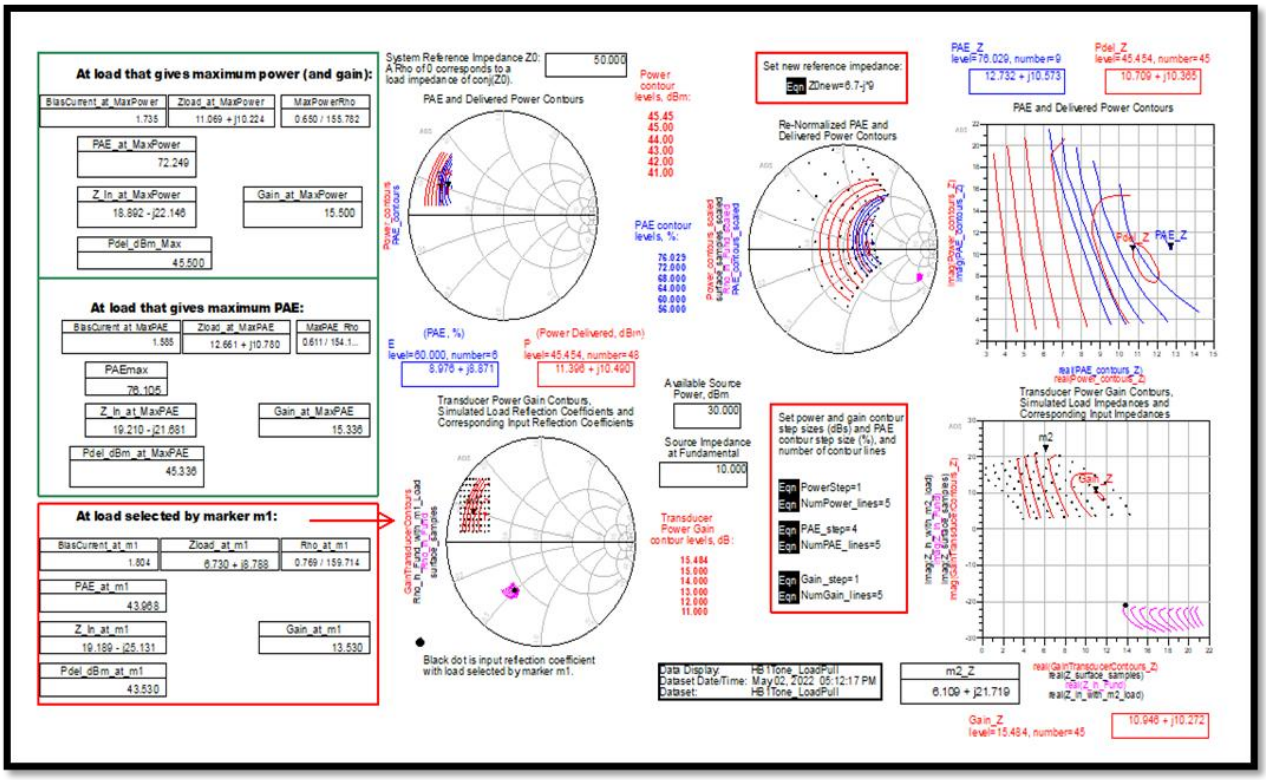

Fig 4.3 Load pull simulations

Fig 4.3 shows the load-pull simulations which are simulated from the load-pull analysis. It generates power contours and PAE contours of various values in the Smith chart and calculates the load and source impedances for maximum PAE and maximum power as shown in Fig 4.4 and Fig 4.5. The selected load and source impedances were 11.069+j10.224 and 18.892-j22.146, respectively.

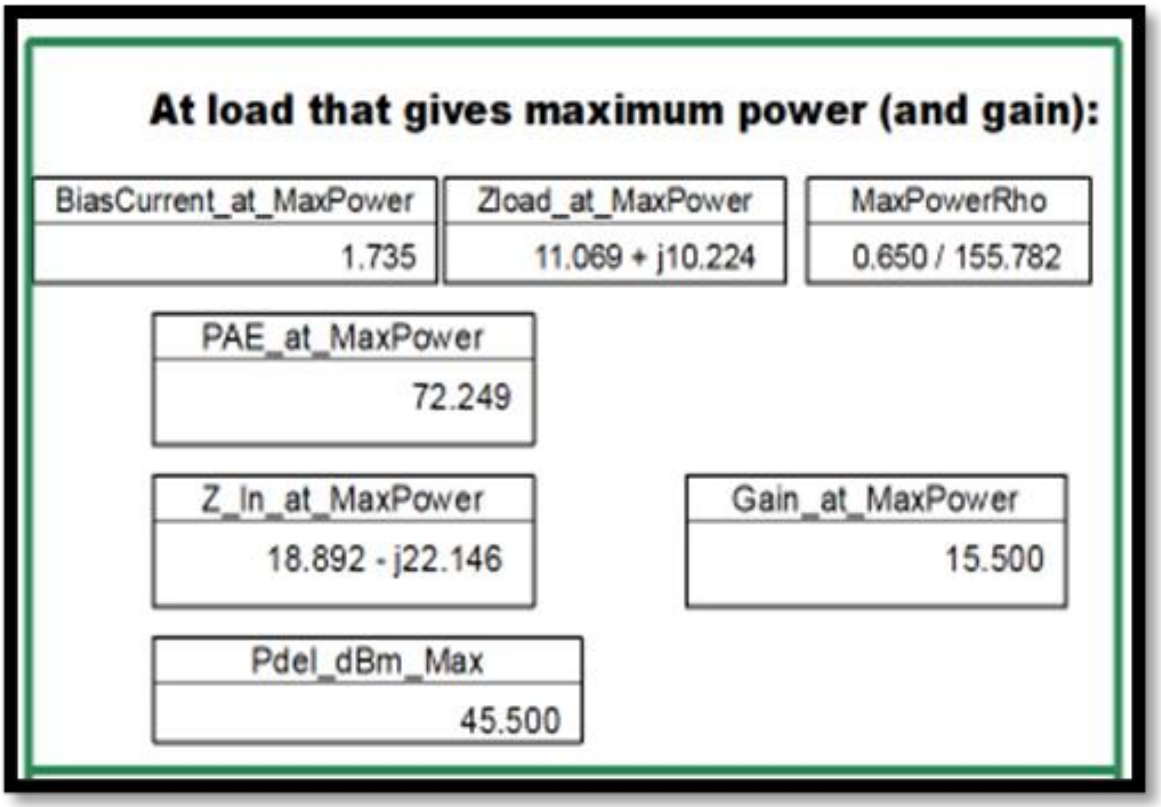

Fig 4.4 Load Impedance for Maximum Power

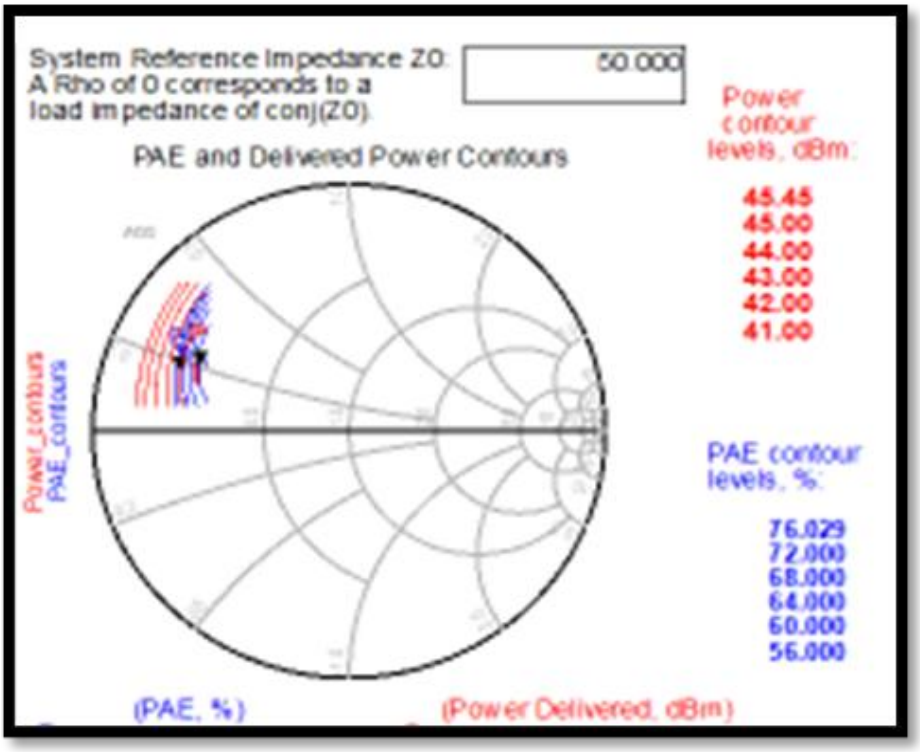

Fig 4.5 Power and PAE Contours

D. Output Matching Network

Impedance matching is done based on the Smith chart utility for both source and load impedances and transmission lines were used for matching the impedances. Fig 4.3 shows the network response of the designed output matching network, and the designed network converges at 433 MHz.

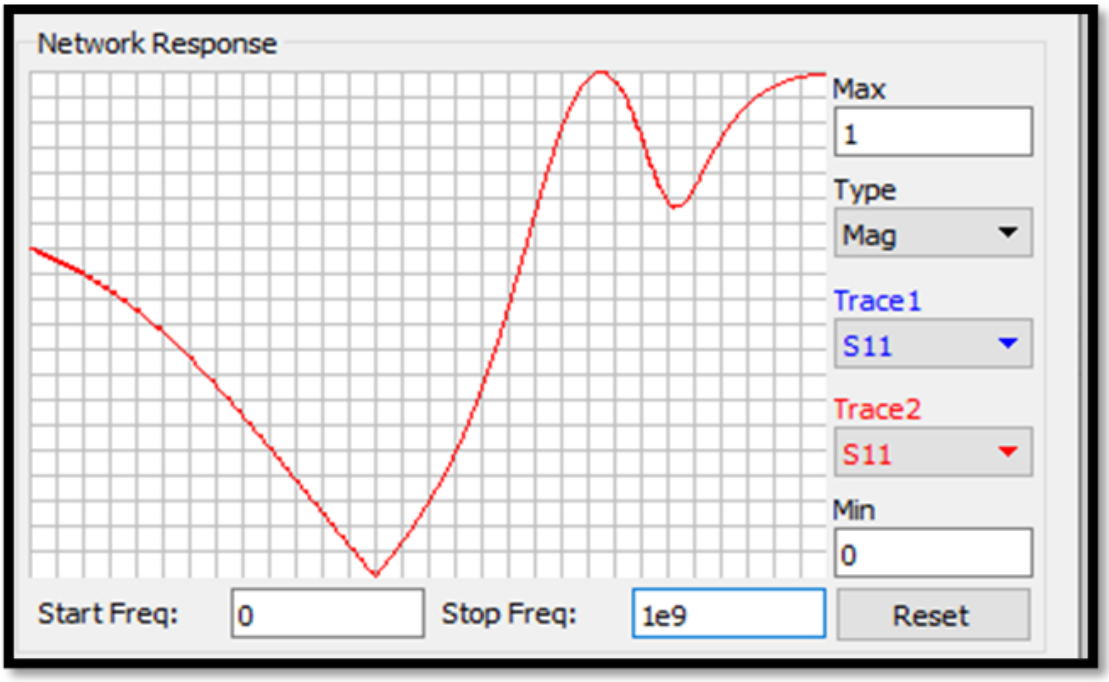

Fig 4.6Output matching network response

E. Input Matching Network

The input matching should also have to be achieved for source impedance to match the output network. Fig 4.7 shows the network response of the input matching network for the range of frequencies from 0 to 1 GHz and as before the input matching network converges at 433 MHz.

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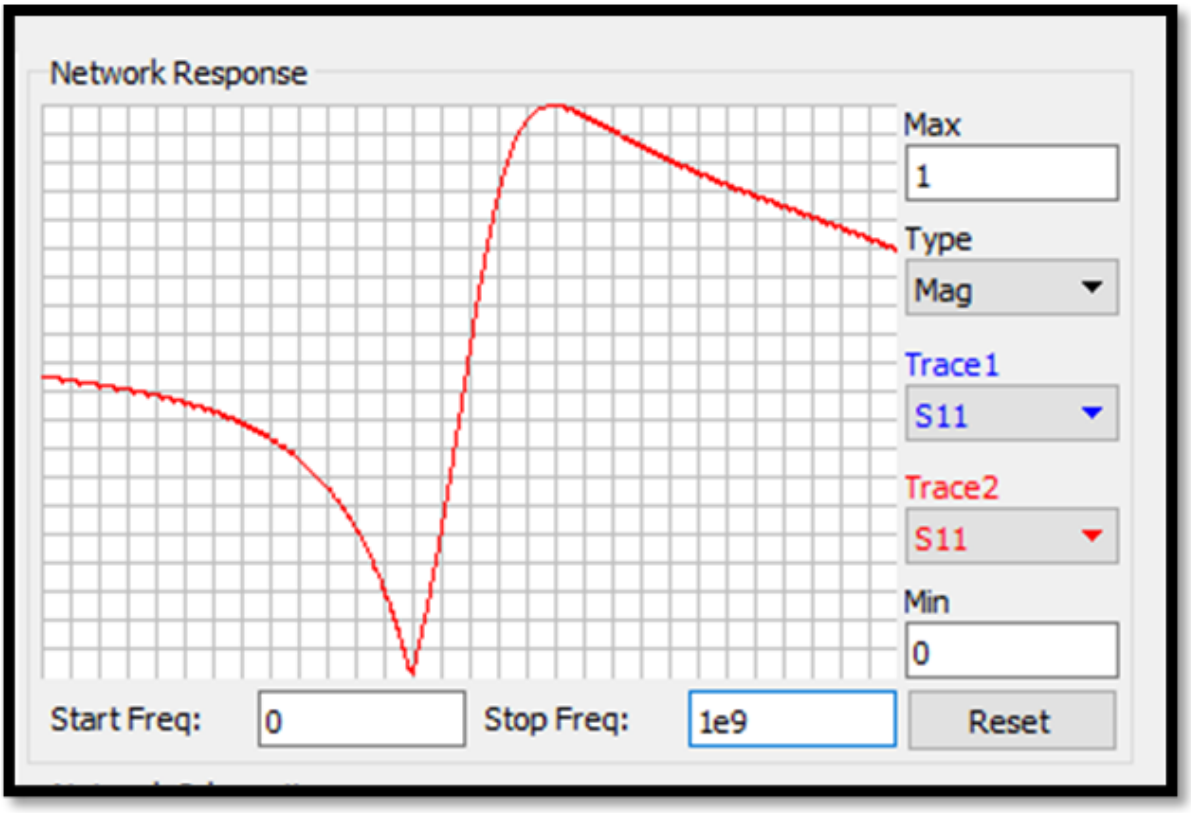

4.7 Input matching network response

F. Harmonic balancing simulations:

Harmonic balancing simulations were performed to identify the power levels available at various harmonic frequencies. This is very helpful to visualize when we try to optimize the power values at harmonic frequencies. Fig 4.8 shows the harmonic balancing circuit which is used to simulate the power levels at various frequencies.

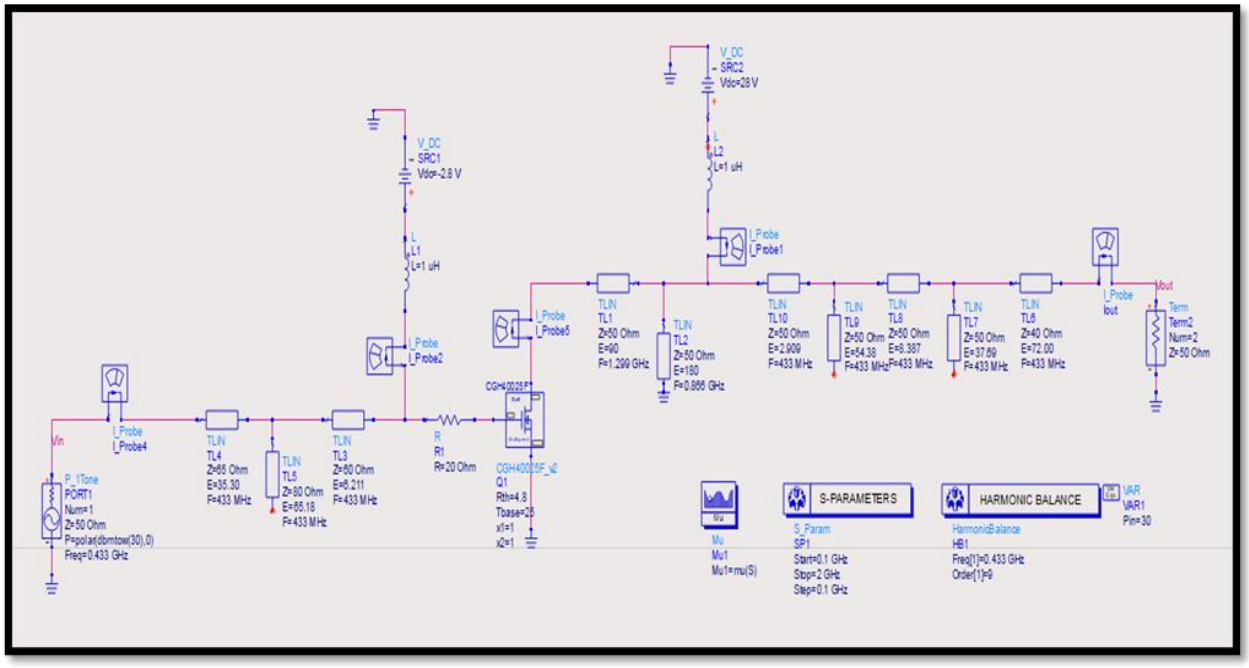

Fig 4.8 Harmonic balance simulations

Table 2 represents the power values simulated as a result of harmonic balancing simulations and from that, it is evident that the even harmonic frequencies were compressed completely, and the odd harmonics were also compressed except for third harmonics and its values are listed in the. This suppression at harmonic frequencies was contributed by the harmonic control circuit added at the output terminal before the output matching network.

Table 2 Power Values at Harmonic Frequencies

Frequency	Output Power
433 MHz	44.585 dBm
866 MHz	-160 dBm
1.299 GHz	25.545 dBm
1.732GHz	-180 dBm
2.165 GHz	2.168 dBm

Based on the results it is evident that the designed power amplifier yielded 44.5 dBm output power at the fundamental frequency for the given input power of 30 dBm. The added harmonic control block was good in suppressing the power level harmonic frequencies. It suppresses the power level below 0 dBm for all harmonics except the third harmonic frequency.

V. CONCLUSION AND FUTURE SCOPE

The proposed class F power amplifier has been designed with DC IV characteristics, stability analysis, load pull analysis for load and source impedance and then output, and input matching were done for the selected load and source impedances along with harmonic control circuit. The added harmonic control block was good in suppressing the power level of harmonic frequencies. It suppresses the power level below 0 dBm for all harmonics except the third harmonic frequency. The designed circuit yielded output power of 44.5 dBm with a gain of 14.5 dBm. The future work focuses on reducing the power level at third harmonics since power consumption at the third harmonic is not desired.

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AUTHOR PROFILE

I. S. Akila received her Bachelor’s degree in Electronics and Communication Engineering from Bharathiar University, India. She has obtained her Master’s degree in Applied Electronics from Anna University Chennai, India. She received her Ph.D. in the Faculty of Information and Communication Engineering from Anna University, Chennai, India in 2017. Currently, she is an Assistant Professor in the Department of Electronics and Communication Engineering at Coimbatore Institute of Technology, India. Her specializations include wireless sensor networks, optimization techniques and wireless Communication.

A. Sankar Kalidas currently pursuing his final year of Bachelor’s degree in the Department of Electronics and Communication Engineering at Coimbatore Institute of Technology, affiliated to Anna University Chennai, India. His field of interest includes Embedded Systems, Wireless Communication and Data communication.

S.Satheesh Kumar currently pursuing his final year of Bachelor’s degree in the Department of Electronics and Communication Engineering at Coimbatore Institute of Technology, affiliated to Anna University Chennai, India. His field of interest includes VLSI Design, Image processing and Wireless communication.

T. Kavi currently pursuing his final year of Bachelor’s degree in the Department of Electronics and Communication Engineering at Coimbatore Institute of Technology, affiliated to Anna University Chennai, India. His field of interest includes Embedded Systems, Antenna Design and VLSI Design.

P. Sujithraj currently pursuing his final year of Bachelor’s degree in the Department of Electronics and Communication Engineering at Coimbatore Institute of Technology, affiliated to Anna University Chennai, India. His field of interest includes Antenna Design, Wireless Communication, and Image processing.