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Design of a tunable LNA and its variability analysis through surrogate modeling

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Abstract

In this paper, a tunable low noise amplifier (LNA), which provides a bandwidth of 1 GHz, has been designed. The tunability of the LNA has been achieved by employing MOS varactors in accumulation mode. A shift in the LNA performance has been observed with the change in the total capacitance of the varactors through the control voltage. Starting from 2 to 3 GHz, the proposed tunable LNA provides a noise figure (NF) of less than 3 dB, a voltage gain of 12 dB and higher, while maintaining input and output power matching (S_{11} and S_{22}) metrics at least below −12 dB. The total power consumption of the circuit is 23 mW. Moreover, two case studies that demonstrate the usage of surrogate modeling in RF circuit design have been described. Three- and six-dimensional surrogate models have been built to illustrate the effect of bondwires on the variability of several LNA design metrics.

KEYWORDS

low noise amplifier, MOS varactor, SUMO toolbox, surrogate modeling, tunability, wirebonding

1 | INTRODUCTION

For the last few decades, wireless communications technology has fostered the quest for advanced communication technologies and standards. Novel approaches such as software defined radio have been proposed to provide the most suitable framework that will accommodate the ever-growing demands by the industry. Such systems should be accompanied with proper hardware designs to satisfy the challenging design specifications. The need for high-performance and compact transceivers has therefore resulted in the development of novel circuit topologies. In that regard, RF circuit designs that are capable of satisfying multiple standards simultaneously have been of great interest.[1] A plausible way to realize this concept is to integrate tunable components into the circuit design, thereby allowing adjustments in the circuit performance at different operation frequencies. Such structures embody multiple receiver or transmitters operating at different frequencies in one single transceiver, which yields significant savings in chip estate.

This paper focuses on the design of a tunable low noise amplifier (LNA). LNAs are the first block of a conventional receiver in a communication system. The signal, whose power has been reduced through propagation in air, is received from the antenna and then introduced to the LNA. The LNA is responsible to amplify the signal while adding as little noise as possible. Since the noise performance of a cascade system depends mostly on the noise figure (NF) of the first block, the noise performance of an LNA is critical. Nevertheless, when designing an LNA, the goal is to keep all other specifications within the specifications, as well, so that the best overall performance can be accomplished. Thus, a typical design aims to achieve high gain, high linearity, and low power consumption.

[Correction added on 3 February 2020, after first online publication: The tilde and bar signs in Equations (4) and (5) were incorrectly typeset and have since been corrected in this version.]

In order to make the LNA tunable in frequency, several methods have been employed in the literature. An LNA can be tuned discretely or continuously. In discretely tunable designs, several shunt LC tanks have been employed, or capacitors driven by switches that allow a shift in the input matching are used.[2,3] However, this technique consumes a lot of chip area and does not provide enough resolution in tunability. On the contrary, continuously tunable LNA designs utilize adjustable circuit elements such as variable inductors[4] or varactors.[5] As pointed out by Yelten and Gard,[6] compared with a variable inductor, a variable capacitor is more convenient to fabricate. Hence, the aim of this paper is to design a single-stage, continuously tunable LNA, using only two accumulation-mode CMOS varactors to realize a large tunable bandwidth with an improved performance with respect to similar studies. The LNA has been designed using a commercial 180-nm CMOS technology using the radio-frequency type (RF-type) transistors.

It is important to notice that designing an analog circuit block often requires expensive simulators and a thorough theoretical and practical background knowledge. Because of their continuous nature, nonlinearities and variability problems can become a challenge to the designer. Moreover, the optimization of parameters, which introduce trade-offs in two or more different circuit characteristics, is not a straightforward task, as well. For this reason, in the second part of the paper, the concept of surrogate modeling is introduced, and two case studies have been discussed to show the facilitation of the tunable LNA design process via surrogate modeling. Previous research studies on this subject mostly focused on the enhancement of the surrogate modeling approach rather than the circuit performance.[7-9] Recently, however, several papers have focused on the application of surrogate modeling in the context of microwave antenna optimization.[10-14] Likewise, in this paper, surrogate modeling has been used to aid the process of circuit design. In particular, the main aim focuses on to give insights on the impact of process variability and other nonlinearities observed in the tunable LNA.

The organization of the paper is made as follows: Section 2 is dedicated to the description of the tunable LNA design. Subsequently, the fundamentals of surrogate modeling and its application on the tunable LNA design will be discussed in Section 3. Finally, concluding remarks are made in Section 4.

2 | DESIGN OF THE TUNABLE LNA

In this part of the paper, the design of a tunable LNA will be explained in a methodological approach. First, the design methodology is analytically discussed. Then, the varactors employed will be described. Finally, the simulation results are provided.

2.1 | LNA design

The design specifications of the proposed tunable LNA are shown in Table 1. Designing a tunable LNA is especially critical and difficult at frequencies below 5 GHz as frequency tuning in this range requires larger changes in inductance or capacitance. Thus, the purpose in this design is to operate within a bandwidth of 1 GHz while consuming a small chip area and satisfying all circuit specifications. The values of the circuit component parameters that are used in the LNA design have been provided in Table 2.

As seen in Figure 1, a single-stage topology with a cascode structure and inductive degeneration has been chosen. Cascoding provides a high reverse isolation and a good noise performance, since the noise level of the common gate transistor is degenerated by the output resistance of the common source transistor. However, there will still be some

TABLE 1 Design specifications for the tunable LNA

Spec	Frequency Range	Noise Figure	Voltage Gain	Input Matching (S_{11})	Output Matching (S_{22})
Value	2-3 GHz	3 dB (max)	10 dB (min)	< -10 dB	< -10 dB

TABLE 2 Parameter values of the circuit elements

Param	$W_{M_{1/2}}$	V_{bias}	L_s	L_g	L_d	C_d	L_{in}	C_{in}	L_{out}	C_{out}
Value	105 μm	700 mV	370 pH	4.5 nH	2.25 nH	16 pF	2.5 nH	6.4 pF	4 nH	510 fF

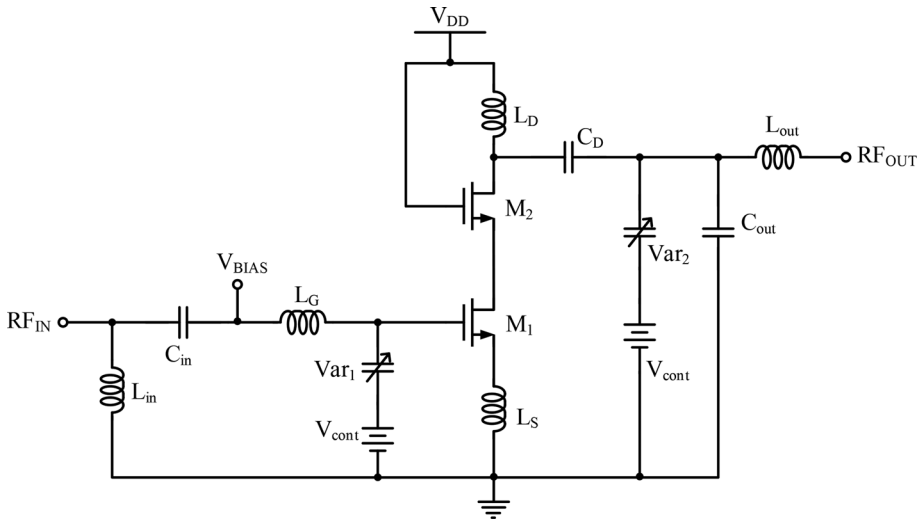

FIGURE 1 The proposed tunable low noise amplifier (LNA) topology

noise contribution of the common source device itself, with the thermal noise being the most impactful component. In the saturation region, parameters such as the transconductance (g_m) and the gate-to-source capacitance (C_{gs}) determine the drain or gate current thermal noise.[15] Therefore, the first step when designing for minimum noise figure (NF_{min}) operation of an LNA is to optimize the drain current density and the channel geometry of the common source transistor. Since NF_{min} is the noise value obtained when the optimum source impedance is presented, the actual NF will depend on the value of source and gate inductors through which NF converges to NF_{min}. Hence, the second design step is to decide upon the values of L_s and L_g. Conversely, since the LNA is source degenerated, the voltage gain (A_v) will be reduced as the value of L_s increases. It is important to mention that the linearity of the LNA changes with current density; therefore, the third-order intermodulation intercept point (*IIP3*) should be checked and optimized.

Another important specification of an LNA is the input power matching in which the input impedance Z_{in} has to be matched with the source impedance of $Z_{in} = 50\ \Omega$. As seen in (1), the input impedance depends on the source and gate inductances, as well. Thus, the optimization of their values is performed considering the NF, gain, and power matching, simultaneously. The voltage gain expression can be derived as in (2), and the real portion of the input impedance due to the source inductance is given in (3).

$$Z_{in} = j\omega L_g + j\omega L_s + \frac{1}{j\omega\left(C_{gs} + C_{var}\right)} + \frac{g_m L_s}{C_{gs} + C_{var}}. \tag{1}$$

$$A_v = \frac{g_m R_L}{2\omega_0 R_s\left(C_{gs} + C_{var}\right)}. \tag{2}$$

$$R_s = \frac{g_m L_s}{C_{gs}}. \tag{3}$$

It should be noted that the expressions of both the gain and the input impedance contain C_{var}. Therefore, when the effective capacitor value of the varactors changes, input and output matching of the LNA, as well as its voltage gain, will shift in frequency. Finally, to complete both the input and the output matching, an LC matching network has been employed with which the values of the remaining matching circuit components are evaluated.

2.2 | Varactors and tunability

As seen in Figure 1, to provide the tunability of the LNA, two varactors have been employed. The positioning of the varactors is such that the input and output impedance matching is shifted in frequency when the control voltage changes the effective capacitance values of the varactors. In the proposed design, an accumulation-mode MOS varactor

from the design kit of the same 180-nm device technology, also referred to as A-MOS, is used. As concluded in various articles,[16,17] A-MOS varactors ensure the highest range of the tunability in comparison with other MOS-types varactors, thereby providing a higher ratio of C_{max}/C_{min} and a less abrupt transition between its maximum and minimum values.

In order to characterize the varactor, simulations have been done in a separate test bench, and the results are shown for the control voltage of interest. The varactor gives a ratio of 2.6 for the C_{max}/C_{min} and an increasing quality factor with the increment of the control voltage. Considering the fundamental definition of a capacitor's quality factor, as the operating frequency goes up, the quality factor of the varactor goes down because of the inversely proportional relation between the two parameters. The latter is demonstrated in Figure 2B in which the lowest quality factor for the varactor is obtained for the highest operating frequency of the LNA.

2.3 | Simulation results

Voltage gain, NF, power matching, and linearity simulations of the proposed LNA have been performed. As seen in Figure 3, the tunable LNA provides a voltage gain of 12 to 15 dB and an NF of less than 3 dB within the range of 2 to 3 GHz. The control voltage is swept from 0 up to the supply voltage, 1.8 V. For demonstration purposes, only five samples of the control voltage have been shown in all of the graphs. Yet, with the increment of the control voltage, the operating frequency of the LNA goes up as well, and the overall performance of the LNA with respect to its voltage gain and NF improves.

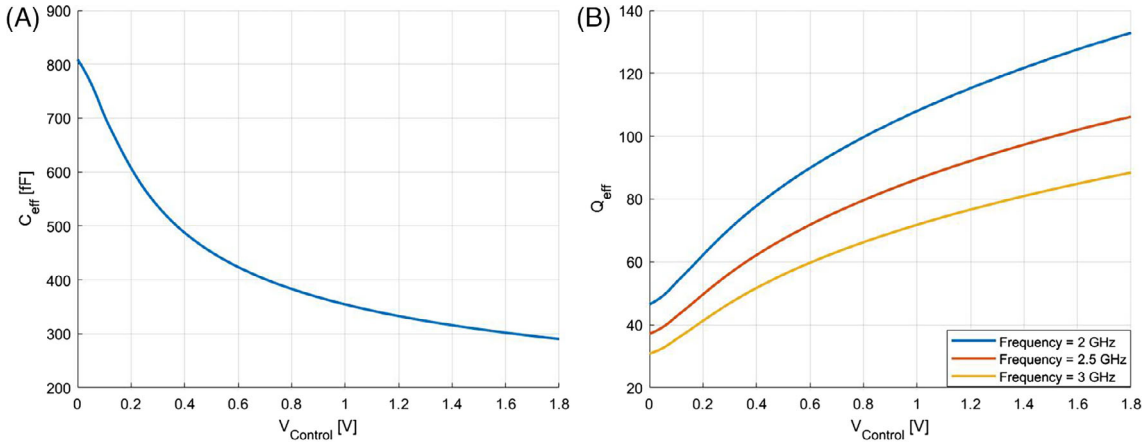

FIGURE 2 (A) The effective capacitance (B) the quality factor of the varactor employed

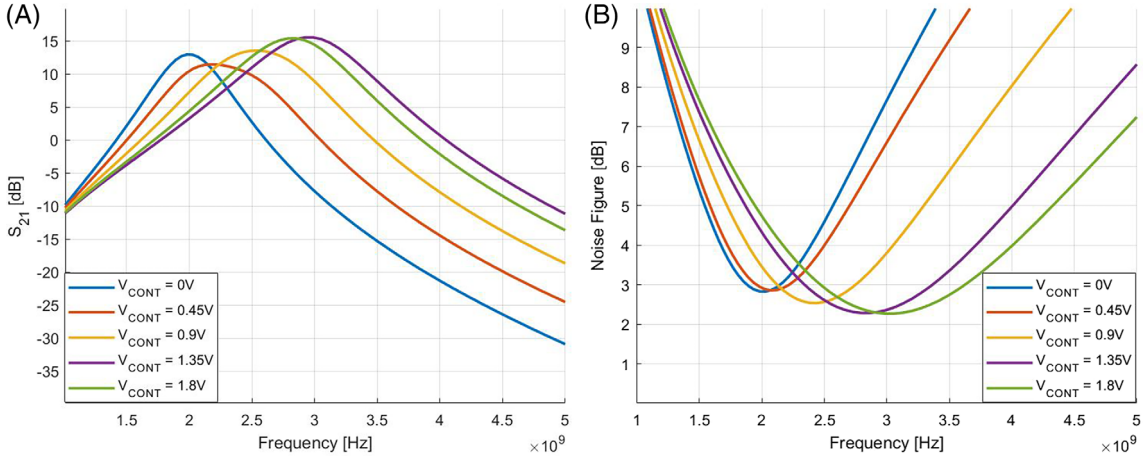

FIGURE 3 (A) The gain and (B) the noise figure of the proposed tunable low noise amplifier (LNA)

To verify the impedance matching between the source and the load of an LNA, the S_{11} and S_{22} parameters are checked, as shown in Figure 4. When the control voltage changes, both parameters are kept below −12 dB, with a better performance in S_{22}. The following results show that the matching of the input/output load impedances to 50 Ω resistance introduced by the input and output ports is achieved with less than 10% signal reflection. In that respect, both the reflected signal power and the resultant noise levels are kept within robust performance ranges.

Another important specification for the performance of a LNA is its linearity. A meaningful merit to measure the latter is the third-order intercept point (*IIP3*). Figure 5 shows the *IIP3* simulation results for the case at which the control voltage reaches the supply voltage level. The achieved *IIP3* is −1.019 dBm while the operating frequency is 3 GHz. However, as shown for the other designed specifications, the low frequency operating points have demonstrated a diminished performance in linearity. Table 3 presents a summary of the *IIP3* values at different frequencies.

Table 4 depicts a comparison of several tunable LNAs reported in the literature with the proposed LNA. For the operation frequency range, the proposed LNA presents a low NF and high linearity in comparison with other studies.

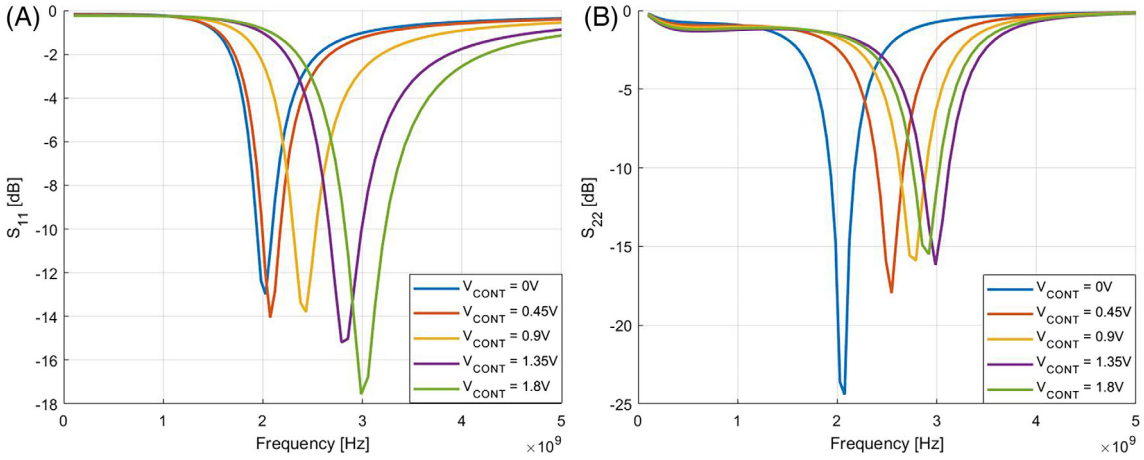

FIGURE 4 (A) S_{11} and (B) S_{22} performance of the proposed low noise amplifier (LNA)

FIGURE 5 *IIP3* simulation of the proposed low noise amplifier (LNA) at 3 GHz

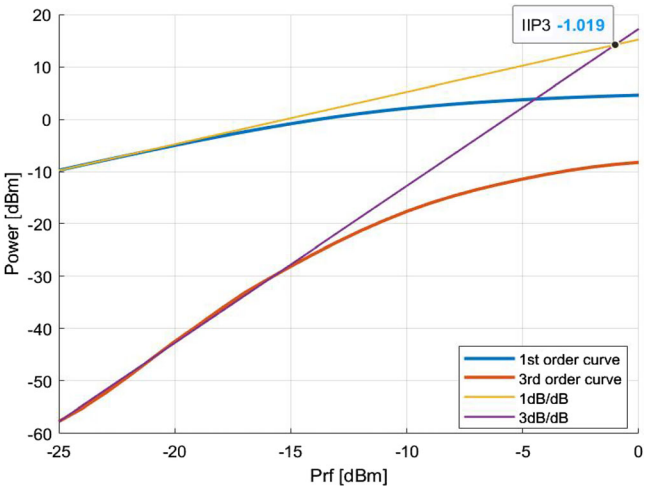

TABLE 3 *IIP3* values at five operation frequencies

Frequency (GHz)	2	2.25	2.5	2.75	3
IIP3 (dBm)	−12.9	−5.23	−4.19	−3.28	−1.019

3 | SURROGATE MODELING

In this section, the variability analysis of the designed tunable LNA is performed using surrogate modeling concepts. First, the fundamentals of surrogate modeling will be given. Then, two case studies are discussed to demonstrate the application of the surrogate modeling in the variability analysis of the tunable LNA.

3.1 | Basics of surrogate modeling

Surrogate modeling is a mathematical approach used to simplify complex input-output relations, which cannot be always expressed explicitly through comprehensive, analytical functions. In order to understand the basics of this approach, the surrogate modeling process is shown step-by-step as a flowchart in Figure 6.

To begin with, a simulator is used to produce the data points in a random fashion, within the design space of interest. The first step in designing the surrogate model is selecting the samples for model training from the data set in a way that the design space is homogeneously covered. There are several different sampling techniques, including Monte Carlo sampling, Latin hypercube sampling, Voronoi Tesselation, and more.[18] Depending on the dimensionality of the data samples, a suitable sampling method should be chosen since the quality of the model relies highly upon the efficient coverage of the design space.[19] After having sampled an initial amount of data, the fitting and modeling methodology should be specified. For this purpose, methods such as artificial neural networks (ANNs), Kriging functions, and

TABLE 4 Performance comparison of the proposed tunable LNA with similar studies

Spec	This Work[a]	Takamatsu et al[2] [b]	Dao et al[3] [b]	El-Nozahi et al[4] [a]	El-Nozahi et al[4] [b]	Chong-Ru and Liang-Hung[5] [a]
Freq (GHz)	2–3	0.47-0.77	0.9, 1.8, 5.2	2.4-5.2	1.9-2.4	2.9-3.5
NF (dB)	2.2-2.9	1.7-3.5	2.3-2.9	2-4.2	3.2-3.7	3 (@3.5GHz)
A_v (dB)	12-15	15.1-19.6	13-16	19-23	10–14	6-12
S_{11} (dB)	< -12	-5.01	< -12	< -13	< -13	< -11
S_{22} (dB)	< -15	< -13.97	-	-	-	< -15
IIP3 (dBm)	-1.019 (@3GHz)	-	-	-3 (@3GHz)	-6.7 (@2GHz)	-
Power (mW)	23	7.5-13.92	7.5	17	17	18
Tech (nm)	180	90	180	130	130	180

[a]Simulated results.
[b]Measured results.

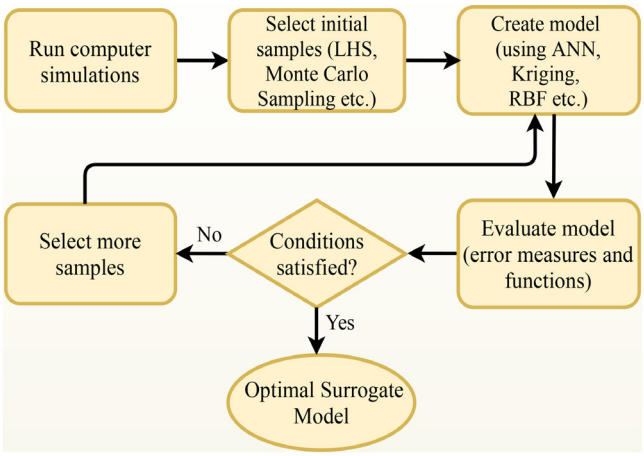

FIGURE 6 Surrogate modeling process flow

radial basis functions can be employed.[20] A surrogate model can be produced in accordance with the working principles of any of these approaches.

In order to evaluate the generated model, both error functions and error measures are used. Error functions (eg, root relative square error [RRSE], maximum relative error [MRE], and average relative error [ARE]) evaluate the error between the estimated and real outputs for all model training samples. Meanwhile, the error measures (eg, cross-validation and holdout) give information on the amount of error that each sample contributes.[7] If the error is higher than the one maximum error projected, more samples should be selected, and the process will iterate, as shown in Figure 6, until the optimal surrogate model has been achieved for which the maximum error projected is not violated.

3.2 | Case study I: modeling the effect of wire bonds in inductance values

Wirebonding is one of the critical steps in integrated circuit (IC) manufacturing, where the pads of the bare die containing the IC are electrically connected to the pins of the package through golden or aluminum wires. The length of the bondwire can vary substantially thereby introducing additional inductance to the IC through the connecting pads. In the context of a tunable LNA, such a contribution could be very detrimental as the excess series inductance can severely alter the performance at the operating frequency. Thus, the impact of the bondwires should be accounted during design time in order to mitigate the possible variability degradations. There have been several studies on how to address the effects of bondwires.[21,22] In this paper, prior modeling of the possible changes in inductance values due to bondwires will be accomplished through surrogate modeling.

As seen in Figure 1, the inductors L_g, L_s, and L_{in} are directly affected by the variability of wire bonds through the bias voltage, ground, and supply voltage connections, respectively. Therefore, the change in the total inductance values can potentially distort the performance of the LNA. For an approximate variability of 20% to 25% in the chosen inductances, LNA performance is simulated for different values of L_g, L_s, and L_{in} that are randomly chosen from the projected variability range. Considering the design fundamentals described in Section 2, the two LNA characteristics that can mostly be affected are the input power matching, S_{11}, and *NF*. Therefore, these two outputs have been modeled in this case study by using the SUMO toolbox in terms of the inductance variability of L_g, L_s, and L_{in}.[23]

After having obtained the data, the inputs (values L_g, L_s, and L_{in}) have been normalized between −1 and 1 and separated into training and test data sets at a ratio of 70:30. Latin hypercube sampling has been chosen to sample the training data, and ANN (300 epochs) is preferred as the model fitting method.[8] The model has been validated via RRSE (4), and a tolerance of 0.01 is assumed. In (4), y_i represents the circuit simulated output value, $_i$ is the surrogate model output, and is the average of all circuit simulation outputs. Meanwhile, as the error measure, cross-validation has been preferred.

$$RRSE = \sqrt{\frac{\sum_{i=1}^{n}(y_i - \tilde{y}_i)^2}{\sum_{i=1}^{n}(y_i - \bar{y})^2}} \tag{4}$$

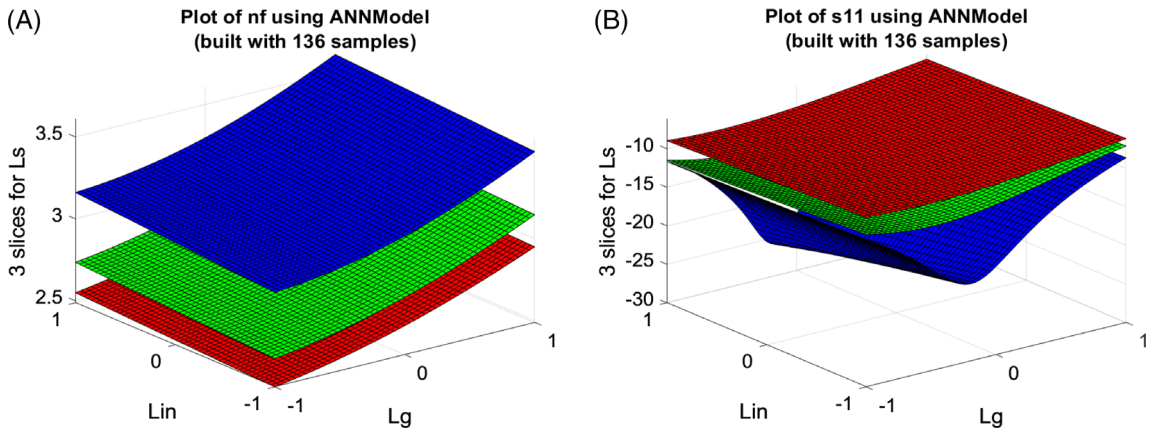

FIGURE 7 (A) Noise figure (NF) and (B) S_{11} surrogate models for the inputs L_g, L_s, and L_{in}

The results of the optimally generated surrogate model have been shown in Figure 7. The relation between L_g and L_{in} for three different values of L_s has been given for both NF and S_{11} outputs, in dB scale. The change in L_s value results in a considerable shift in the LNA performance. For the NF model, a substantially growing change in the noise level is seen when the normalized values of the inductors L_{in} and L_g tend towards one. Another important fact to be mentioned is the trade-off that appears in the simultaneous design of both outputs. The best performance for the NF is achieved for the lowest value of L_s (bottom slice), while for the same value, S_{11} appears to have the lowest performance (top slice). These results should be taken into account during the LNA design.

In Tables 5 and 6, RRSE and MRE error function values of the constructed surrogate models are shown in absolute values for both the training and test data sets. The definition of MRE is given in (5). All the values are within the tolerance yet, including the error in the test data set, which is the most critical measure, since it proves the validity of the model for the data set not used during training.

$$MRE = max\left|\frac{y_i - \tilde{y}_i}{y_i}\right| \tag{5}$$

3.3 | Case study II: comprehensive variability analysis of the LNA voltage gain

As deduced by the results of the first case study, modeling of NF and S_{11} with only three input parameters resulted in a successful surrogate model using only 136 samples. Hence, the aim of the second case study is to increase the complexity of the model by providing a total of six normalized input parameters. As one of the most important specifications in an LNA, the voltage gain of the circuit is related to many design parameters. Thus, the variability of these parameters can significantly decrease the voltage gain. In order to demonstrate this fact, L_g, L_s, and L_d, as well as their quality factors, have been swept in LNA performance metrics simulations to get a voltage gain output for a total amount of 2000 data points at two corner operating frequencies of the tunable LNA. The procedure of the design has been done in the same way as in case study I, yet this time with an RRSE error tolerance of 0.001.

As shown in Table 4, the model has been well trained, and the RRSE of the test data set is around the required error tolerance. Only the MSE of the test data for the 2-GHz case seems to be higher than expected. This might be due to the fact that the problem has been modeled to converge for the RRSE function requirement. The complexity of the model has also been proved by the increased complexity in the neuron number and layers when compared with the previous case. Moreover, the number of samples used to train the models has been significantly higher. Specifically, 308 samples have been used to build the voltage gain model at 2 GHz and 465 samples to build the model at 3 GHz.

In order to be able to interpret the results of the six-dimensional model, separate graphs have been plotted in Figure 8. These specific plots have been chosen to demonstrate the importance of the quality factor (Q) in the RF inductor design. The unnormalized value for the lowest inductance shown in the graphs is 2, while the middle is 10, and the highest is 18.

It is important to note that the voltage gains for the lowest Q values would not be sufficient to satisfy the aimed LNA design specifications. Moderate Q values, however, result approximately in voltage gains on par with the outputs reported in the LNA design section. In order to get a bigger improvement in those results, a quality factor of 18 should be chosen for which the voltage gain rises to almost 16 dB at 3 GHz. Finally, as expected, better performance results have been obtained at 3 GHz, in all situations considered.

The developed models can be employed to improve the LNA design performance. This approach could be viewed as a "closed-loop" type of usage, as the outputs of the models become the input of the next iteration in a multistage optimization problem. Without surrogate modeling, such a process would be very time-consuming and complicated as several

TABLE 5 Case study I: surrogate model accuracy information

	RRSE		MRE	
	Training	Test	Training	Test
NF (@ 2 GHz)	0.0011	0.0014	2.68E-04	3.2E-04
S_{11} (@ 2 GHz)	6.807E-04	0.0018	0.0011	0.0023

Abbreviations: MRE, maximum relative error; RRSE, root relative square error.

TABLE 6 Case study II: surrogate model accuracy information

	RRSE		MRE	
	Training	Test	Training	Test
A_v (@ 2 GHz)	4.37E-04	0.001	0.0083	0.025
A_v (@ 3 GHz)	3.59E-04	0.0013	7.08E-04	0.0024

Abbreviations: MRE, maximum relative error; RRSE, root relative square error.

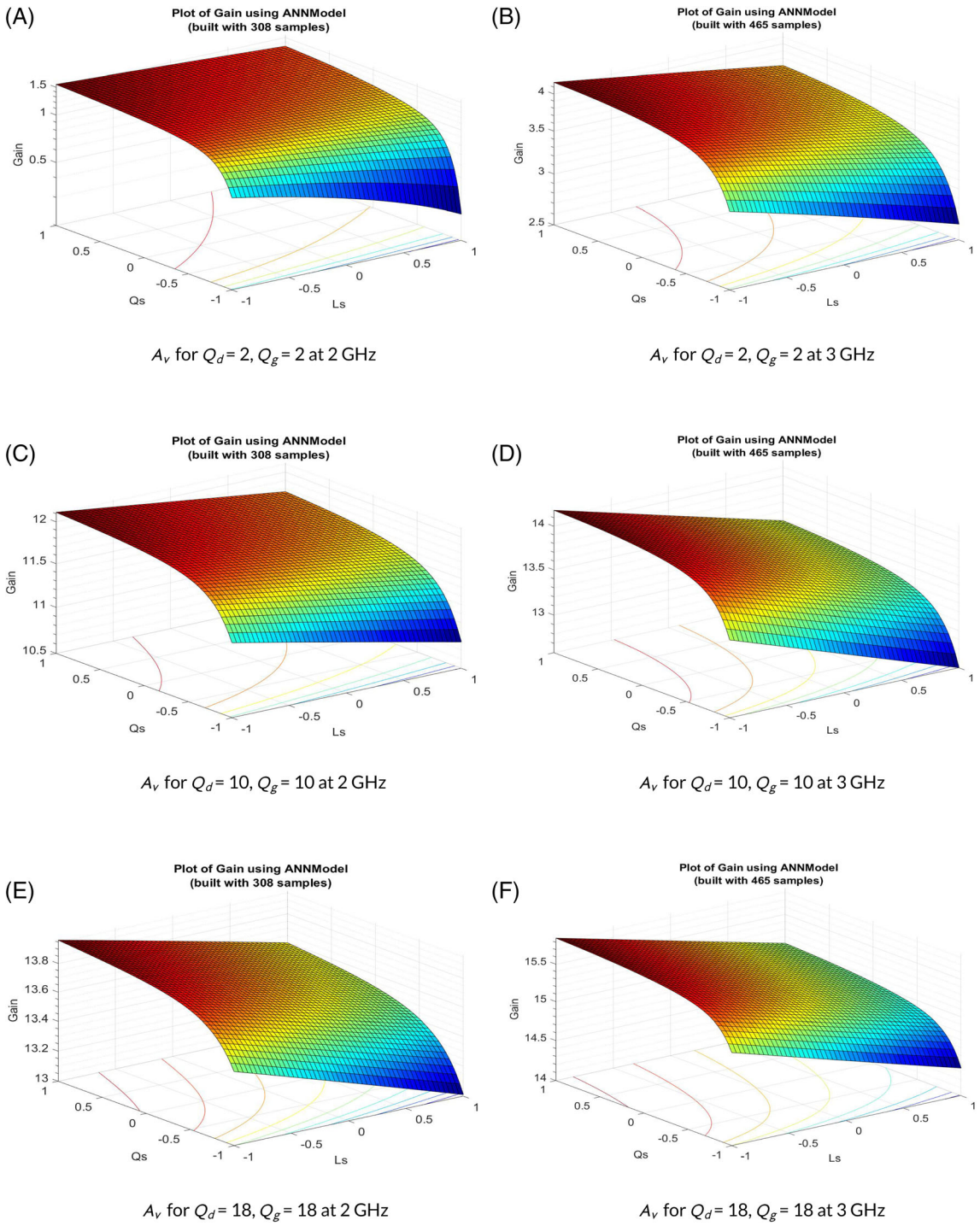

FIGURE 8 A_v surrogate modeling results for six input parameters

design parameters should be jointly changed. Nevertheless, the models described in this paper enable the designers to check several different combinations of multiple parameters, observe the outcome, and then revise the design such that the overall performance is enhanced.

4 | CONCLUSION

In this paper, a 2- to 3-GHz tunable LNA has been designed using A-MOS varactors in both input and output matching circuits. This circuit block can be used in communication systems and internet-of-things applications that employ the S frequency band based on its continuous tunability. Moreover, an analysis on the impact of bondwires via two surrogate models on NF and S_{11} has been conducted. In a second case study on the variability of the tunable LNA voltage gain, a six-dimensional model with higher complexity has been successfully trained and tested at two different frequencies. The contribution of surrogate modeling in facilitating the optimal design of a tunable LNA has been investigated and verified.

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