```vhdl
1    library IEEE;
2    use IEEE.std_logic_1164.all;
3    use IEEE.numeric_std.all;
4
5    entity dwl is
6        port(
7                AGTB            : in std_logic; -- input (A>B) as obtained from the 4-bit comparator
8                AEQB            : in std_logic; -- input (A=B) as obtained from the 4-bit comparator
9                ALTB            : in std_logic; -- input (A<B) as obtained from the 4-bit comparator
10               door            : in std_logic; -- input from pb(0)
11               window          : in std_logic; -- input from pb(1)
12               leds_out        : out std_logic_vector(5 downto 0) -- output for the leds
13
14       );
15   end entity dwl;
16
17   architecture logic_dwl of dwl is
18
19   begin
20
21       leds_out(2) <= AGTB AND window AND door; -- If it's ABOVE temp and the window and door
     are closed, the A/C should turn ON
22       leds_out(1) <= AEQB;                     -- If the current and desired temp are equal,
     then system is AT temp
23       leds_out(0) <= ALTB AND window AND door; -- If it's BELOW temp and the window and door
     are closed, the Furnace should turn ON
24       leds_out(3) <= (AGTB OR ALTB) AND window AND door; -- If A/C or Furnace is ON and the
     door and window are closed
25       leds_out(4) <= NOT(door); -- when pb(0) is pressed, that means the door is open
26       leds_out(5) <= NOT(window); -- when pb(1) is pressed, that means the window is open
27
28   end logic_dwl;
```