```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4
5   entity concatenate_sum_mux is
6   port(
7      inp1        : in std_logic_vector(7 downto 0);   -- concatenate input
8      inp2        : in std_logic_vector(7 downto 0);   -- sum input
9      mux_select  : in std_logic;                      -- pb(3) as selector
10     output      : out std_logic_vector(7 downto 0)   -- 8 bit output
11  );
12
13  end entity concatenate_sum_mux;
14
15  architecture mux_logic of concatenate_sum_mux is
16
17  begin
18
19  -- for multiplexing the concatenate and sum of hex_A and hex_B
20
21  with mux_select select
22
23  output <= inp1 when '1',  -- concatenate input should be outputted when pb(3) is 0 but we
    are inverting here
24            inp2 when '0';  -- sum input should be outputted when pb(3) is 1 but we are
    inverting here
25
26  end mux_logic;
```