```
 1
 2   library ieee;
 3   use ieee.std_logic_1164.all;
 4
 5   entity Compx1 is
 6   port (
 7         A         : in std_logic; -- 1 bit input from A
 8         B         : in std_logic; -- 1 bit input from B
 9         GT        : out std_logic; -- output for greater than (A>B)
10         EQ        : out std_logic; -- output for equal to (A=B)
11         LT        : out std_logic -- output for less than (A<B)
12   );
13
14   end entity Compx1;
15
16   architecture comp_logic of Compx1 is
17
18   begin
19
20      GT <= A AND NOT(B); -- logic for getting the value of GT(A>B)
21      EQ <= A XNOR B; -- logic for getting the value of EQ(A=B)
22      LT <= NOT(A) AND B; -- logic for getting the value of LT(A<B)
23
24
25   end comp_logic;
26
```