# INTEL UNNATI INDUSTRIAL TRAINING - SUMMER 2023

Problem Statement: Design and Implementation of Automated Teller Machine (FSM) Controller

College Name: PARUL UNIVERSITY

**Team Name: Tech Girls**
Team Member 1:
Name: Ayushi Jignesh Desai
Email: 200305105099@paruluniversity.ac.in
Mobile No.: 9409188369

Team Member 2:
Name: Siddhi AjitSingh Chaudhary
Email: 200305105089@paruluniversity.ac.in
Mobile No.: 7046486407

Mentor:
Name: Monika Nayak
Email: monika.nayak20808@paruluniversity.ac.in
Mobile No.: 9913908664

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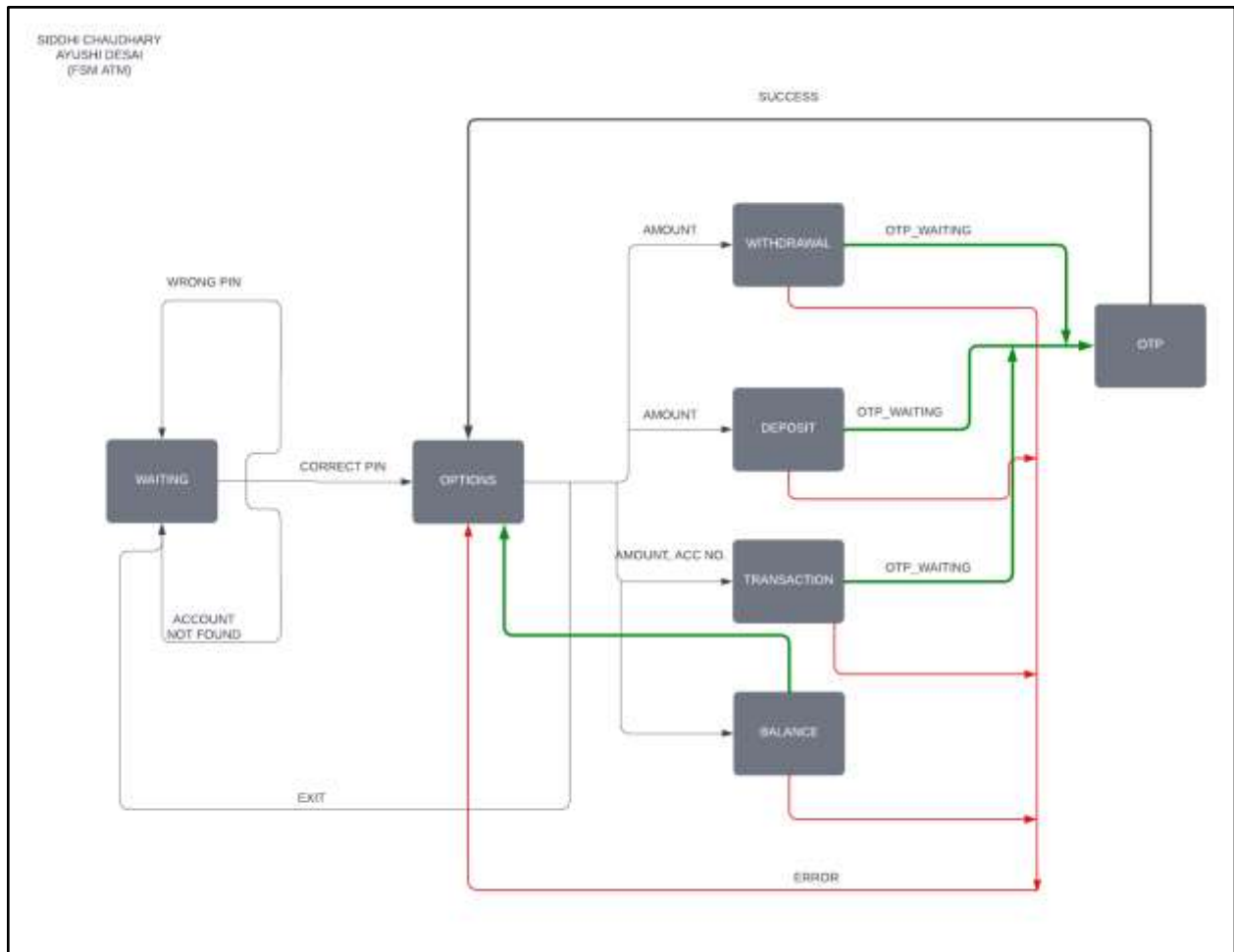
# LIST OF FIGURES

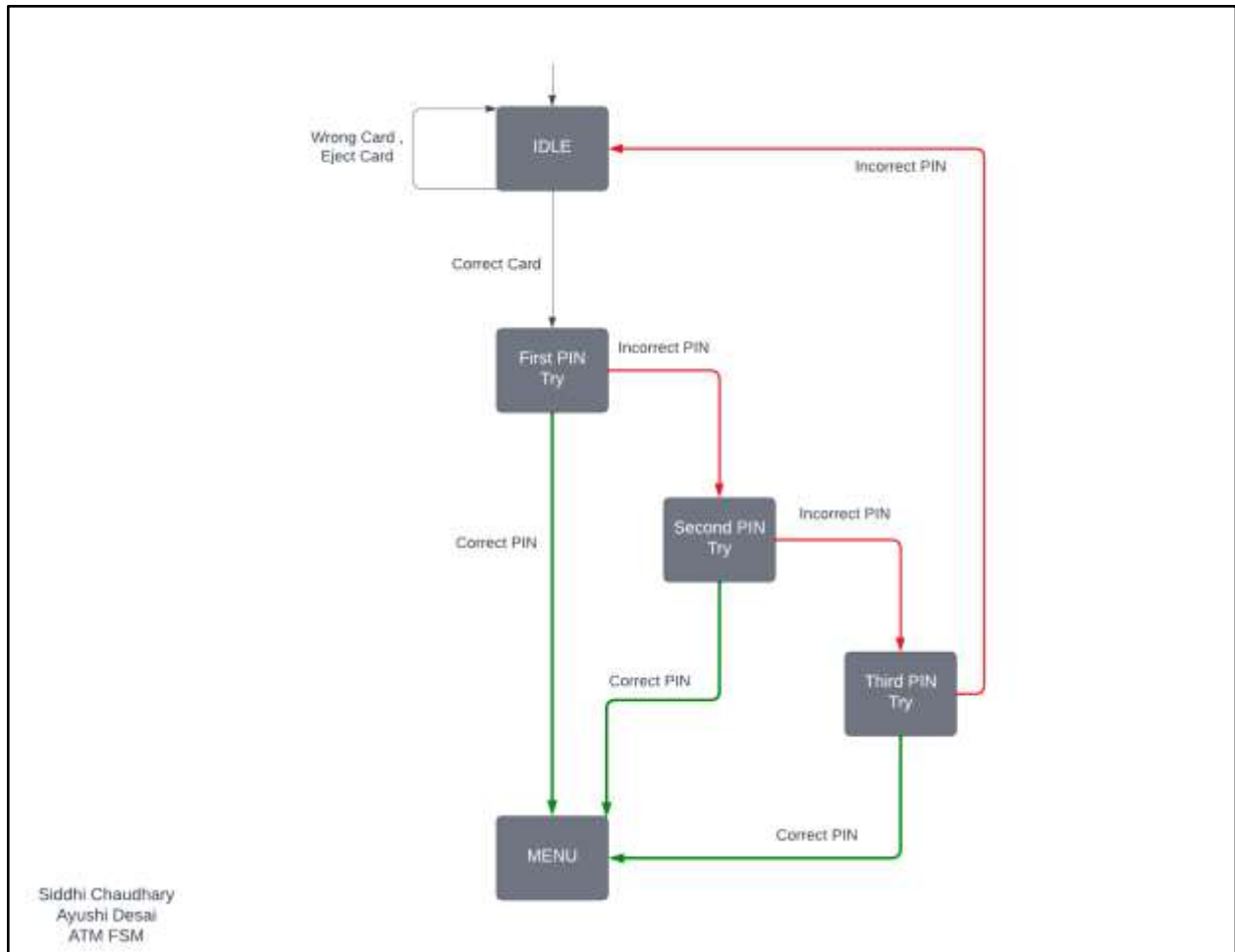# 1. BLOCK DIAGRAM



Fig. 1.1 Block Diagram

Fig. 1.2 PIN Try Block Diagram

# 3. APPROACH TO SOLVE THE PROBLEM

Our problem statement is: Design and Implementation of Automated Teller Machine (FSM) Controller in which we had to design a virtual Automated Teller Machine(ATM) based on two FSM(Finite State Machine): Mealy State Machine or Moore State Machine.

## WEEK 1:
For the implementation of the problem statement we started with Block Diagram and its specification based on which our ATM would be created. And for the solution of our problem statement we have used the Mealy State Machine (FSM).
While developing the Block Diagram the specifications and the correct flow for the project was challenging through the First week.

## WEEK 2:
For the second week of our training period we have started with the Verilog coding for our given FSM with the help of the Block Diagram. After we are finished with the Verilog coding with successful compilation of Analysis and Elaboration (No error) then we started to work on the Test Bench for our Verilog code to verify its functionalities.
Developing the Verilog code was the most difficult part of this project as it was very new to us for coding in Intel Quartus with the Verilog Language initially and it took us much more time than expected but we were able to come through it.

## WEEK 3:
Successfully developed the Test Bench, integrated it with the Verilog code and Verification of the Specification for the given FSM. After the completion of the Verilog code and its Test Bench we started with the RTL Simulation and prosperously got the Waveform for our ATM and the RTL Viewer for the same.
Designing the Test Bench with effective and accurate test cases was a task to be done.

## WEEK 4:
Developed the Pin Planner with our required pin for the project then successfully passed through the fitter and developed the Chip Planner. After developing the Chip planner we started with the Power Analyzer Tool and got the results.
Assigning the accurate pins with the pin planner took some time to work properly.

**WEEK 5:**

Started analyzing the code coverage, the area and power, the timing and proper timing constraints reports. Implemented the given design on the targeted FPGA. Developing the project report and uploading the pieces of the project on the Github repository. Finished with the Video Demo.

# 4. COMPLETE FLOW OF SOLUTION

We started to solve our problems by coding the given statement. We considered the given criteria before beginning the coding portion. We coded an ATM using the FSM (mealy) we created. Our main concerns for the code other than the standard ATM was to exit if the pin was entered wrong 3 times and also if the amount entered to deposit or withdraw was greater than 10,000 then the code will switch to using OTP for more security.

To begin, we coded the basic ATM with states of Withdrawal, Deposit and Withdrawal with showing of balance. We first declared the basic states and params which were globally used throughout the code, and moreover created databases for Accounts and Pins consisting of account numbers and pins to corresponding account numbers. We added different inputs and output registers and wires to store the results and clock. And, further in coding we added OTP and Exiting of code if the pin was entered wrong three times. For OTP we added extra states to the existing ones and a condition if the amount entered was greater than 10,000 then the OTP state will be activated. And, for pin we took approach of for loop with condition if wrong pin was entered 3 times the code will move back to menu option.

Once the code was done, we started to code the test bench for the code with various cases which the code should successfully pass through. Some of the test cases were if the pin entered was wrong, withdrawing too much money, showing the balance etc. After successfully coding the test bench we performed a compiling of design which consisted of various steps. Afterwards, we moved on to the different steps of the process of solving the problem statement.

Firstly, we configured RTL simulation where we got a graph as output of the performance with various states on the y-axis. Then, we performed different netlist viewers (technology map viewer (post-mapping), RTL viewer, technology map viewer (post-fitting)). We faced difficulty in performing a state machine viewer. Proceeding, we assigned different pins in the pin planner to the outputs and inputs. On the basis of it a chip planner was formed. After performing the power analyzer tool, we got the temperature at 0 C for lower end and 85 C for higher end, also, 25 virtual pins were calculated.
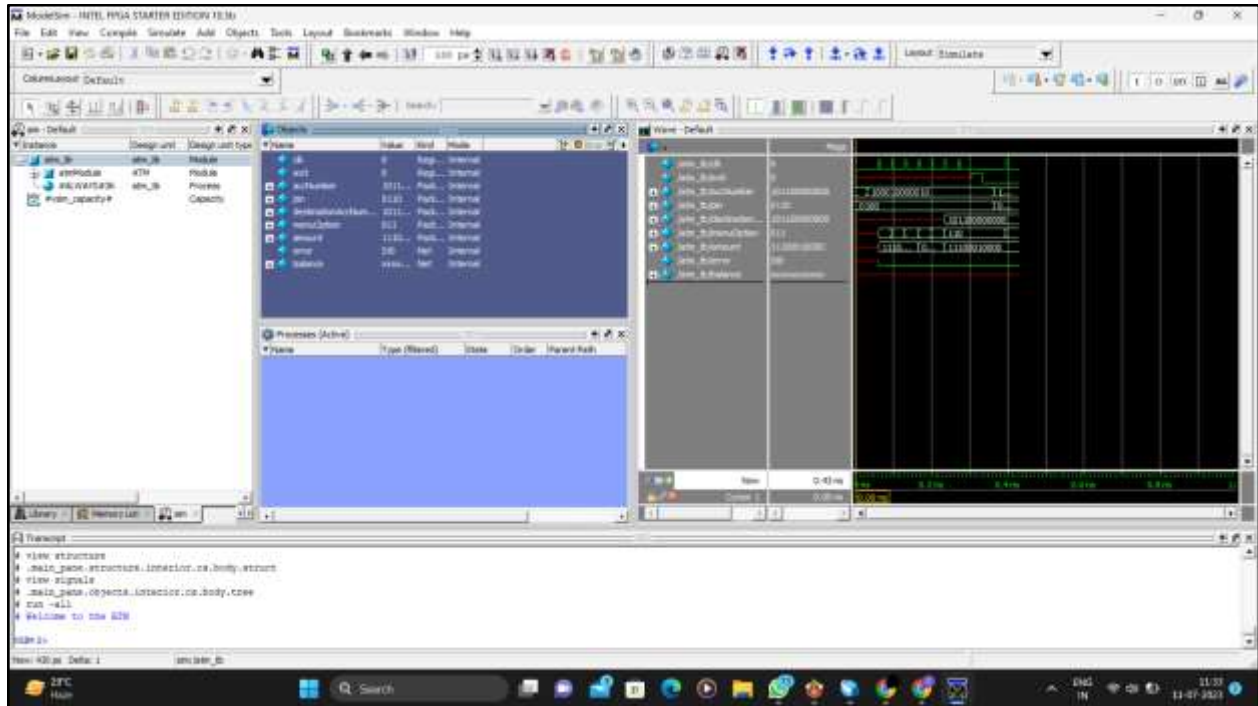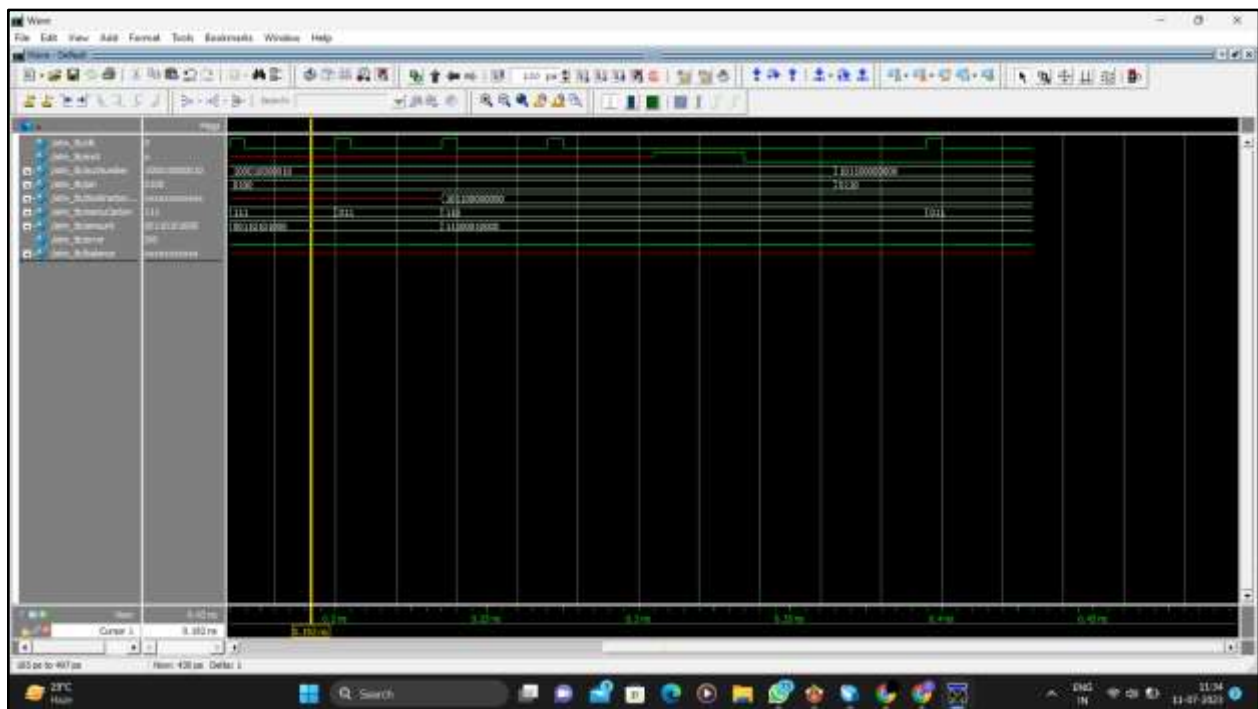
# 5. NECESSARY FILES
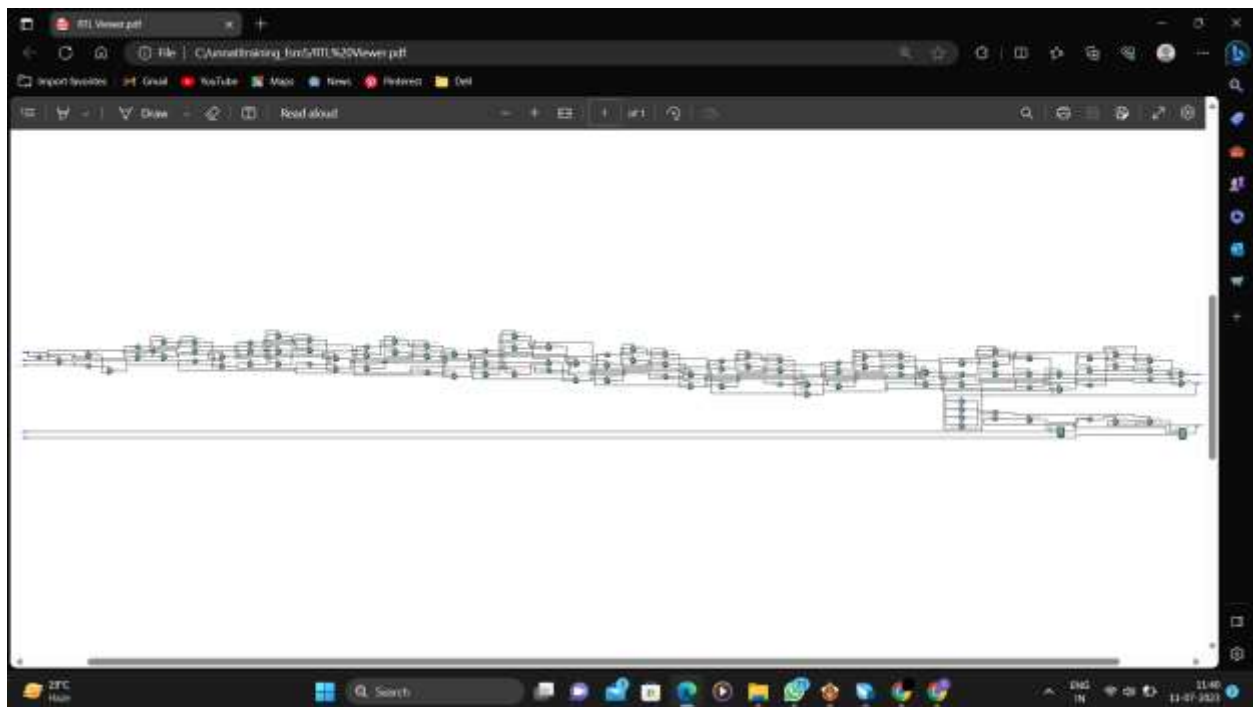


Fig. 5.1 RTL Simulation


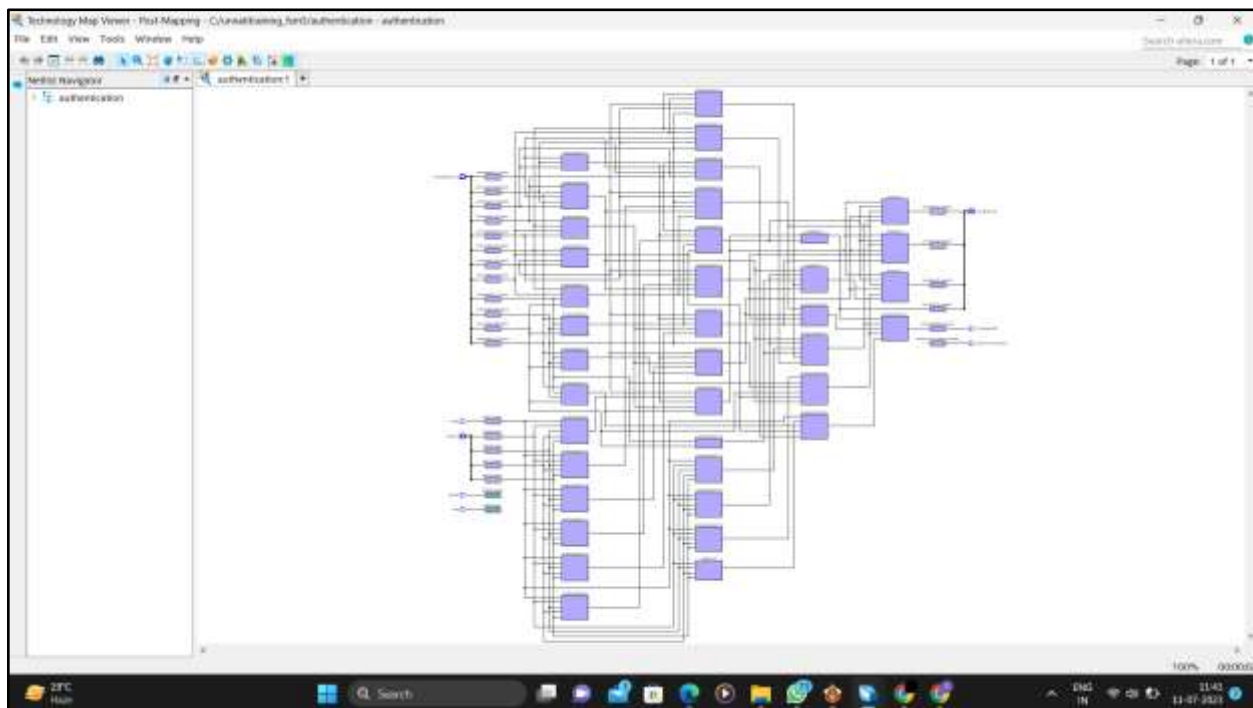
Fig. 5.2 WaveForm

Fig. 5.3 RTL Viewer
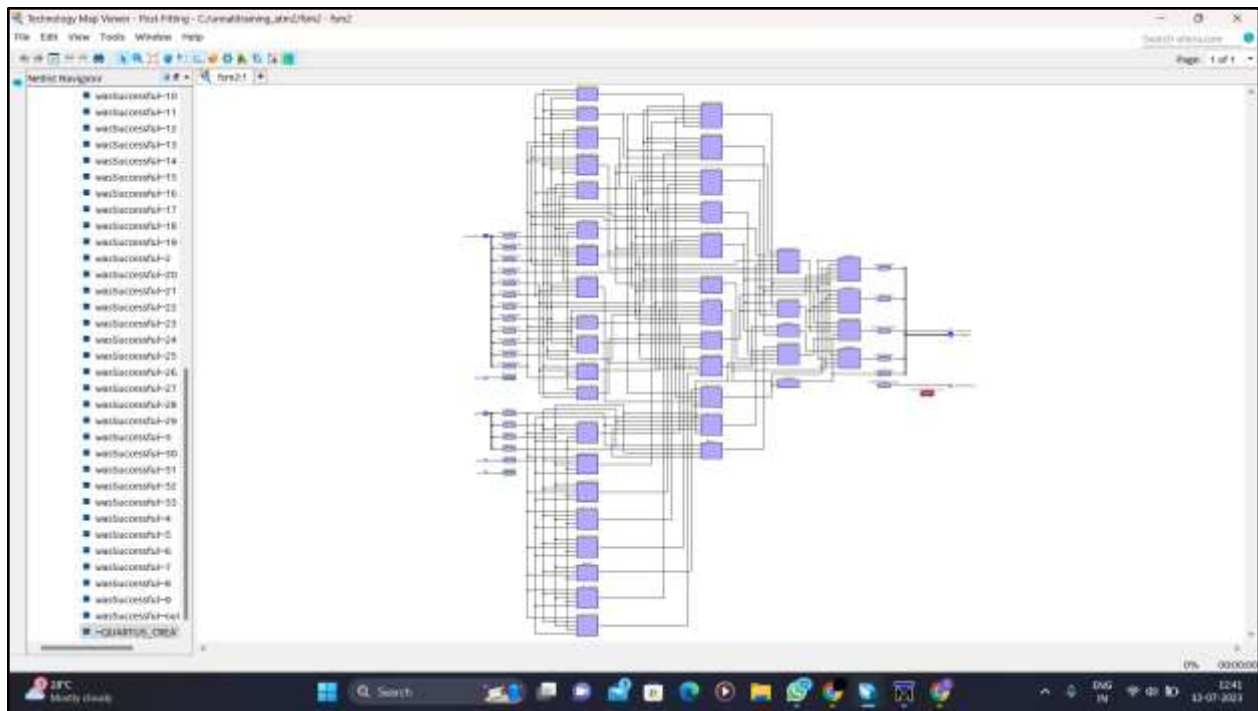
Fig. 5.4 Technology Map Viewer (Post Mapping)

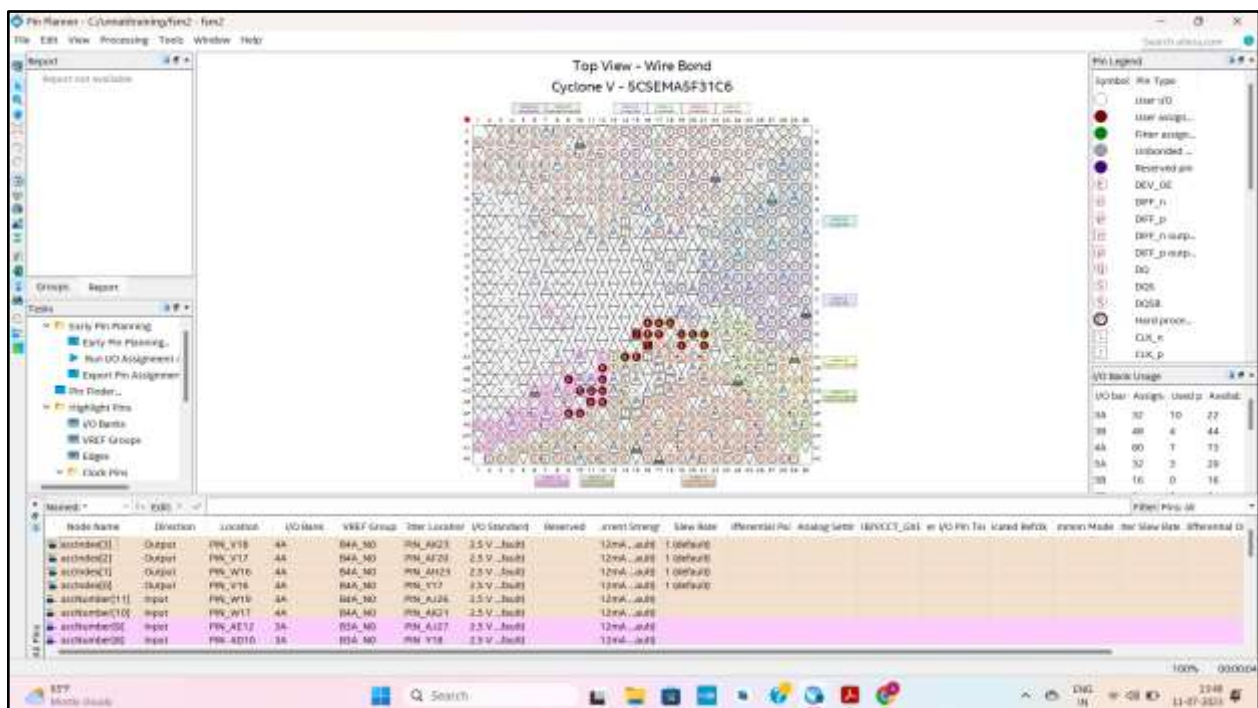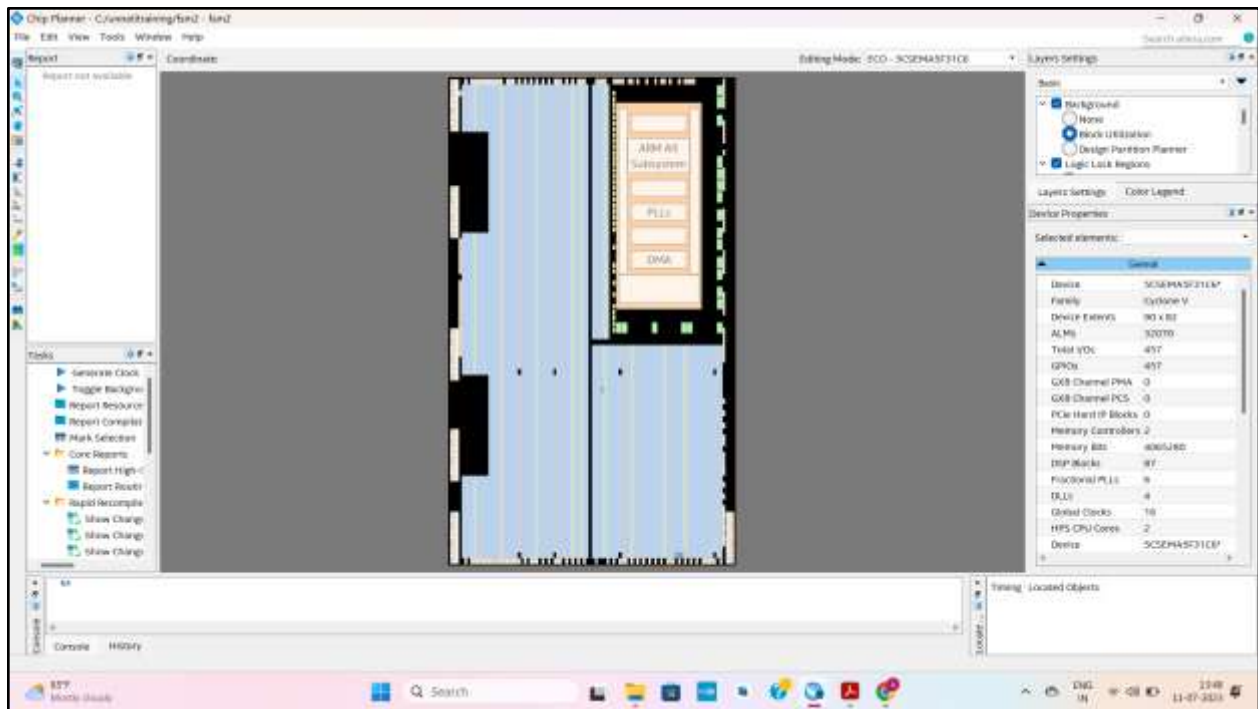Fig. 5.5 Technology Map Viewer (Post Fitting)
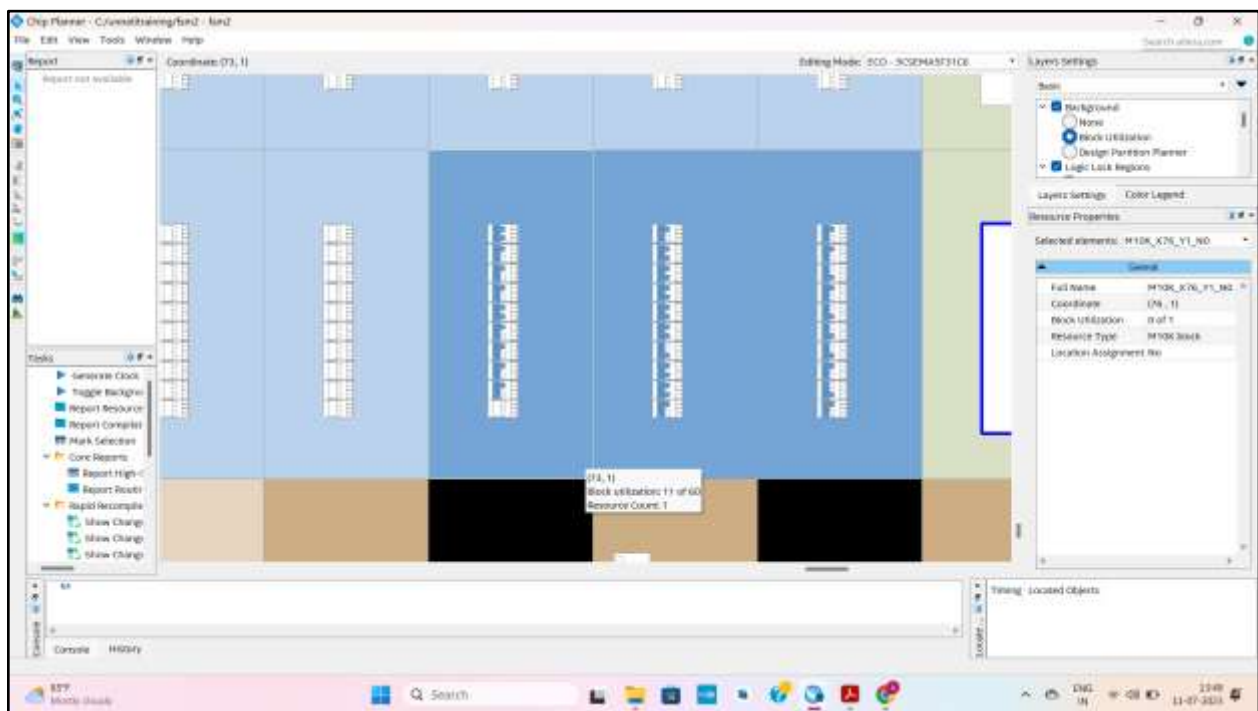


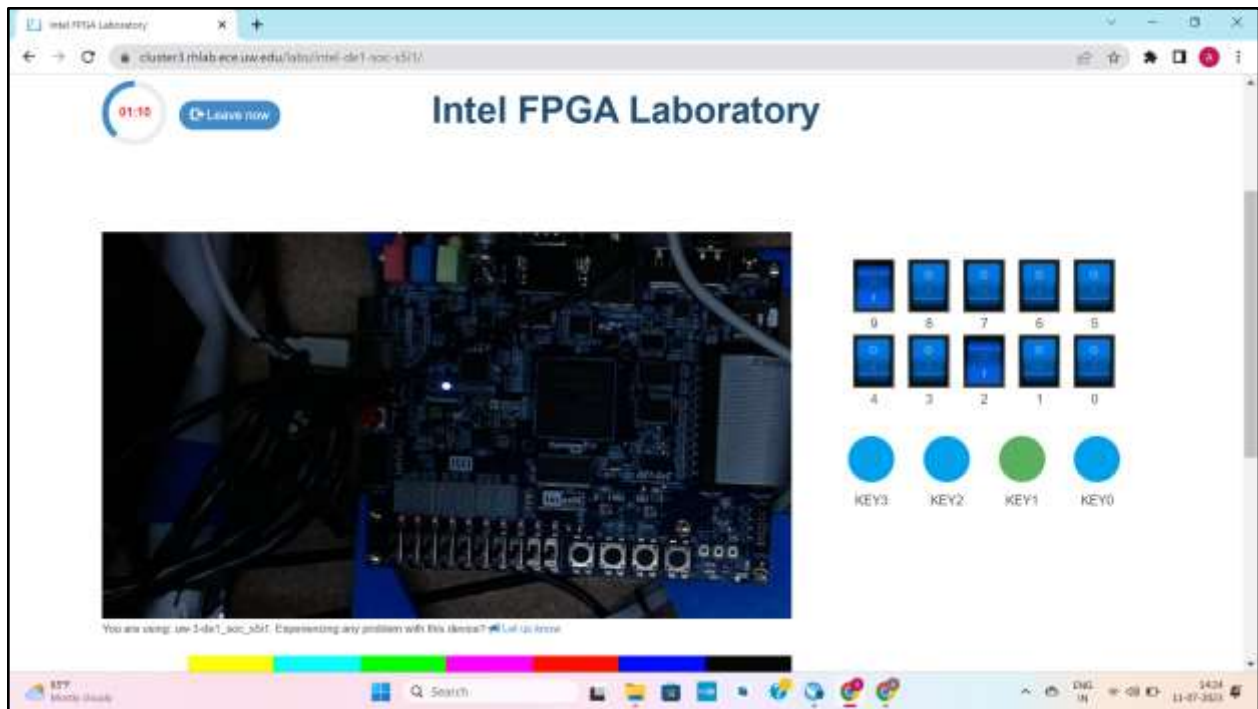Fig. 5.6 Pin Planner

Fig. 5.7 Chip Planner
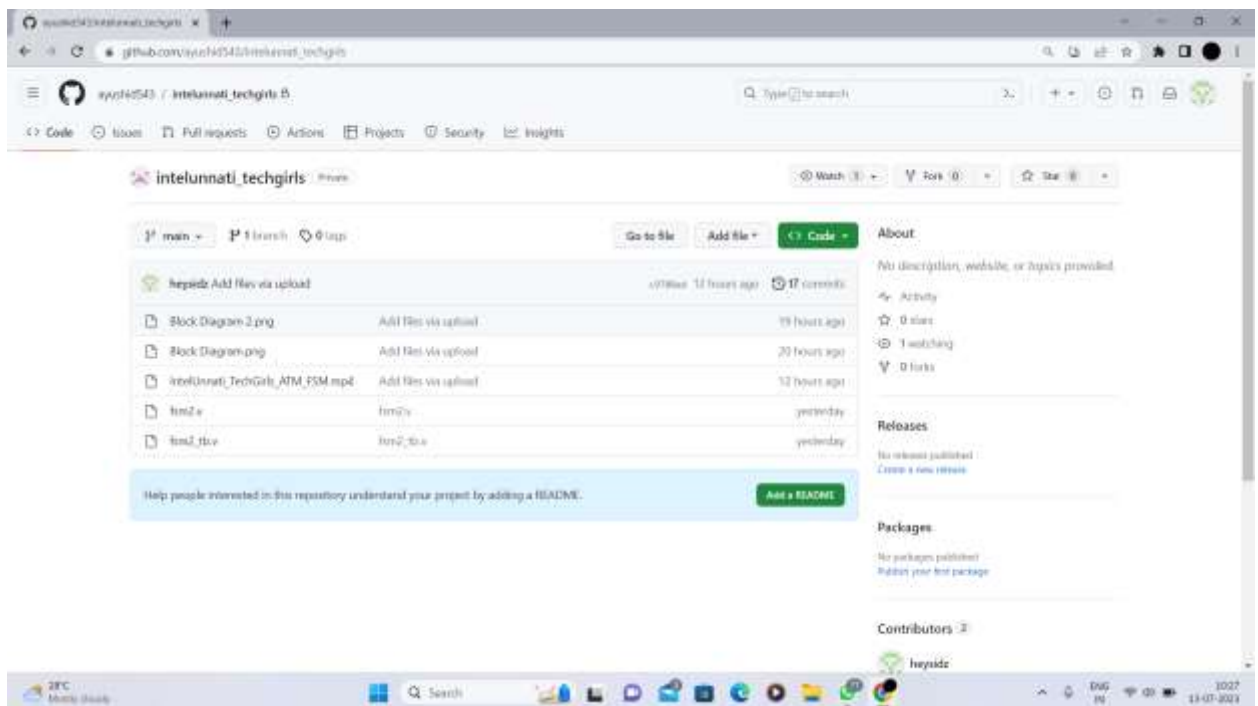


Fig. 5.7(a) Chip Planner

Fig. 5.8 Labsland


Fig. 5.9 GitHub Repository

# 6. VIDEO DEMONSTRATION

https://github.com/ayushid543/intelunnati_techgirls/blob/main/IntelUnnati_TechGirls_ATM_FSM.mp4

# 7. RESULTS

According to our problem statement: Design and Implementation of Automated Teller Machine (FSM) Controller we have designed a Automated Teller Machine (FSM) Controller using Intel Quartus with Verilog coding language. Specification for this ATM (FSM) Controller are the options for Withdrawal, Deposit, View Balance and View Balance after Withdrawal or Deposition. For the PIN entry we kept 3 trials in case of incorrect PIN insertion and after 3 attempts the account will be locked. In case of withdrawal of more than Rs 10,000 then there is an OTP sent to the user's registered mobile number for authentication along with the PIN entry. And same goes in case of Deposition.

# 8. SUMMARY

We have completed the given problem statement to the best of our abilities from making ourselves familiar with the topic to executing our ideas. We started with making a block diagram and continuing to code and then test our written code and analyzing it. The project at hand has encountered several challenges throughout its execution. These challenges have presented themselves in various forms, posing obstacles and requiring adaptive strategies to overcome them. Some of them are us being complete novices at working with this technology and others just a part of the process. Despite these constraints we have successfully designed an ATM using FSM with functionalities like OTP and exiting the code after three unsuccessful attempts at entering the pin. We have learnt immensely from this project and are grateful for the opportunity that was provided (and will continue to work and make it optimal code).