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Digital Electronics

Term-Test 2

Solutions:

1) i) Practically, we don't get toggling in sequential circuits. Since clock pulse is more than the propogation delay, so within one clock pulse the output will keep on toggling again and again and it may became ~~inter~~ indeterminate. This is known as race-around condition.

2) Race around condition occurs because of the feedback connection.

3) Race around condition occurs only in level-triggered flip flop.

4) RAC is when J = 1 and K = 1 [flip flop in toggling mode]

5) We can overcome this problem by making the clock = 1 for very less duration.

6) The circuit used to overcome race around conditions is called master slave JK flip flop.

7) Race-around condition can be eliminated using master-slave flip-flop.

8) Master-slave flip-flop is the cascaded combination of two flip-flops among which the first is designated as master flip-flop while the next is called slave flip-flop.

→ 2) The excitation table for S-R flip flop to D flip-flop convergion is given by:

Input	Present State	Next State	Flip-flop Inputs			
			S	R	S	R
	Q_n	Q_{n+1}				
0	0	0	0	0	0	X
			0	1		
0	1	0	0	1	0	1
1	0	1	1	0	1	0
1	1	1	0	0	X	0
			1	0		

The excitation table is simplified using K-map.

K-map for S

Q_n \ D	0	1
0	0	1
1	0	X

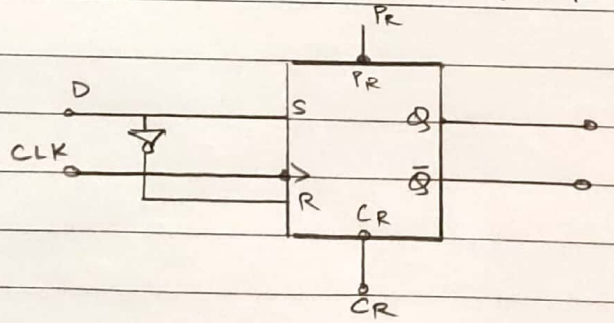
$S = 0$

K-map for R

Q_n \ D	0	1
0	X	0
1	1	0

$R = \bar{D}$

The logic diagram of D flip-flop using S-R flip flop.



→ 3) $f(A,B,C,D,E) = \Sigma m(2,4,5,7,10,16,15,16,17,25,26,30,31)$

Inputs	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
$\bar{A}$	0	1	(2)	3	(4)	(5)	6	(7)	8	9	(10)	11	12	13	(14)	(15)
A	(16)	(17)	18	19	20	21	22	23	24	(25)	26	27	28	29	(30)	(31)
For MUX	A	A	$\bar{A}$	0	$\bar{A}$	$\bar{A}$	0	$\bar{A}$	0	A	$\bar{A}$	0	0	0	1	1