Digital Electronics

Experiment – 4

Name: Ayush Jain

SAP ID: 60004200132

Div: B1 **Branch:** Computer Engineering

DE Expt 04

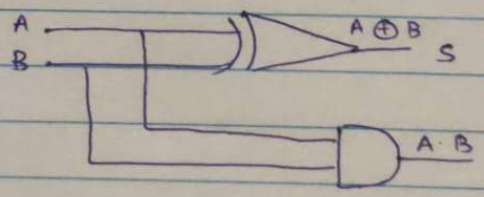
Aim: To verify the truth table of half adder and full adder by using XOR and AND gate for halfadder and XOR, AND and OR gate for full adder.

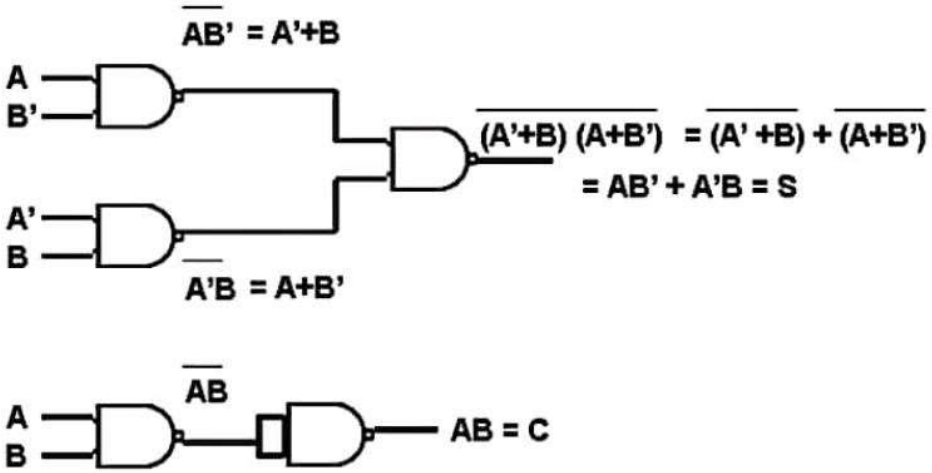
Theory:

Half Adder: Half adder is a combinational circuit that performs simple addition of two binary numbers. If we assume A and B as the two bits whose addition is to performed, a truth table for half adder with A, B as inputs and sum, carry as outputs can be tabulated. The sum output of the binary addition is similar to that of an X-or operation while carry output is similar to that of an AND operation.

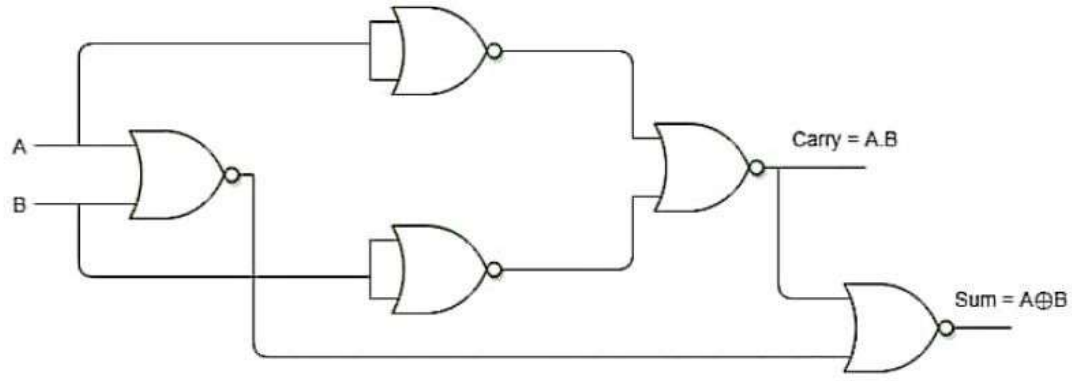
TRUTH TABLE			
INPUT		OUTPUT	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Adder Logic diagram



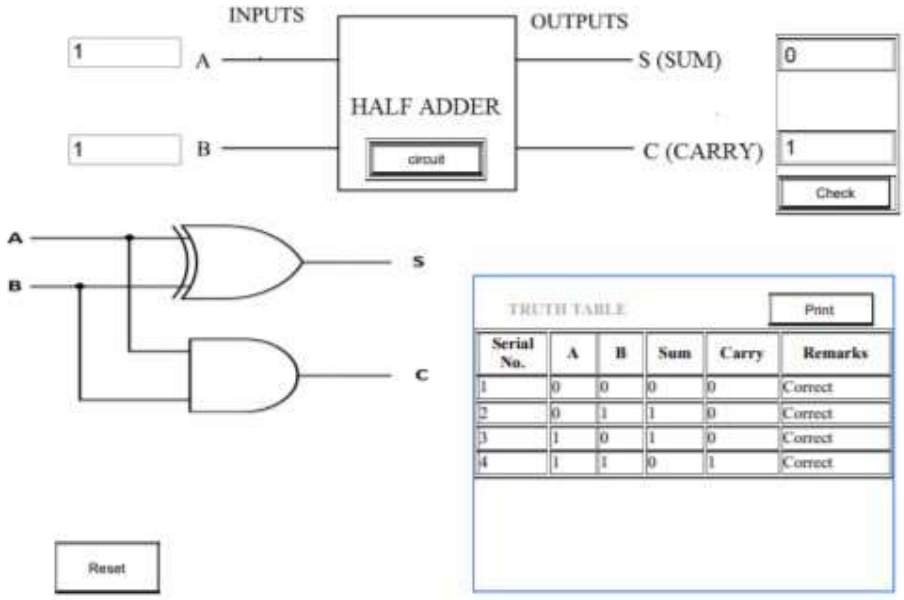


Realization of half adder using NAND gates



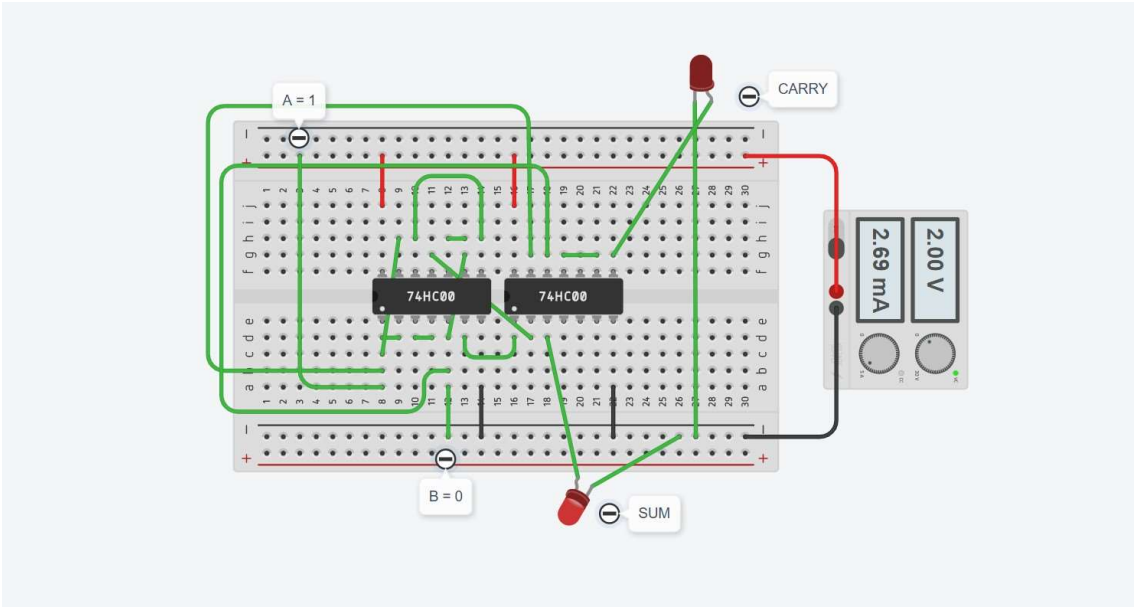
Realization of half adder using NOR Gates

Verification of truth table for HALF ADDER



Serial No.	A	B	Sum	Carry	Remarks
1	0	0	0	0	Correct
2	0	1	1	0	Correct
3	1	0	1	0	Correct
4	1	1	0	1	Correct

Tinkercad:

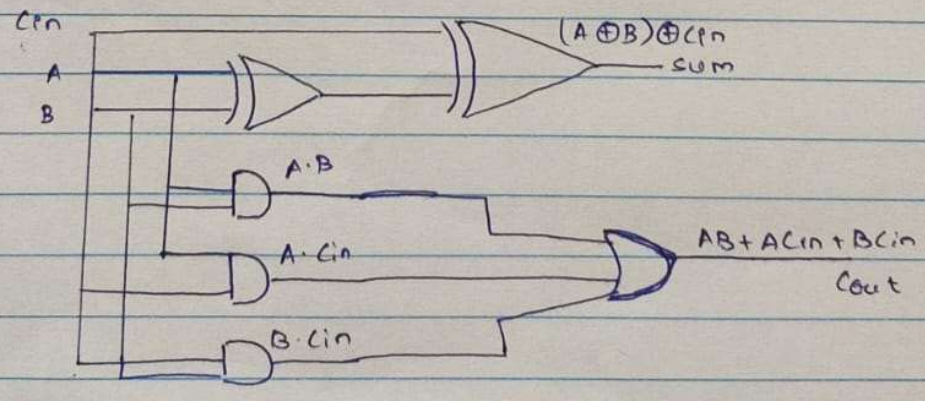


Half adder using NAND gate with inputs 1 and 0

Full adder: Full adder is a digital circuit used to calculate the sum of the binary bits which is the main difference between half and full adder. A, B, Cin are the three inputs bits and Cout is the output. Cin is carry from half adder and Cout is output carry. Sum is implemented using 2 X-OR gates ((A⊕B)⊕Cin) and Cout is AB + A Cin + BCin

TRUTH TABLE				
INPUT			OUTPUT	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full adder logic diagram



Full adder

K-MAP (C = Cin)

Sum

A \ BC	00	01	11	10
0	0	(1)	0	(1)
1	(1)	0	(1)	0

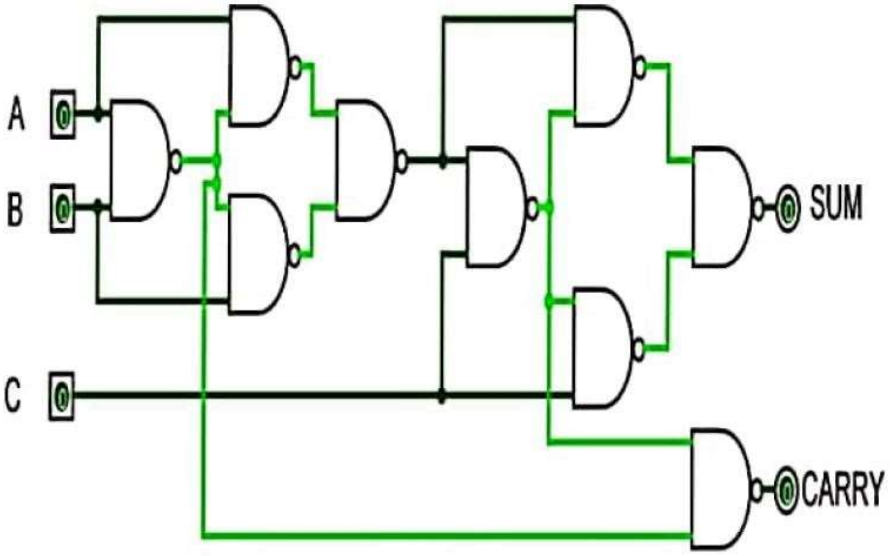
$\therefore$ Sum $= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= (A \oplus B) \oplus C$

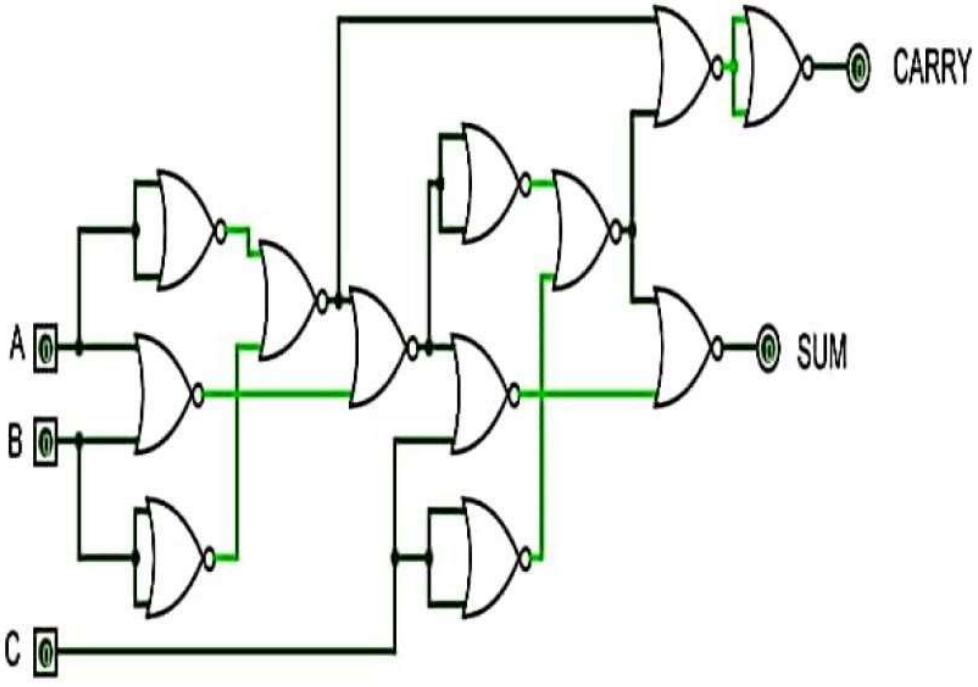
Carry

A \ BC	00	01	11	10
0	0	0	(1)	0
1	0	(1)	(1)	(1)

$\therefore$ Carry $= AB + BC + AC$

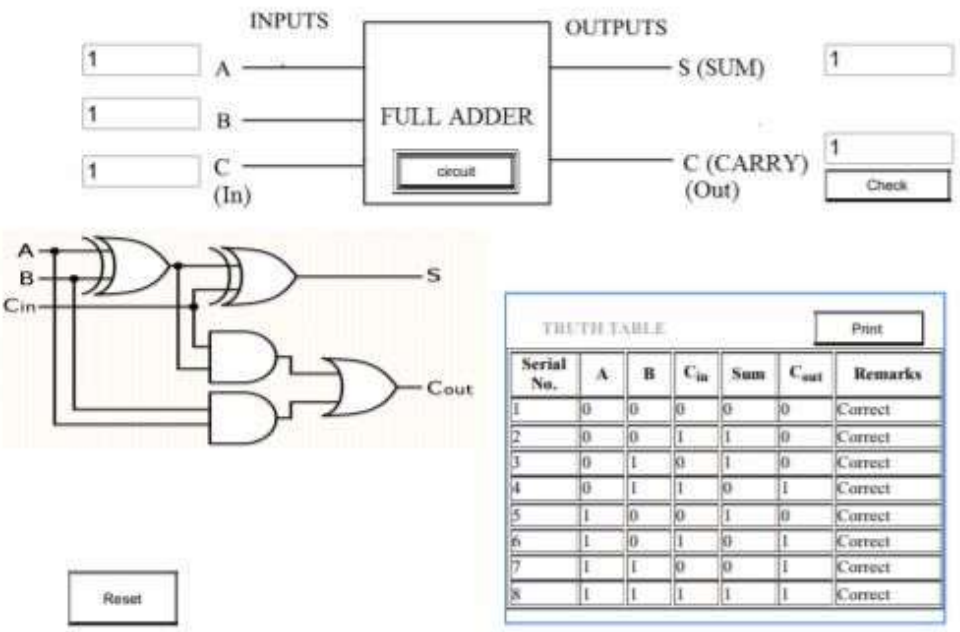


Full Adder using NAND gates



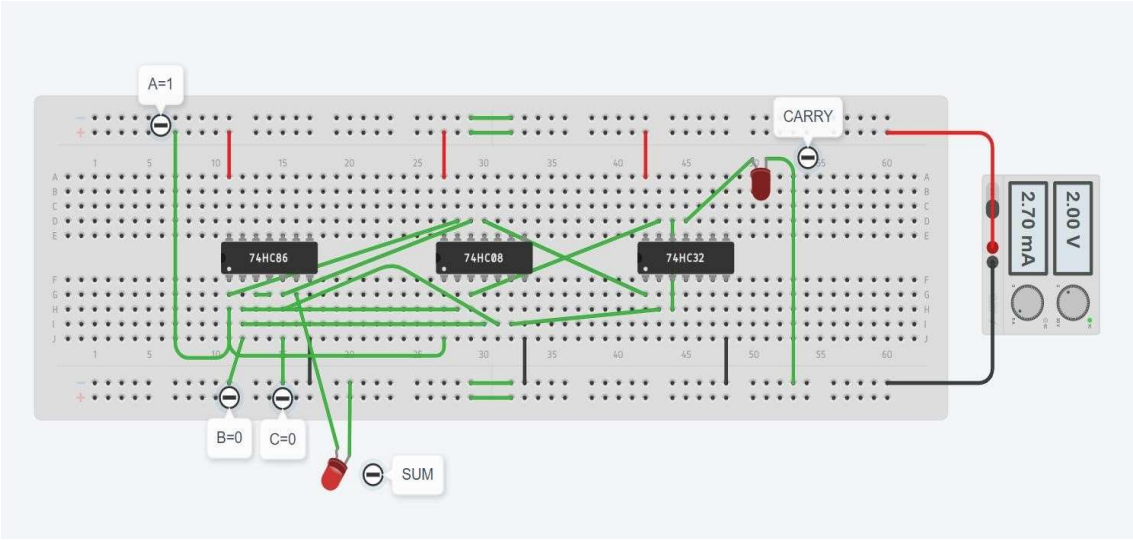
Full Adder using NOR gates

Verification of truth table for FULL ADDER



Serial No.	A	B	C_{in}	Sum	C_{out}	Remarks
1	0	0	0	0	0	Correct
2	0	0	1	1	0	Correct
3	0	1	0	1	0	Correct
4	0	1	1	0	1	Correct
5	1	0	0	1	0	Correct
6	1	0	1	0	1	Correct
7	1	1	0	0	1	Correct
8	1	1	1	1	1	Correct

Tinkercad:



Full adder using XOR, AND, OR gates with inputs 1,0,0