Digital Electronics

Experiment 6

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Aim:

Verify the truth table of one bit and two-bit comparator using logic gates (NOT, AND and OR).

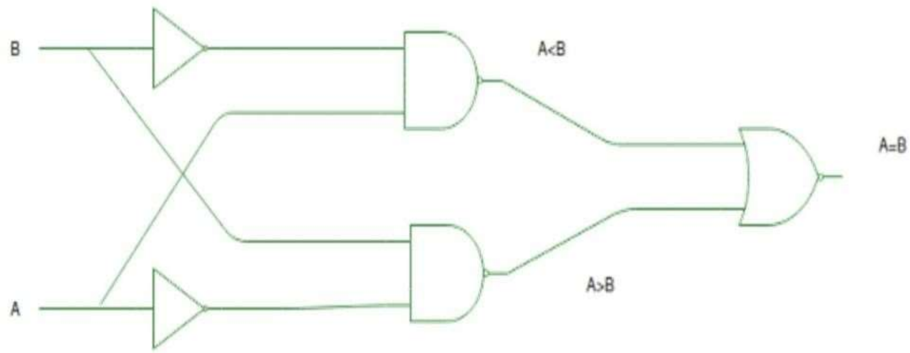
Theory:

A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number. We logically design a circuit for which we will have two inputs one for A and other for B and have three output terminals, one for A > B condition, one for A = B condition and one for A < B condition.

1-Bit Magnitude Comparator

A comparator used to compare two bits is called a single bit comparator. It consists of two inputs each for two single bit numbers and three outputs to generate less than, equal to and greater than between two binary numbers.

Circuit Diagram:



Truth Table:

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

From the above truth table logical expressions for each output can be expressed as follows:

A > B : AB'

A < B : A'B

A = B : A'B' + AB

1 Bit Magnitude Comparator

Truth Table

A	B	A < B	A = B	A ≥ B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

K-MAP

A < B

A \ B	0	1
0	0	1
1	0	0

$= \bar{A}B$

A = B

A \ B	0	1
0	1	0
1	0	1

$= \bar{A}\bar{B} + AB$

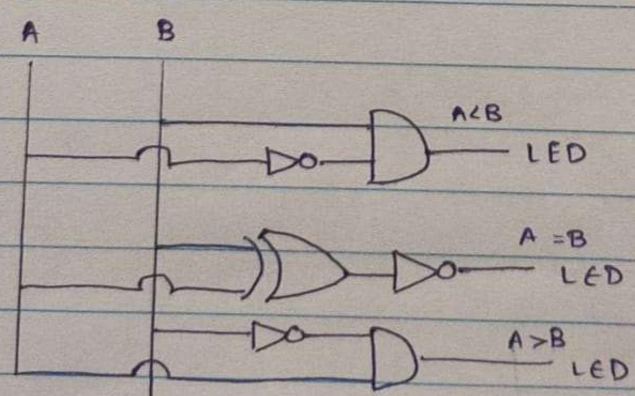
$= \overline{A \oplus B}$

A > B

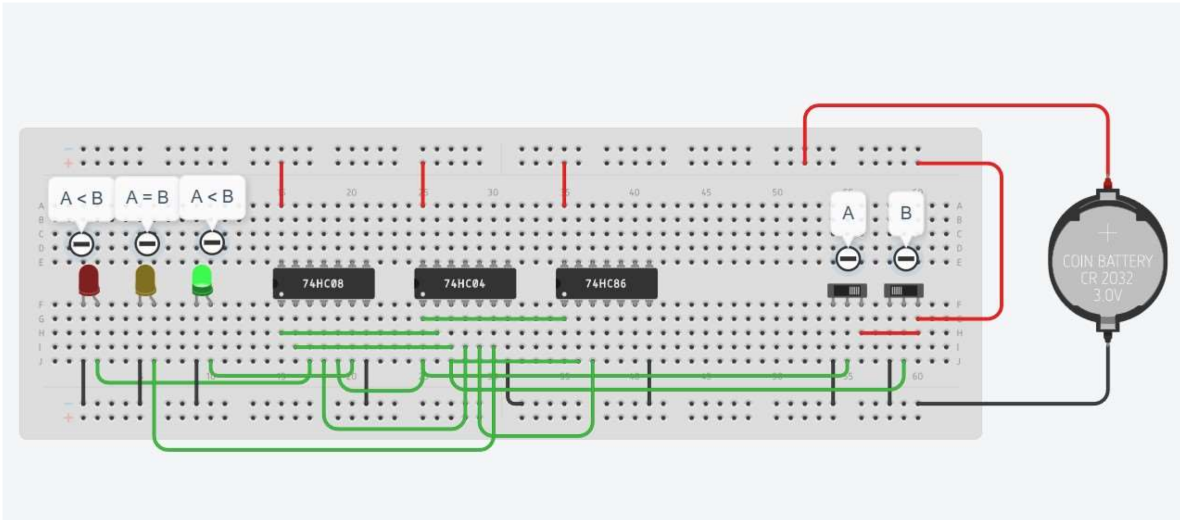
A \ B	0	1
0	0	0
1	1	0

$= A\bar{B}$

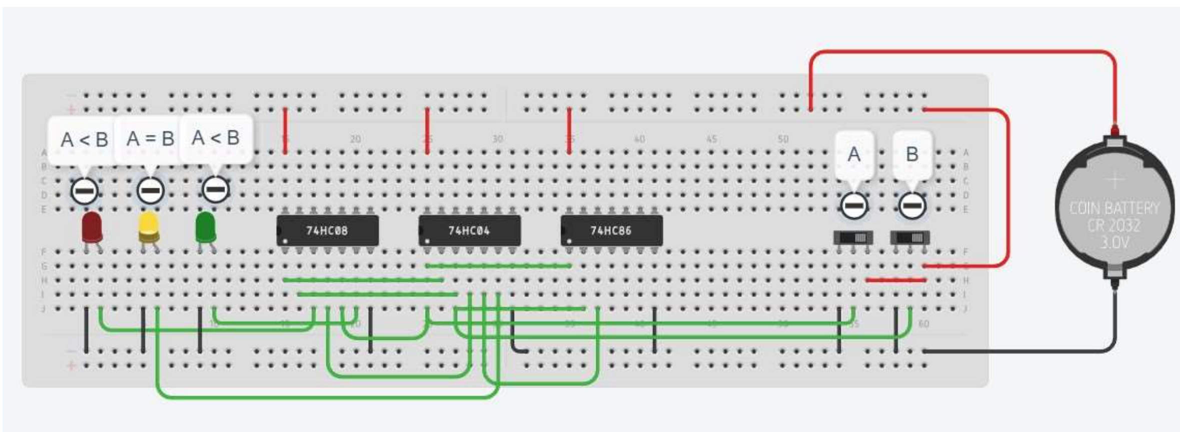
Realization



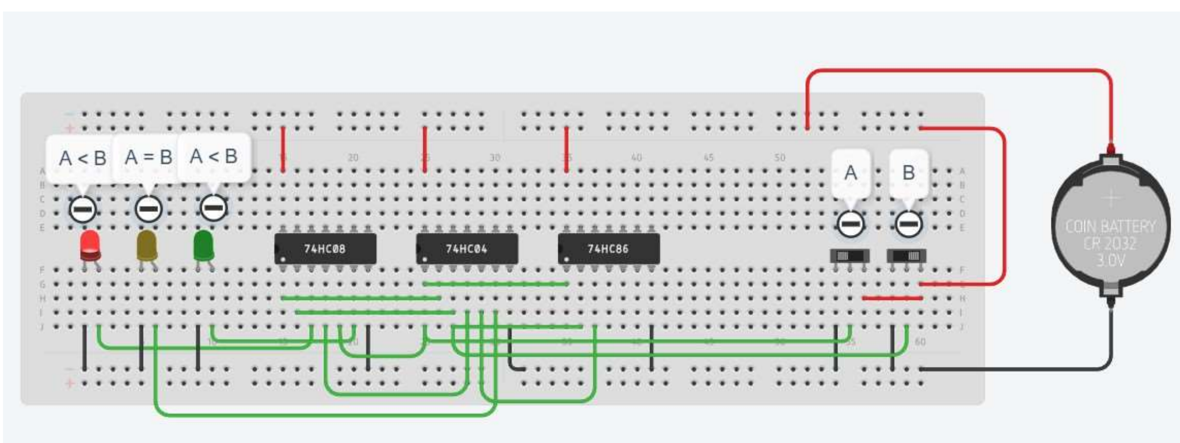
Tinkercad:



1-Bit Comparator using AND, NOT, XOR gates with inputs 1 and 0



1-Bit Comparator using AND, NOT, XOR gates with inputs 1 and 1

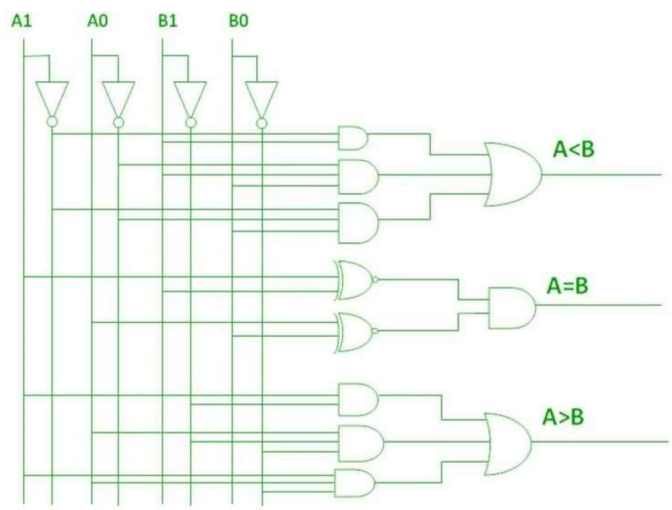


1-Bit Comparator using AND, NOT, XOR gates with inputs 0 and 1

2-Bit Magnitude Comparator

A comparator used to compare two binary numbers each of two bits is called a 2bit magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers.

Circuit Diagram:



Truth Table:

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

From the above truth table logical expressions for each output can be expressed as follows:

$A > B : A_1B_1' + A_0B_1'B_0' + A_1A_0B_0'$

$A = B : A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0B_1B_0 + A_1A_0'B_1B_0'$

$: A_1'B_1' (A_0'B_0' + A_0B_0) + A_1B_1 (A_0B_0 + A_0'B_0')$

$: (A_0B_0 + A_0'B_0') (A_1B_1 + A_1'B_1')$

$: (A_0 \text{ Ex-Nor } B_0) (A_1 \text{ Ex-Nor } B_1)$

$A < B : A_1'B_1 + A_0'B_1B_0 + A_1'A0'B0$

2 Bit Magnitude Compartor

Truth Table

A_1	A_0	B_1	B_0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

K-MAP

A<B

B_1B_0 \ A_1A_0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
1Φ	1	1	0	1
10	Φ	1	0	0

$= B_1\bar{A_1} + \bar{A_0}\bar{A_1}B_0 + \bar{A_0}B_1B_0$

A=B

B_1B_0 \ A_1A_0	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

~~K-MAP~~

$= \bar{A_1}\bar{A_0}\bar{B_1}\bar{B_0} + A_1A_0B_0B_1$

$+ \bar{A_1}\bar{B_1}B_0A_0 + \bar{B_0}\bar{A_0}A_1B_1$

$$(A = B) = \bar{A_1}\bar{A_0}\bar{B_1}\bar{B_0} + \bar{A_1}A_0\bar{B_1}B_0 + A_1\bar{A_0}B_1\bar{B_0} + A_1A_0B_0B$$

$$= \bar{A_1}\bar{B_1}(\bar{A_0}\bar{B_0} + A_0B_0) + A_1B_1(\bar{A_0}\bar{B_0} + A_0B_0)$$

$$= (\bar{A_1}\bar{B_1} + A_1B_1)(\bar{A_0}\bar{B_0} + A_0\bar{B_0})$$

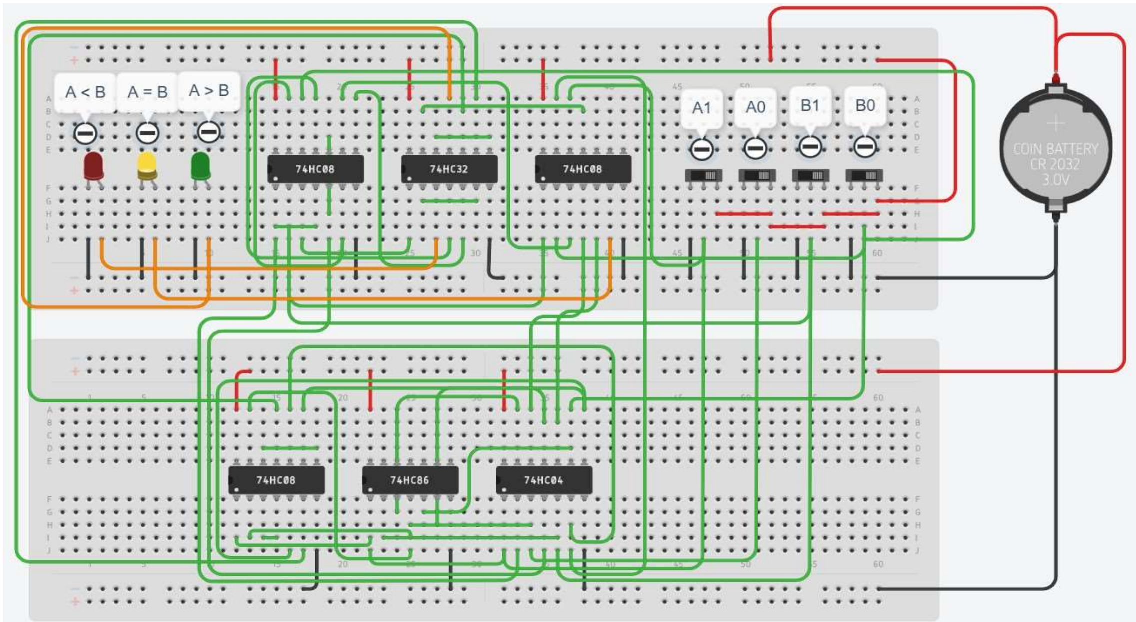
$$= (\overline{A_1 \oplus B_1}) \cdot (A_0 \oplus B_0)$$

A>B

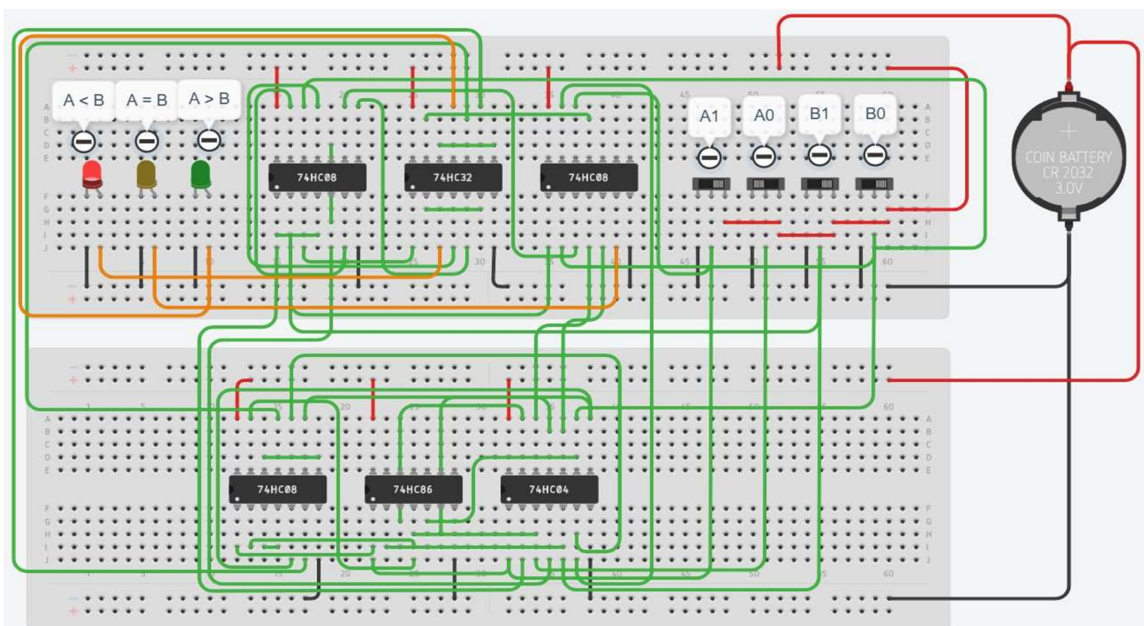
A_1A_0 \ B_1B_0	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

$$= \bar{B_1}A_1 + A_1A_0\bar{B_0} + \bar{B_1}\bar{B_0}A_0$$

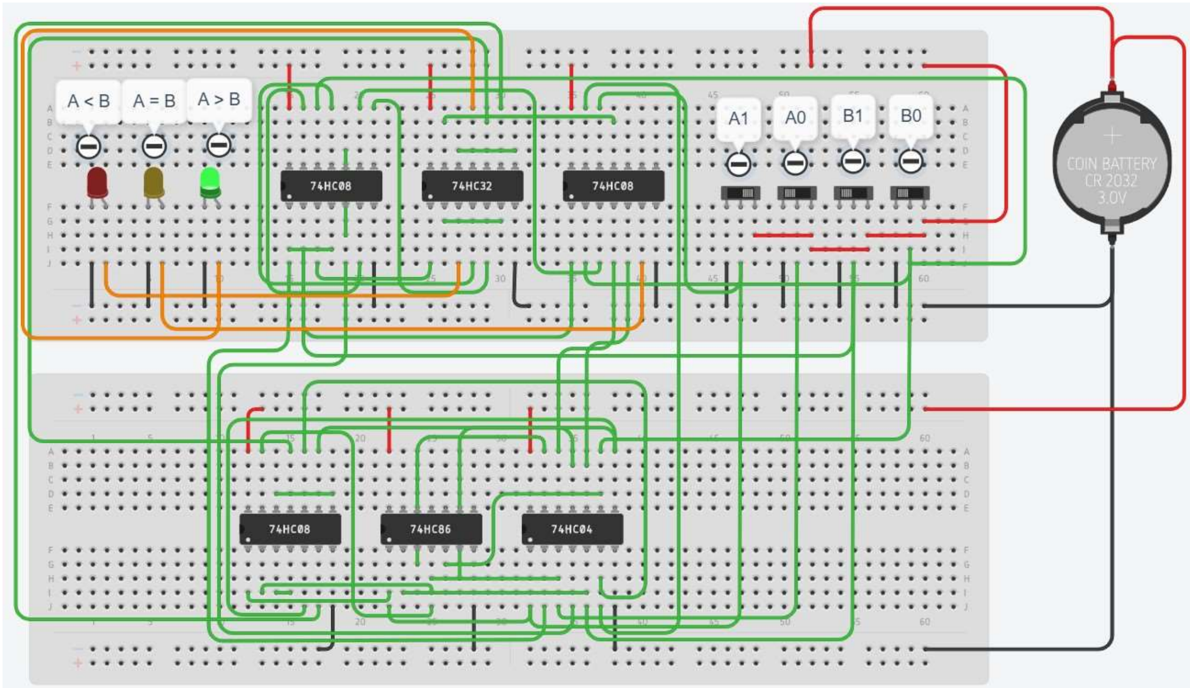
Tinkercad:



2-Bit Comparator using AND, OR, NOT, XOR gates with inputs 1, 1 and 1, 1



2-Bit Comparator using AND, OR, NOT, XOR gates with inputs 1, 0 and 1, 1



2-Bit Comparator using AND, OR, NOT, XOR gates with inputs 1, 0 and 0, 0