DIGITAL ELECTRONICS

EXPERIMENT – 8

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DIV: B1

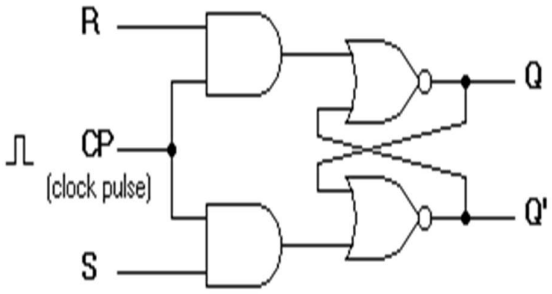
BRANCH: Computer Engineering

AIM: To verify the truth table and timing diagram of RS, JK, T and D flipflops by using NAND & NOR gates ICs and analyse the circuit of RS, JK, T and D flip-flops with the help of LEDs display.

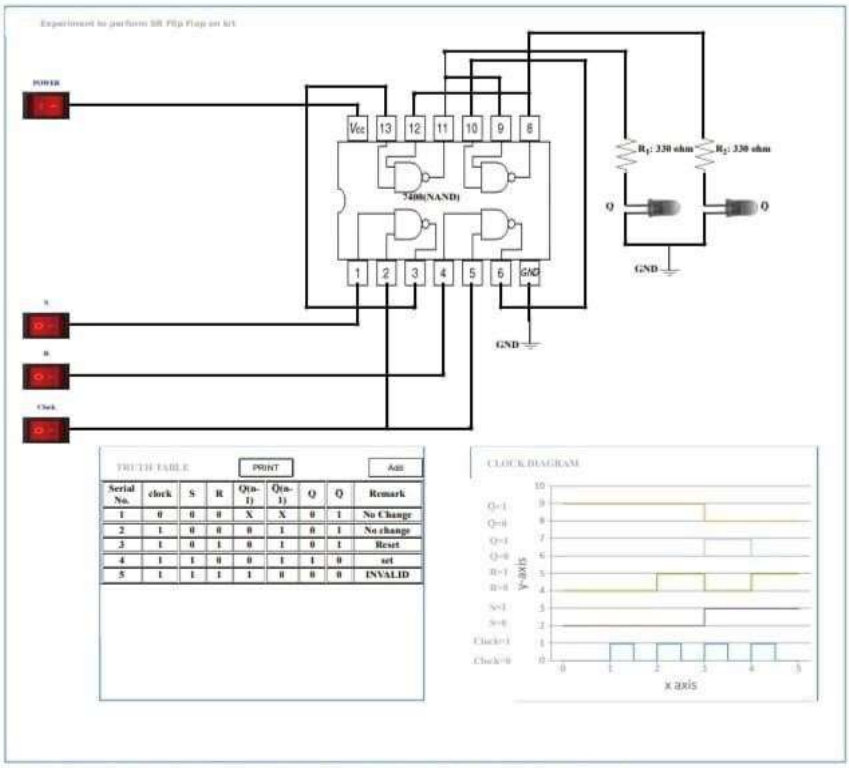
THEORY: A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs.

RS Flip Flop: The basic NAND gate RS flip flop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs. The RS flip flop actually has three inputs, SET, RESET and its current output Q relating to its current state.

Circuit Diagram and Truth Table:

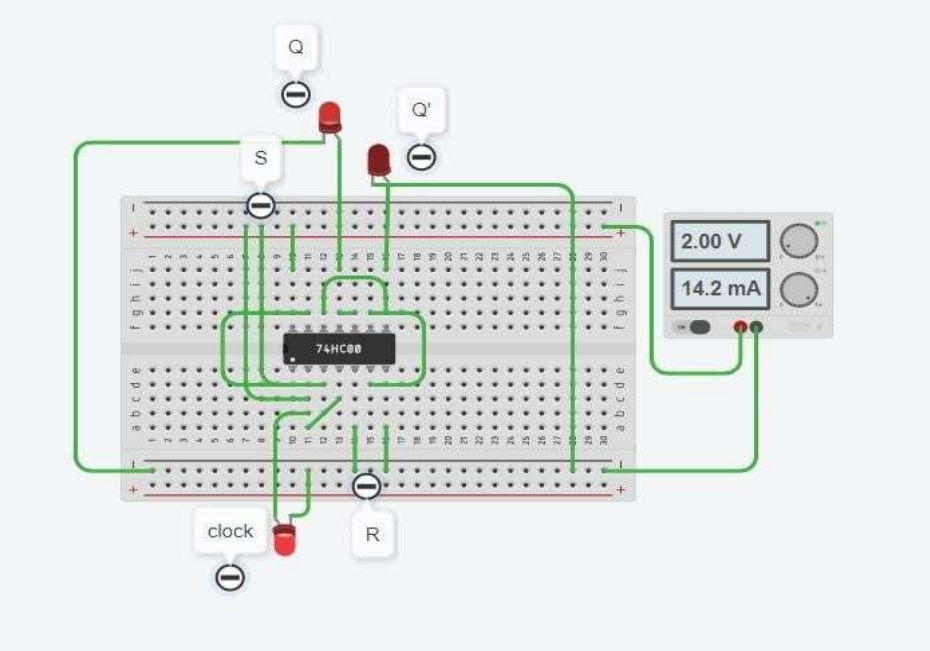


INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden



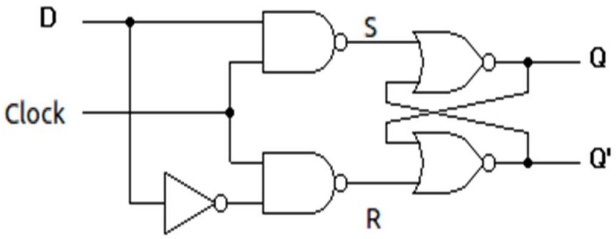
https://de-iitr.vlabs.ac.in/exp/truth-tables-flip-flops/round-template/experiment/simulation/SR FLIP FLOP/SRGraph.html

TINKERCAD:

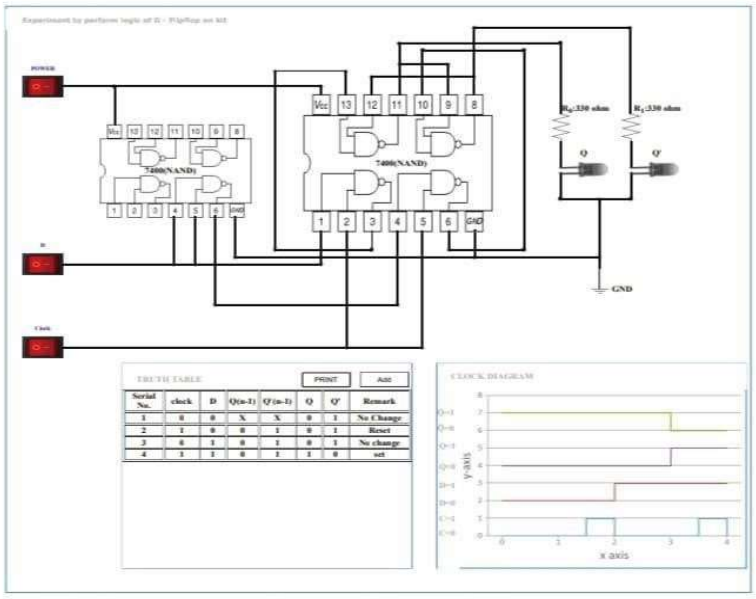


D Flip Flop: A D flip flop has a single data input. This type of flip flop is obtained from the SR flip flop by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked SR flip-flop is known as D-flip-flop.

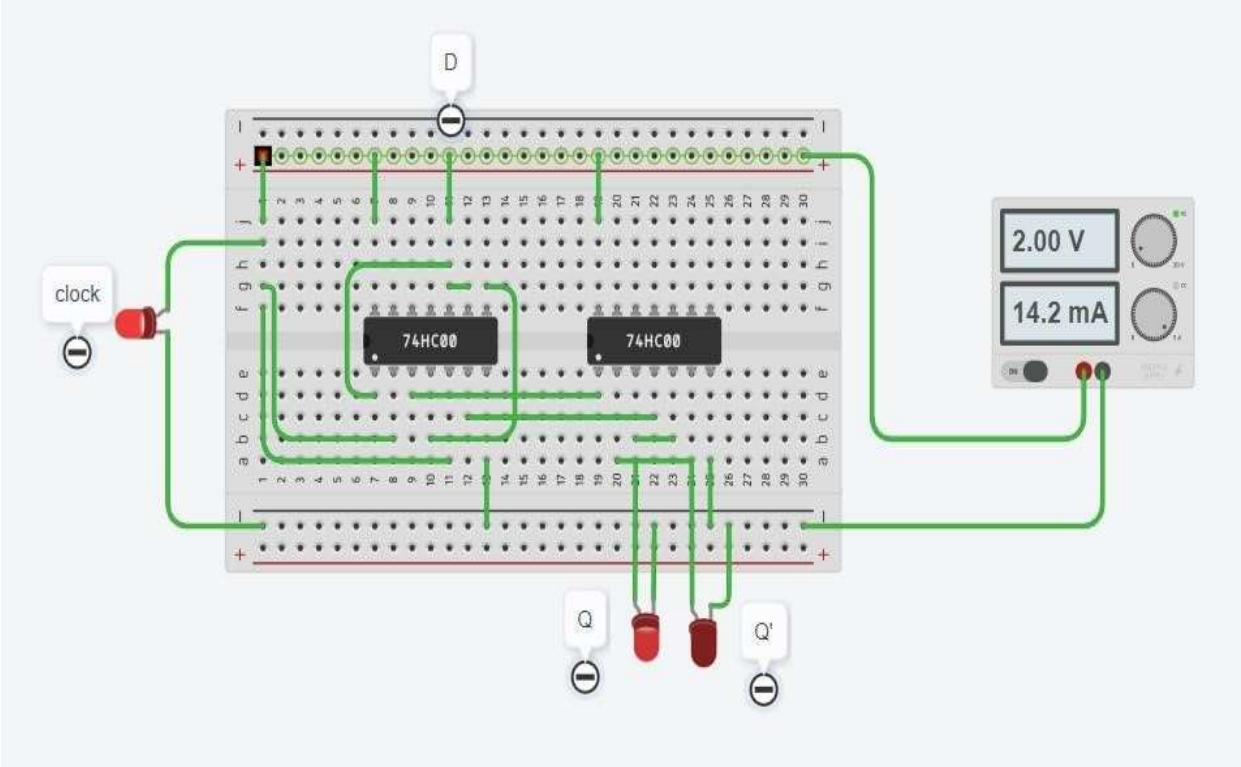
Circuit Diagram and Truth Table:



Input			Output	
D	reset	clock	Q	Q`
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

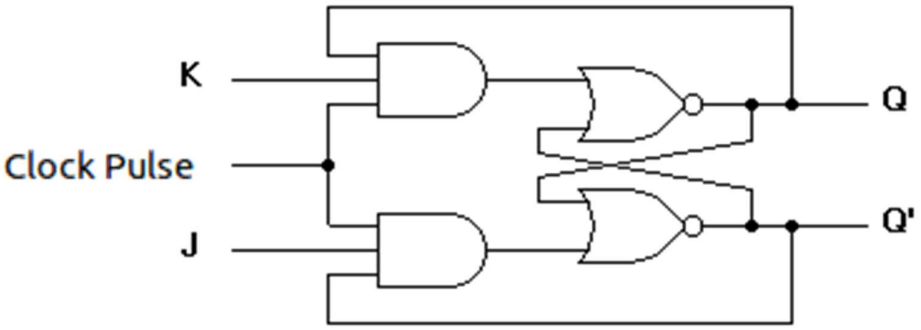

INSTRUCTIONS
7400(NAND)
7400(NAND)
GND
TRUTH TABLE
PRINT
Add
CLOCK DIAGRAM
y-axis
X axis

TINKERCAD:

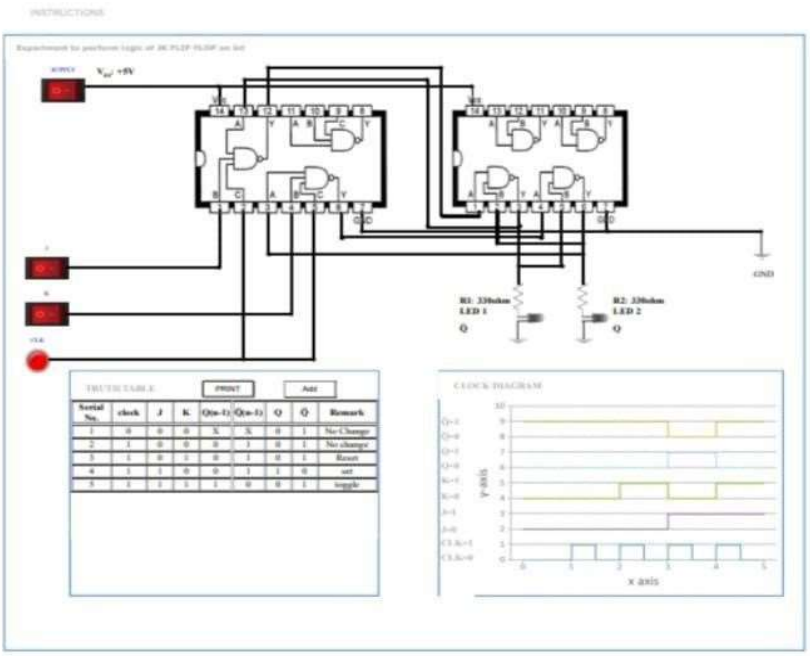

D
clock
74HC00
74HC00
2.00 V
14.2 mA
Q
Q'

J-K Flip Flop: In a RS flip-flop the input R=S=1 leads to an indeterminate output. The RS flip-flop circuit may be re-joined if both inputs are 1 than also the outputs are compliment of each other.

Circuit Diagram and Truth Table:



Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
⊠	x	x	-		-		Latched
⊓	0	0	0	1	0	1	No Change
⊓			1	0	1	0	
⊓	0	1	0	1	0	1	Reset
⊓			1	0	0	1	
⊓	1	0	0	1	1	0	Set
⊓			1	0	1	0	
⊓	1	1	0	1	1	0	Toggles
⊓			1	0	0	1	



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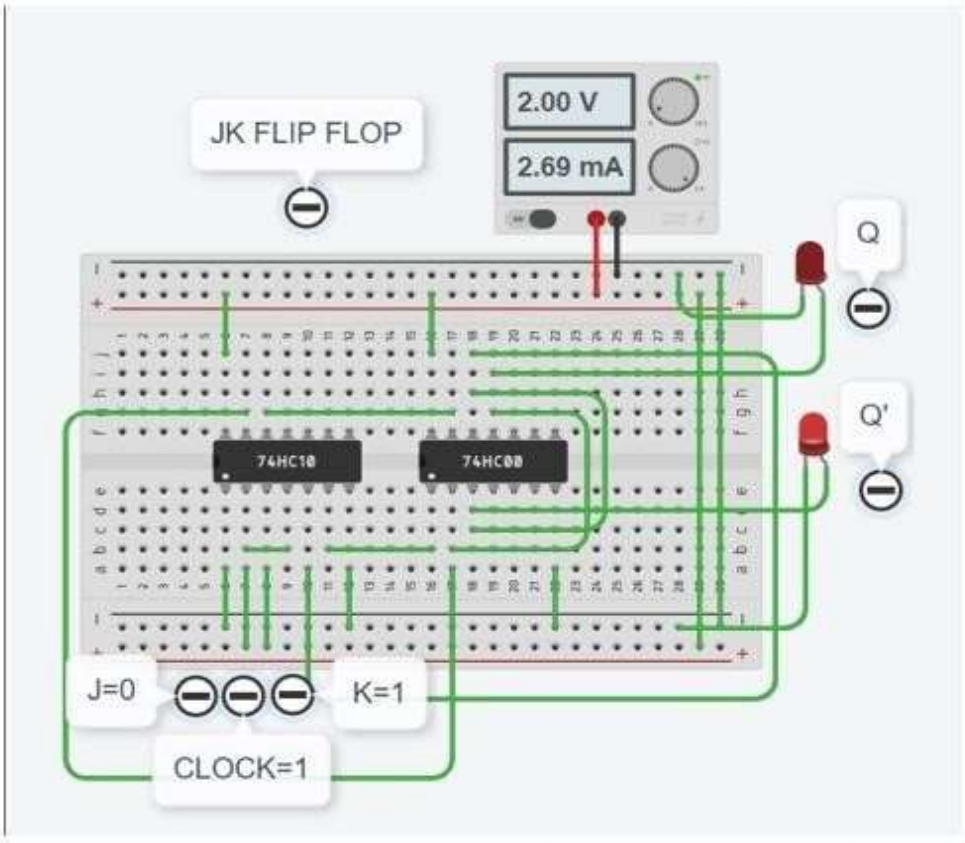
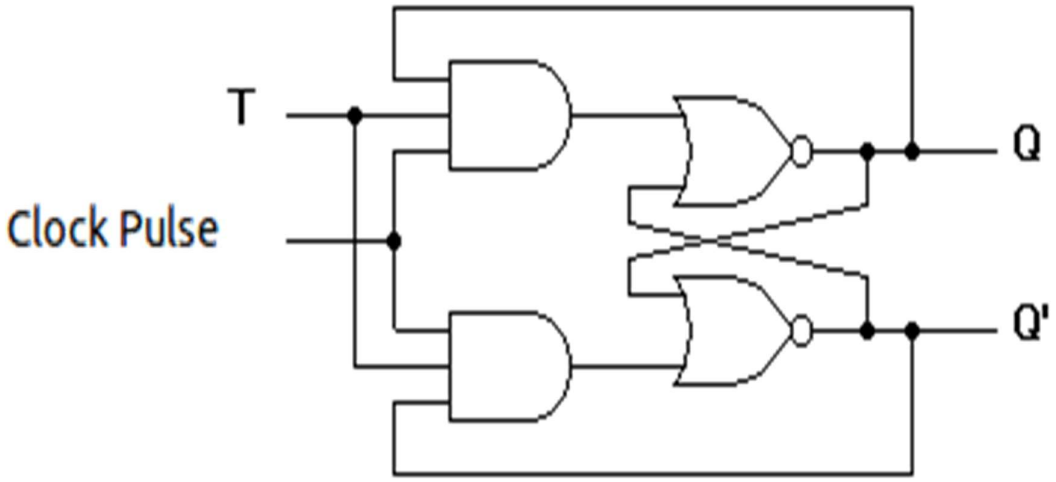


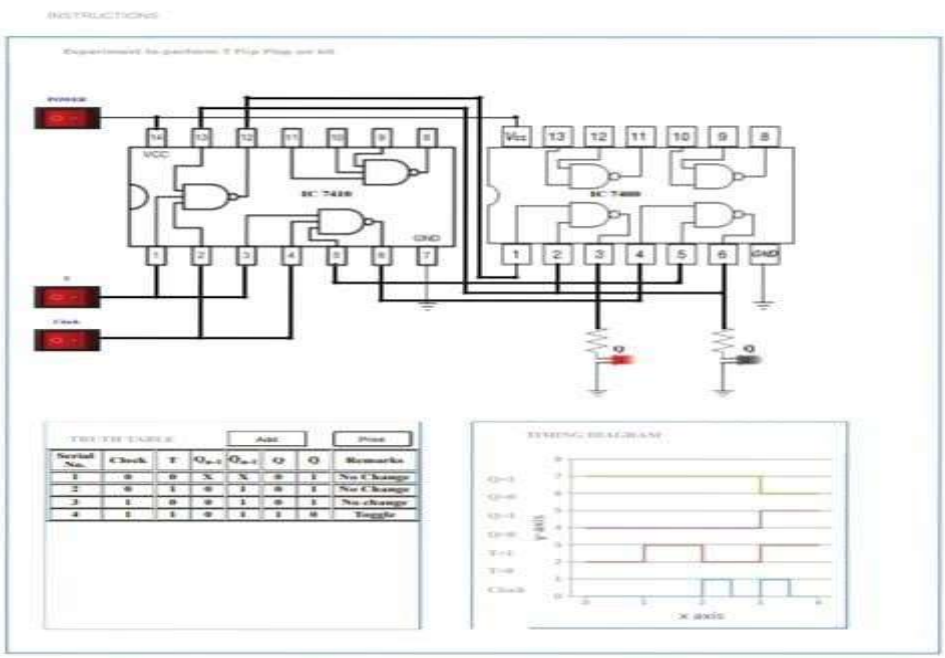
T Flip Flop: T flip-flop is known as toggle flip-flop. The T flip-flop is modification of the J-K flip-flop. Both the JK inputs of the JK flip – flop are held at logic 1 and the clock signal continuous to change.

Circuit Diagram and Truth Table:



T flip-flop

T	Clock	Q	Q'
0	↑	Q	Q'
1	↑	Q'	Q
X	↓	Q	Q'



https://de-iitr.vlabs.ac.in/exp/truth-tables-flip-flops/round-template/experiment/simulation/T FLIP FLOP/T.html

TINKERCAD: