A.Y. 2022-2023

PROCESSOR ORGANIZATION AND ARCHITECTURE AYUSH JAIN

COMPUTER ENGINEERING | TE - B2 | 60004200132

EXPERIMENT - 4

AIM: Demonstrate Cache Organization with Cache Simulator

THEORY:

Cache Memory is a special very high-speed memory. It is used to speed up and synchronizing with high-speed CPU. Cache memory is costlier than main memory or disk memory but economical than CPU registers. Cache memory is an extremely fast memory type that acts as a buffer between RAM and the CPU. It holds frequently requested data and instructions so that they are immediately available to the CPU when needed.

Cache memory is used to reduce the average time to access data from the Main memory. The cache is a smaller and faster memory which stores copies of the data from frequently used main memory locations. There are various different independent caches in a CPU, which store instructions and data.

DIRECT MAPPING

The simplest technique, known as direct mapping, maps each block of main memory into only one possible cache line. or In Direct mapping, assign each memory block to a specific line in the cache. If a line is previously taken up by a memory block when a new block needs to be loaded, the old block is trashed. An address space is split into two parts index field and a tag field. The cache is used to store the tag field whereas the rest is

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stored in the main memory. Direct mapping's performance is directly proportional to the Hit ratio.

i = j modulo m where

i=cache line number j= main memory

block number m=number of lines in

the cache

For purposes of cache access, each main memory address can be viewed as consisting of three fields. The least significant w bits identify a unique word or byte within a block of main memory. In most contemporary machines, the address is at the byte level.

FULL ASSOCIATIVE MAPPING

In this type of mapping, the associative memory is used to store content and addresses of the memory word. Any block can go into any line of the cache. This means that the word id bits are used to identify which word in the block is needed, but the tag becomes all of the remaining bits. This enables the placement of any word at any place in the cache memory. It is considered to be the fastest and the most flexible mapping form.

SET ASSOCIATIVE MAPPING

This form of mapping is an enhanced form of direct mapping where the drawbacks of direct mapping are removed. Set associative addresses the problem of possible thrashing in the direct mapping method. It does this by saying that instead of having exactly one line that a block can map to in the cache, we will group a few lines together creating a **set**. Then a block in memory can map to any one of the lines of a specific set. Set-associative mapping allows that each word that is present in the cache can have two or more words in the main memory for the same index address. Set associative cache mapping combines the best of direct and associative cache mapping techniques. In this case, the cache consists of a number of sets, each

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of which consists of a number of lines. The relationships are $m = v * k i = j \mod v$ where i=cache set number j=main memory block number v=number of sets

m=number of lines in the cache number of sets k=number of lines in each set

DEMONSTRATION:

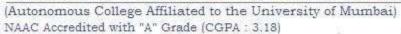
Direct Mapped (LRU: 1 word per block)

ordAddr	BinAddr	Tag	Index	0ffset	Hit/Mis
0	0000	00	00	n/a	mis
8	1000	10	00	n/a	mis
0	0000	00	00	n/a	mis
6	0110	01	10	n/a	mis
8	1000	10	00	n/a	mis
		Cache			
00	01		10	11	

Direct-mapped (LRU; 2 words per block)

WordAddr	BinAddr	Tag		Index Offset	Hit/Miss	
	0000 0011	0000		001	1	miss
180	1011 0100	1011	010 101			miss
43	0010 1011	0010			miss	
	0000 0010	0000		001	0	HIT
191	1011 1111	1011		111		miss
88	0101 1000	0101		100	0	miss
190				HIT		
14	0000 1110	9999		111	0	miss
181	1011 0101	1011		010		HIT
44	0010 1100 0010 110 0	0	miss			
186	1011 1010	1011		101	0	miss
253	1111 1101	1111		110		miss
		Cache				
9 001	010	011	100	101	110	111
2,3	180,181		88,89	186,187	252,253	14,15

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2-way set associative (LRU; 1 word per block)

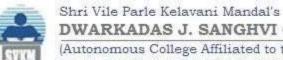
Hit/Mis	Offset	Index	Tag	BinAddr	WordAddr
mis	n/a	0	000	0000	0
mis	n/a	0	100	1000	8
HI	n/a	0	000	0000	0
mis	n/a	0	011	0110	6
miss	n/a	0	100	1000	8
			Cache		
	1			0	

3-way set associative (LRU; 2 words per block)

WordAddr	BinAddr	Tag	Index	Offset	Hit/Miss
3	0000 0011	00000	01	1	miss
180	1011 0100	10110	10	0	miss
43	0010 1011	00101	01	1	miss
2	0000 0010	00000	01	0	HIT
191	1011 1111	10111	11		miss
88	0101 1000	01011	00	0	miss
190	1011 1110	10111	11	0	HIT
14	0000 1110	00001	11	0	miss
181	1011 0101	10110	10		HIT
44	0010 1100	00101	10	0	miss
186	1011 1010	10111	01	0	miss
253	1111 1101	11111	10	1	miss
		Cache			
00	01		10	11	

Fully associative (LRU; 1 word per block)

Hit/Mis	0ffset	Index	Tag	BinAddr	WordAddr
mis	n/a	n/a	0000	0000	0
mis	n/a	n/a	1000	1000	8
HI	n/a	n/a	0000	0000	0
mis	n/a	n/a	0110	0110	6
HIT	n/a	n/a	1000	1000	8
			Cache		



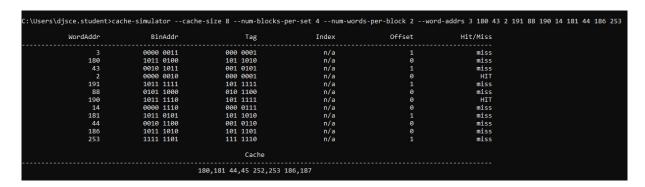




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Fully associative (LRU; 2 words per block)



CONCLUSION: Thus, Cache organization was implemented using cache simulator.