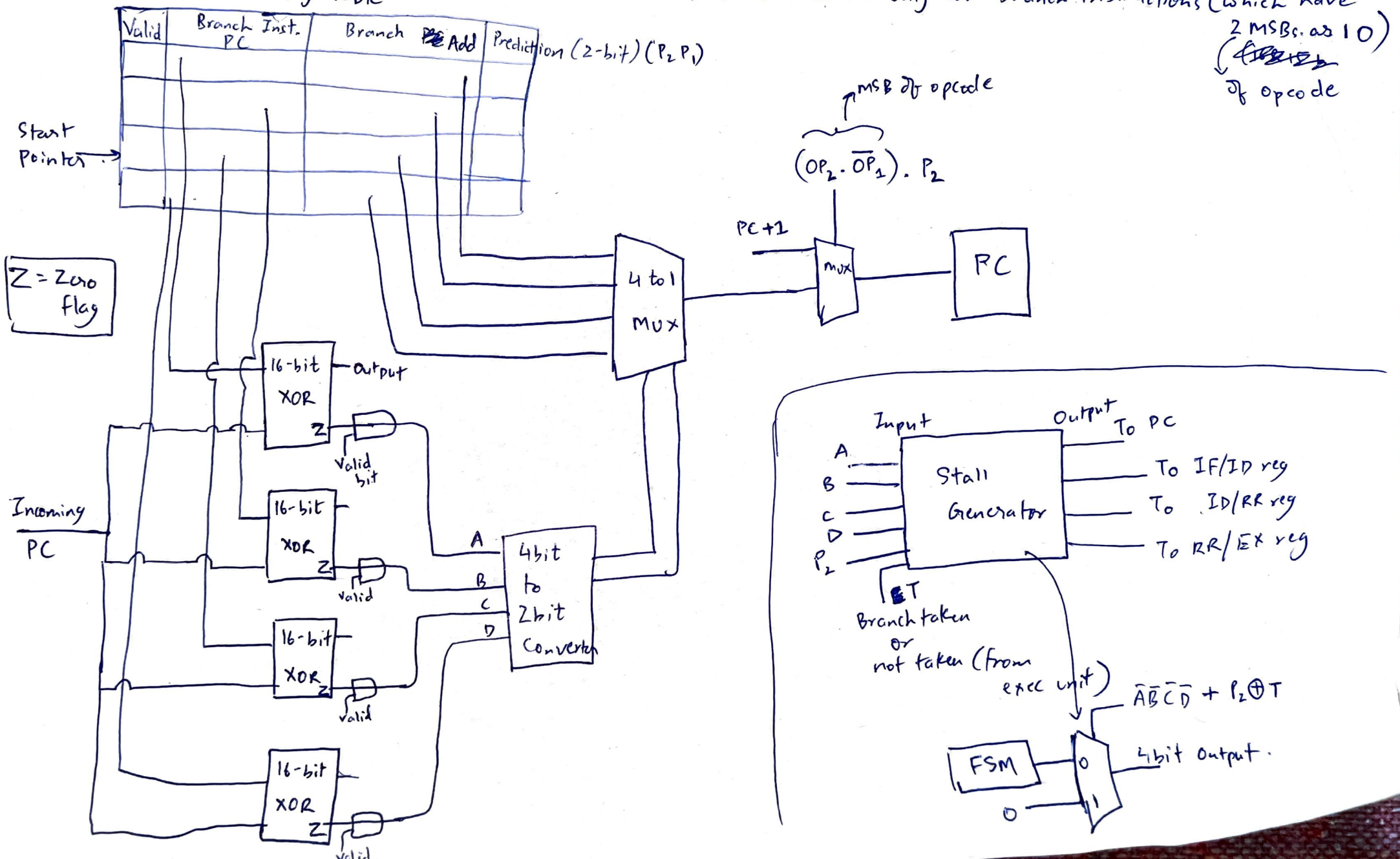
2-bit Branch Predictor design

4 entry Table

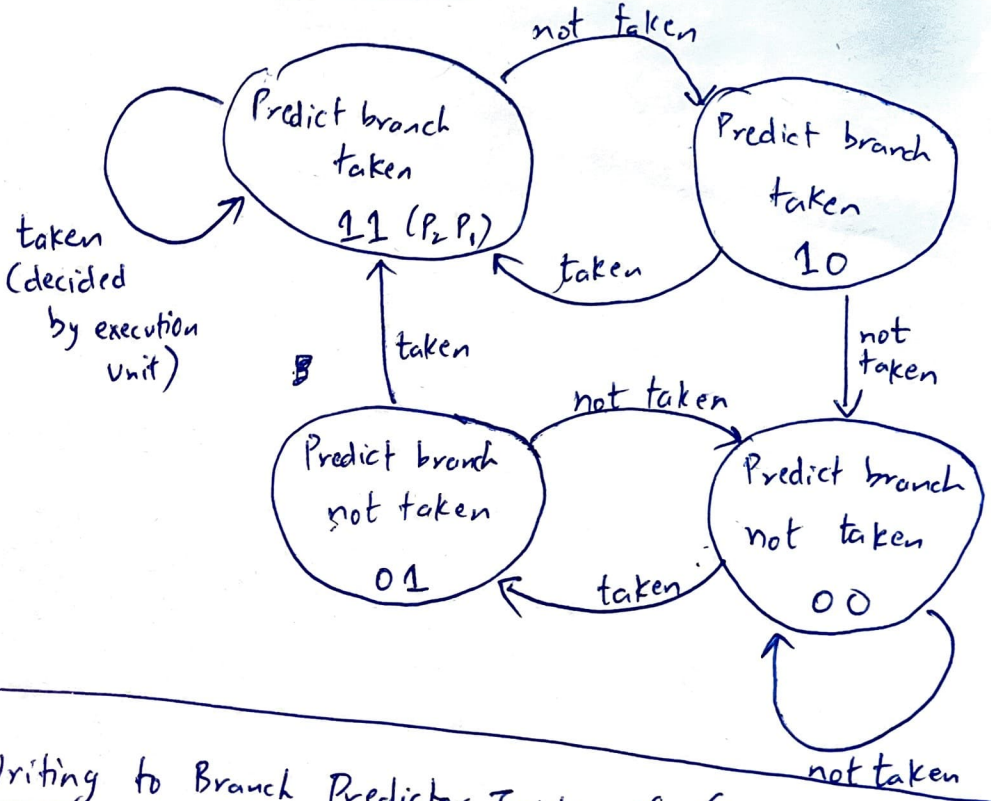
→ Branch Prediction only for branch instructions (which have 2 MSBs as 10 of opcode)



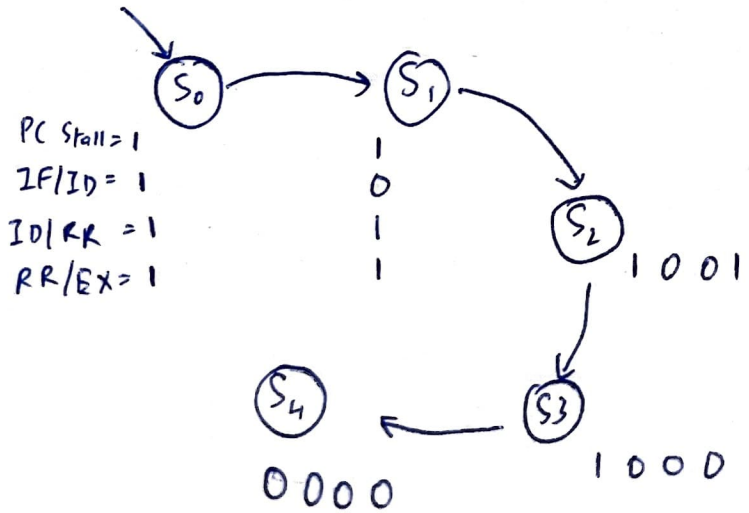
4-bit to 2-bit Converter.

A	B	C	D	Y_2	Y_1
1	0	0	0	0	0
0	1	0	0	1	1
0	0	1	0	1	0
0	0	0	1	0	1
All other Inputs				X	X

Prediction 2-bit FSM



Stall Manager FSM



Writing to Branch Predictor Table (of new branch instruction)

→ Start pointer points to memory cell in table where new Branch Instruction PC can be stored.

→ If $\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} = 1$, then new Branch Inst. PC written to Table. (& also its Branch Add)

→ Also Valid bit set to 1 after writing.