

2-bit Branch Predictor design

4 entry Table

→ Branch Prediction only for branch instructions (which have 2 MSBs. as 10)
~~(1010)~~
 of opcode

Valid	Branch Inst. PC	Branch PC Add	Prediction (2-bit) ($P_2 P_1$)

Start Pointer →

Z = Zero flag

Incoming PC

PC+1

MSB of opcode
 $(OP_2 \cdot \overline{OP_1}) \cdot P_2$

PC

4 to 1 MUX

MUX

16-bit XOR
Z

valid bit

16-bit XOR
Z

valid

16-bit XOR
Z

valid

16-bit XOR
Z

valid

4bit to 2bit Converter

Input
A
B
C
D
 P_2
ET
Branch taken or not taken (from exec unit)

Output To PC
To IF/ID reg
To ID/RR reg
To RR/EX reg

ET

Branch taken or not taken (from exec unit)

$\overline{A} \overline{B} \overline{C} \overline{D} + P_2 \oplus T$

FSM

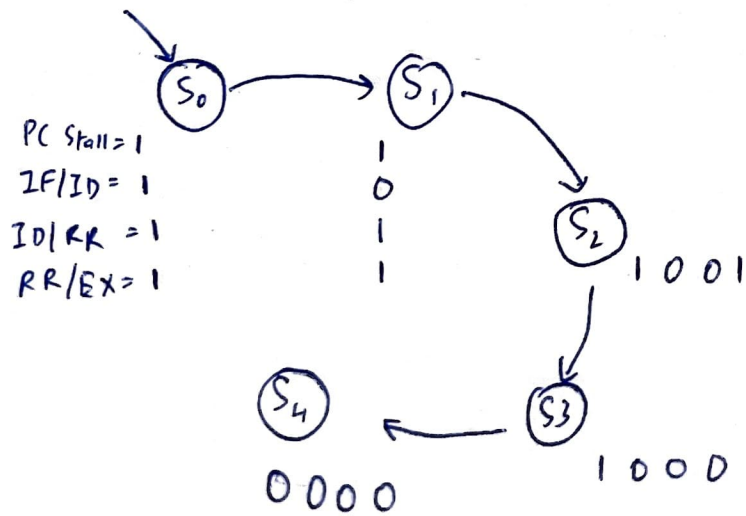
0

4bit output.

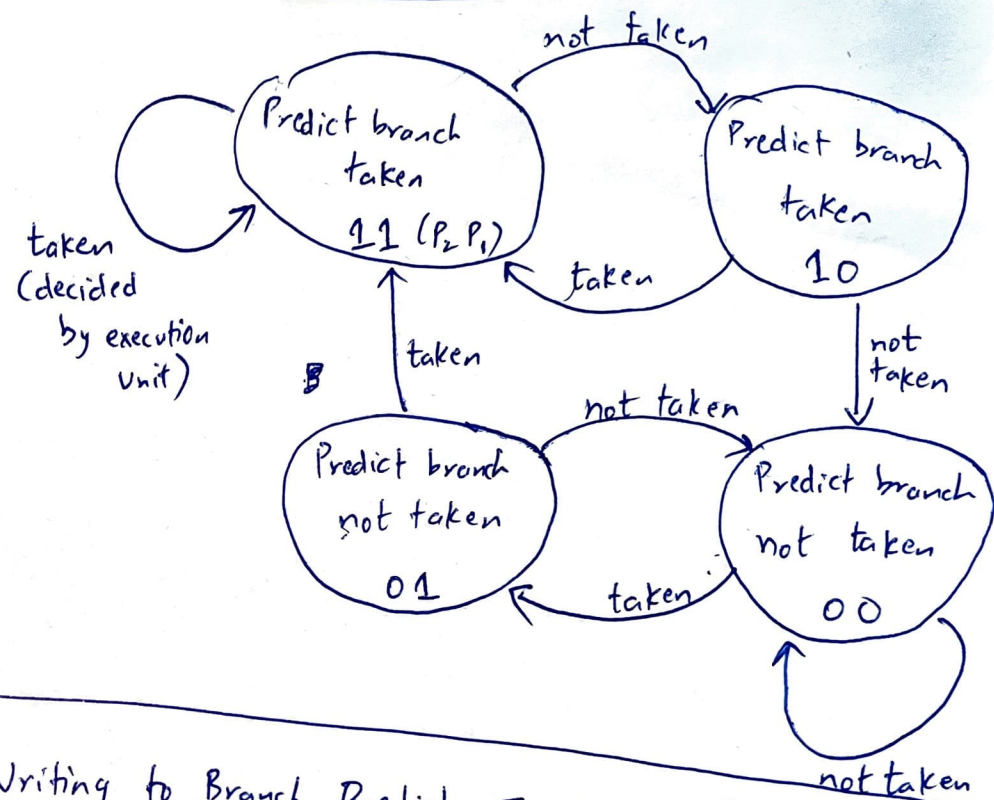
4-bit to 2-bit Converter.

A	B	C	D	Y_2	Y_1
1	0	0	0	0	0
0	1	0	0	1	1
0	0	1	0	1	0
0	0	0	1	0	1
All other inputs				X	X

Stall Manager FSM



Prediction 2-bit FSM



Writing to Branch Predictor Table (of new branch instruction)

- Start pointer points to memory cell in table where new Branch Instruction PC can be stored.
- If $\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} = 1$, then new Branch Inst. PC is written to Table. (& also its Branch Add)
- Also valid bit set to 1 after writing.