B.Tech. (Information Technology) Third Semester (C.B.C.S.)

Digital Electronics & Fundamentals of Microprocessor

P. Pages : 2

Time : Three Hours

* 2 7 8 6 *

PSM/KW/23/2583

Max. Marks : 70

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Due credit will be given to neatness and adequate dimensions.
8. Assume suitable data whenever necessary.
9. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Define Digital System. Compare Digital and Analog System? **6**

b) State and prove De-Morgan's theorem. Why NAND and NOR Gates are called as a Universal Gates. **8**

OR

2. a) Perform the following. **6**

i) $(4CE.12E)_H = (?)_8$

ii) $(10011.001)_B = (?)_G$

iii) $(156.56)_{10} = (?)_{BCD}$

b) i) Perform the following subtraction using BCD Subtraction Method. **4**

$(38)_{10} - (65)_8$

ii) Perform the following subtraction using $2^{'s}$ complement method **4**

$(AE)_{16} - (6)_{10}$

3. a) Simplify the following function $F(A,B,C) = \Pi M(0,2,4,6)$ and realize using NAND Gates only. **7**

b) Simplify following expression using K-MAP and realize the minimum Expression Using logic gates. **7**

$F(A,B,C,D) = \Pi M(4,6,8,9,10,12,13,14) + d(0,2,5)$

OR

4. a) Find reduced SOP form for the following equation by using K-MAP? **6**

$F(A,B,C,D) = \Sigma m(1,3,7,11,15) + \Sigma d(0,2,5,8,14)$

b) Design Logic Diagram for 4 bit binary to Grey code convertor. **8**

5. a) Design 8 bit BCD Adder Circuit by using 4 bit adder circuit (IC 7483). 8

b) Design Binary Parallel Subtractor using 1's Complement Method. Use full Adder circuit. 6

OR

6. a) Draw the logic diagram of 4:1 MUX using NAND gate only along with its truth table and explain it. 7

b) Construct 16:1 multiplexer by using 4:1 multiplexer. 7

7. a) Explain different methods of Triggering of Flip Flops. 6

b) Convert the following. 8

i) T to D Flip Floop

ii) JK to SR Flip Flop

OR

8. a) Explain the working of JK flip flop. What is race around condition and How it is eliminated. 7

b) Draw and explain the 4 bit Ripple counter with waveforms. 7

9. a) Give the format of flag Register in 8085 microprocessor and explain each flag. 5

b) Draw & Explain the Architecture of 8085 microprocessor in detail. 9

OR

10. a) Explain the addressing modes of 8085 microprocessor. 6

b) Explain the following instruction: 8

i) STAX B

ii) PUSH B

iii) LXI H, address

iv) LHLD address

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