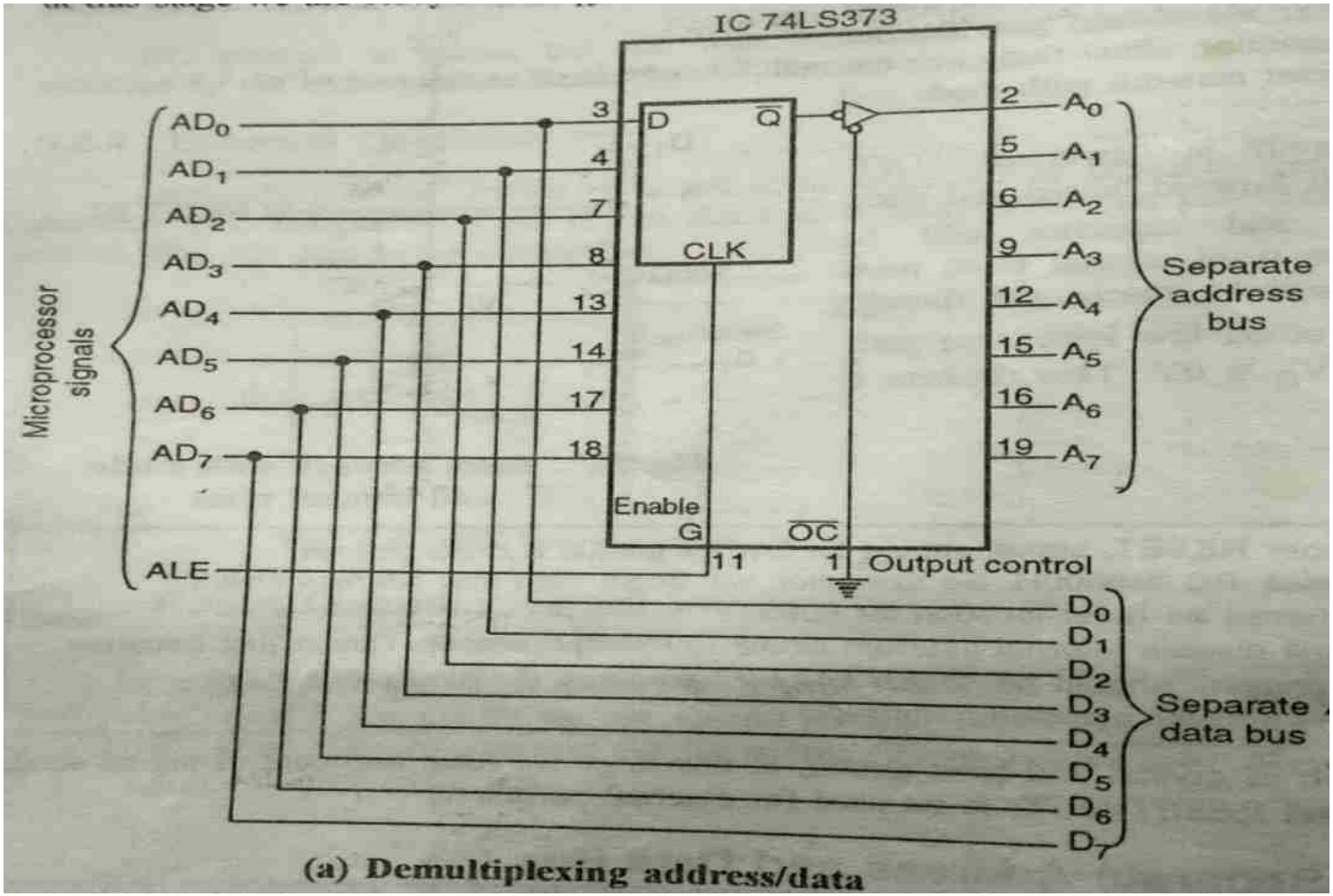
8 Bit Microprocessor 8085

Features of 8085

- It is 8 bit microprocessor i.e. it can accept or provide 8 bit data simultaneously
- It has 16 address lines hence it can access $2^{16} = 64K$ bytes of memory
- It has 8 data lines
- It requires a single +5V power supply
- It provides on chip clock generator
- Max operating clock frequency is 3MHz & minimum is 500KHz
- It provides 74 operation with following addressing modes: immediate ,register, direct, indirect & implied.
- The data bus is multiplexed with lower order address bus

Address / Data Demultiplexing

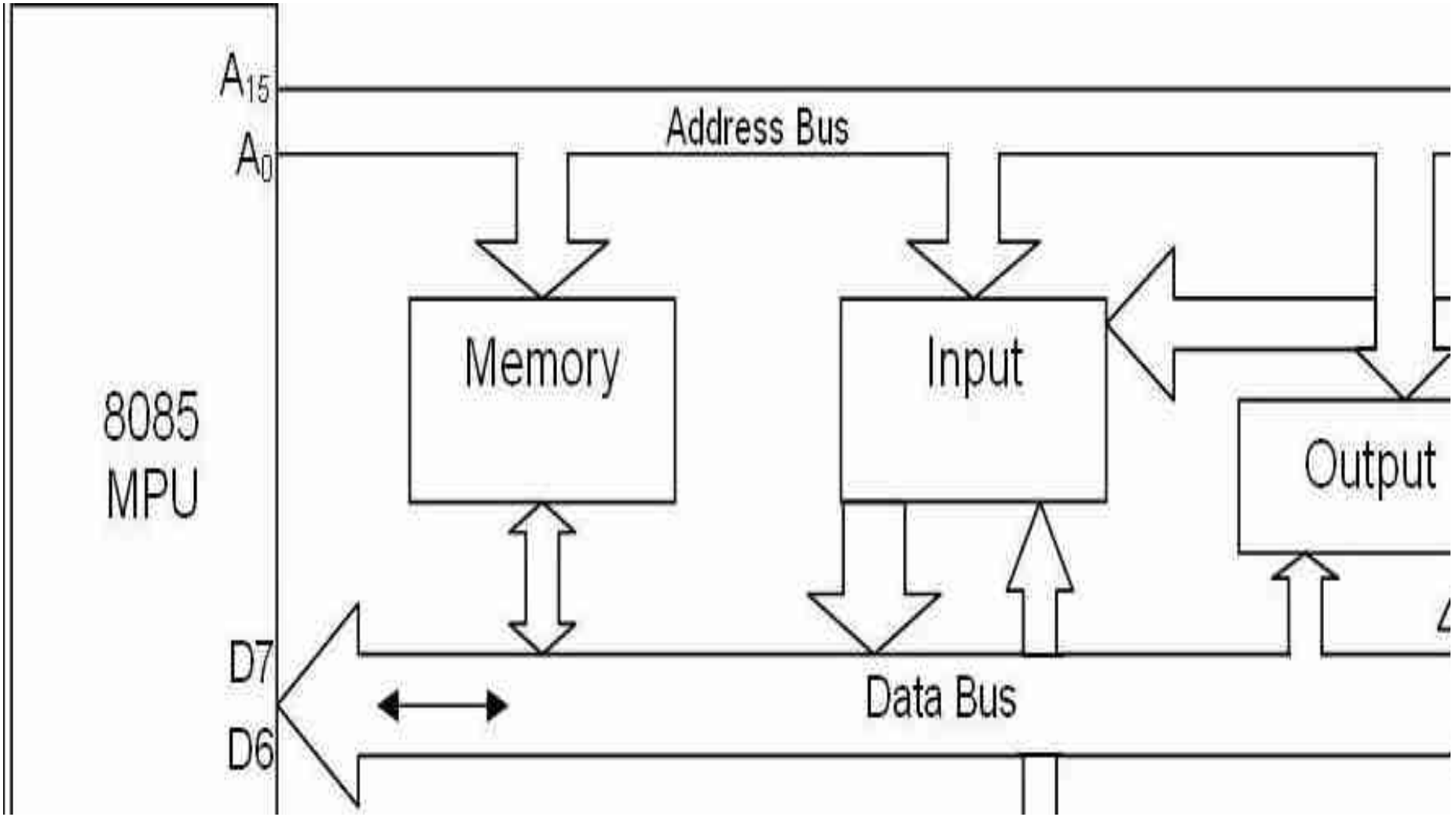


(a) Demultiplexing address/data

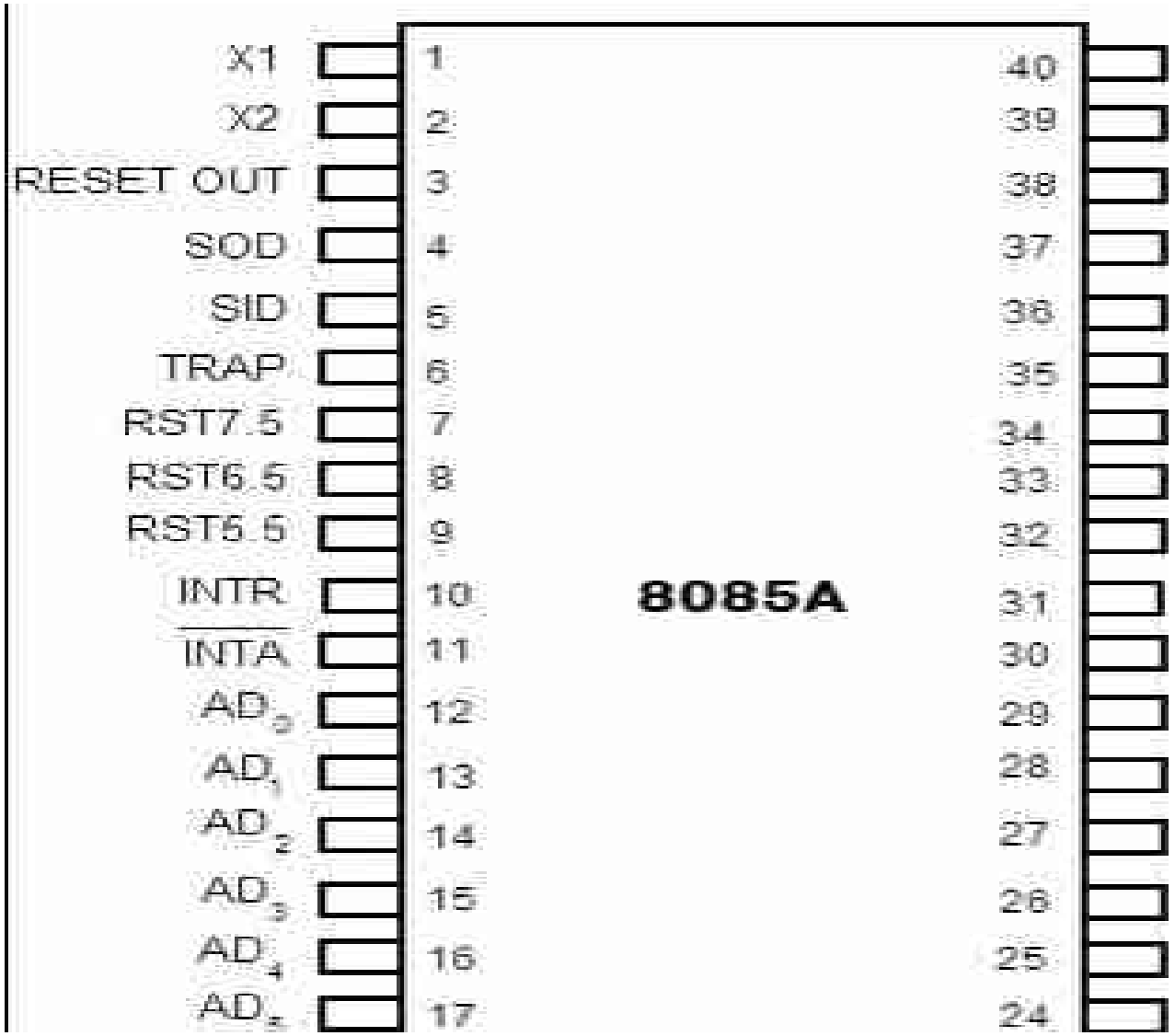
Features of 8085

- It generates 8 bit I/O address, hence it can access $2^8 = 256$ input ports & 256 output ports.
- It performs arithmetic & logical operation
- It provides 5 hardware interrupts :TRAP, RST7.5, RST6.5, RST5.5 & INTR
- It provides one accumulator, one flag register, 6 general purpose registers (i.e. B,C,D,E,H & L)& two special purpose register.
- It provides two serial I/O lines viz SOD & SID

8085 Bus Structure



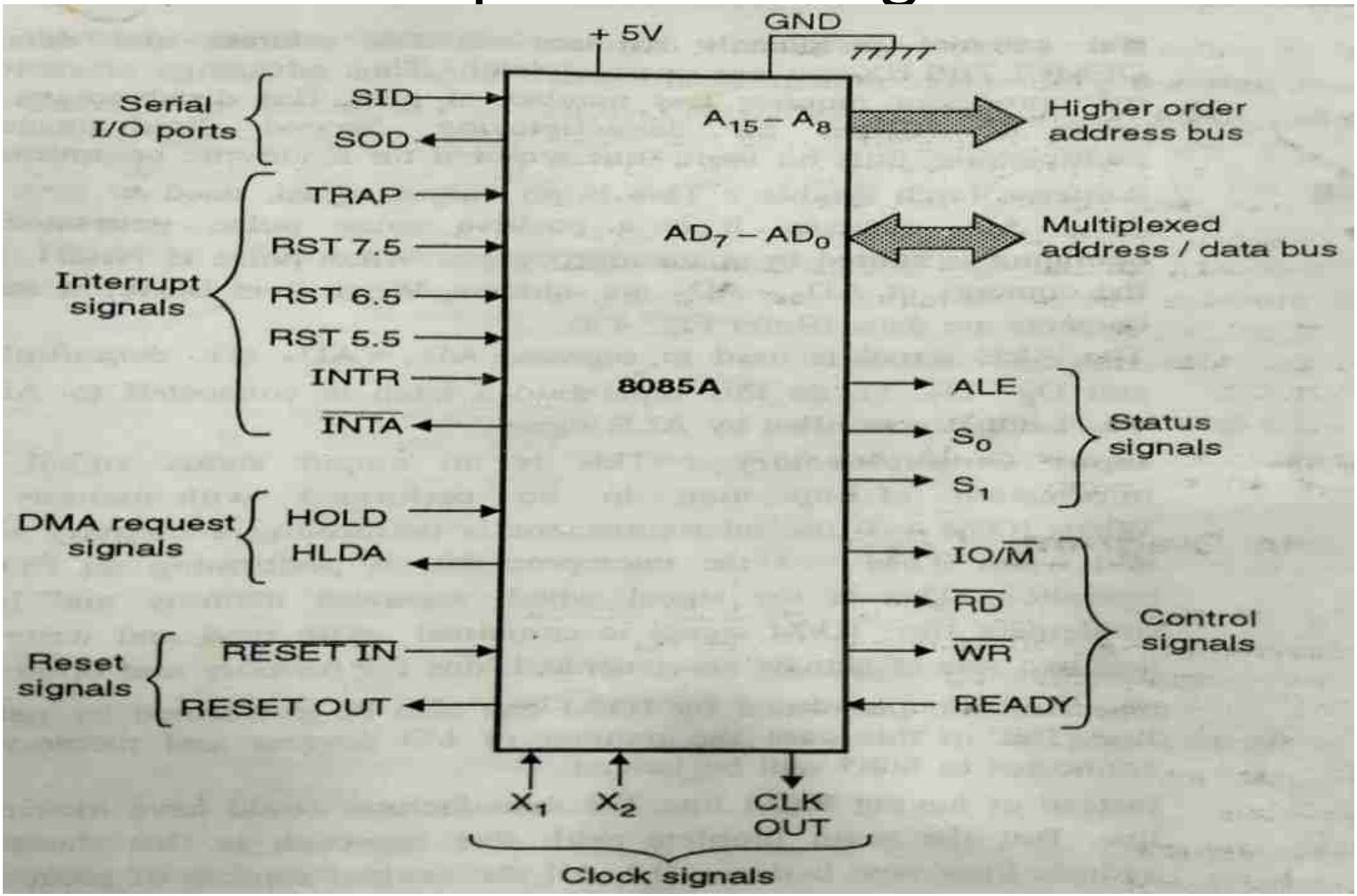
Pin Diagram of 8085



Group of 8085 Signals

- Address Bus
- Data Bus
- Status Signals
- Control Signals
- Clock Signals
- Reset Signals
- DMA Request Signals
- Interrupt Signals
- Serial I/O Ports

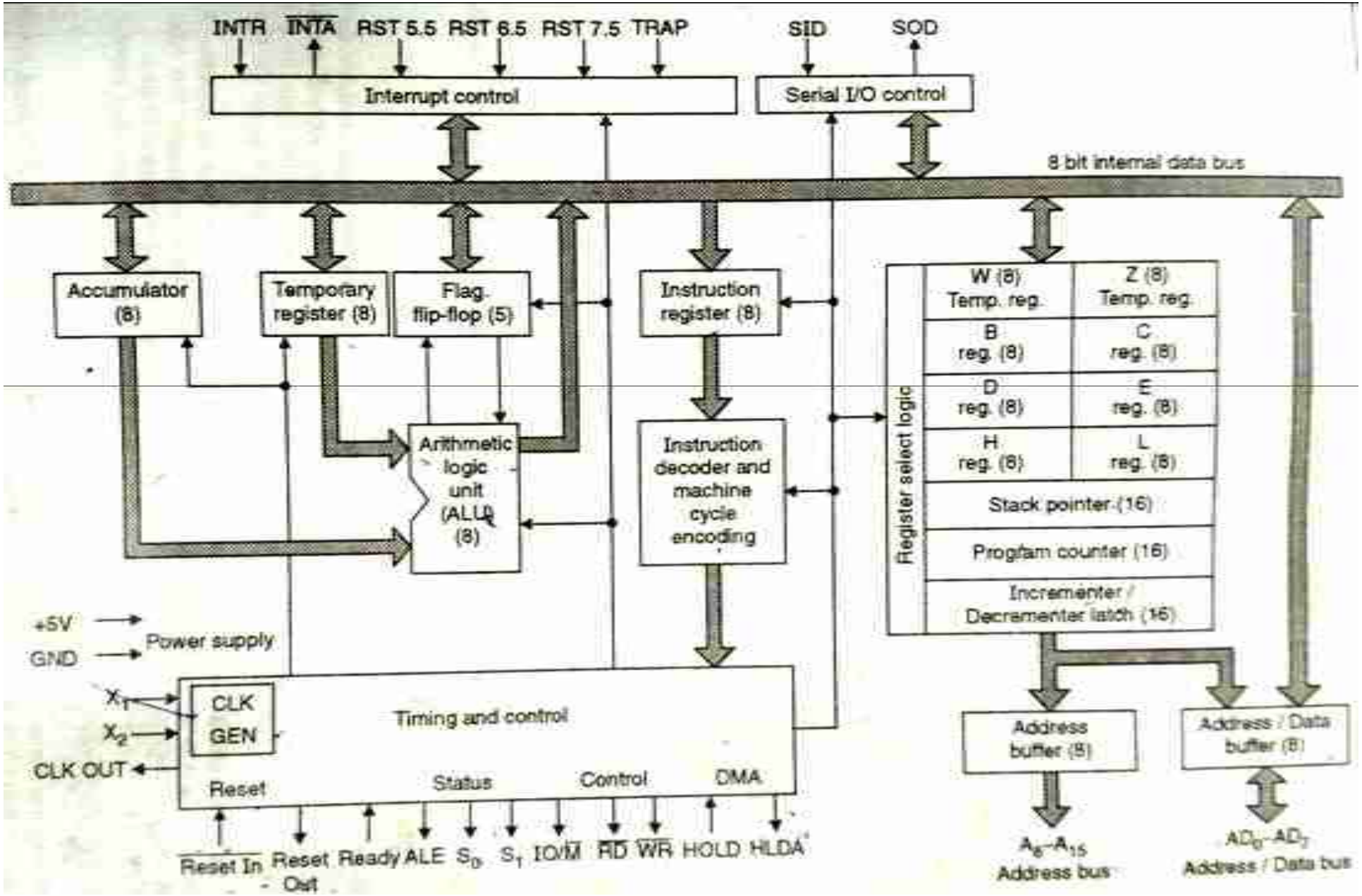
Group of 8085 Signals



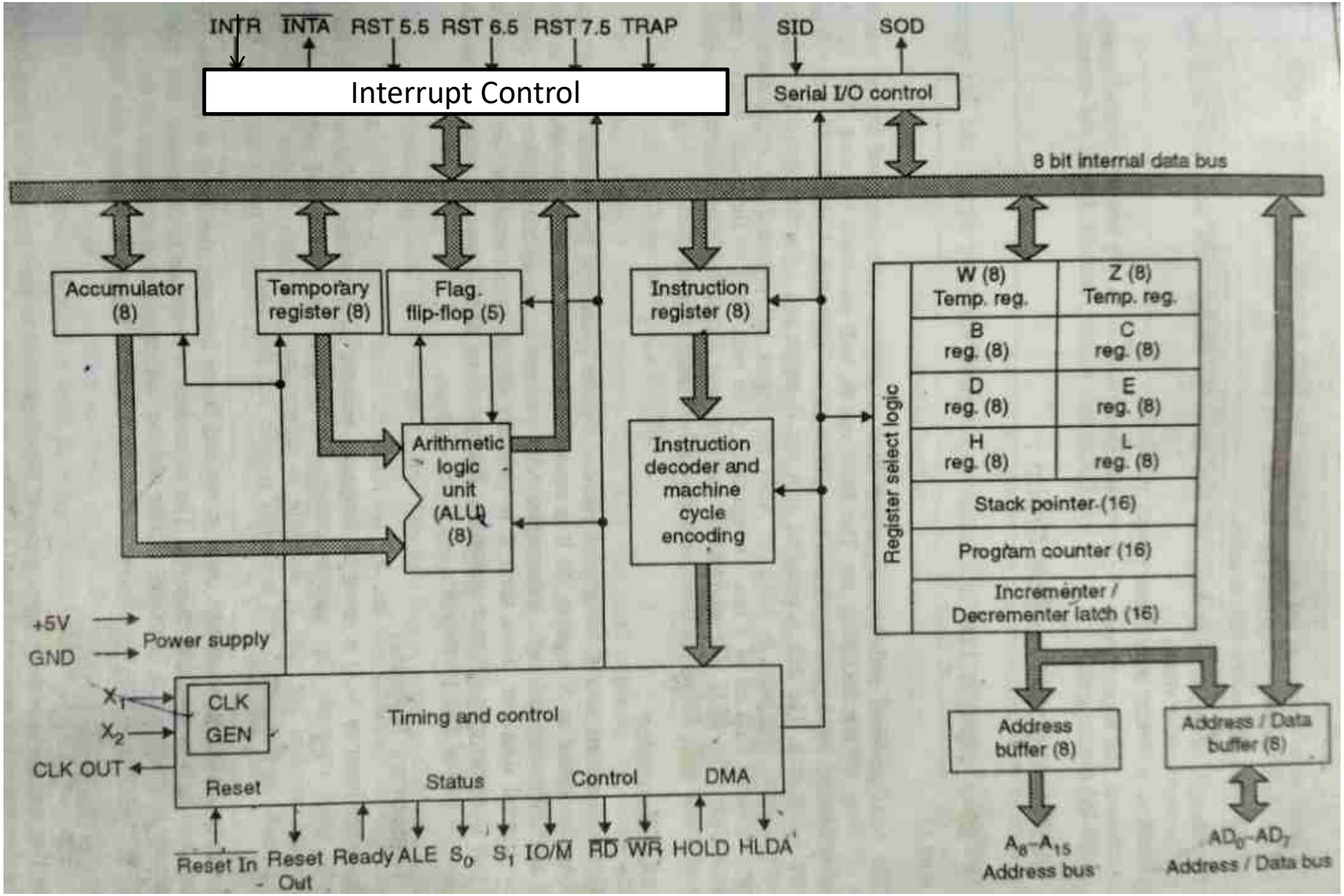
Architecture of 8085

- Interrupt control group
- Serial I/O control group
- Register group
- Instruction register, decoder, timing & control group
- Arithmetic & logical group

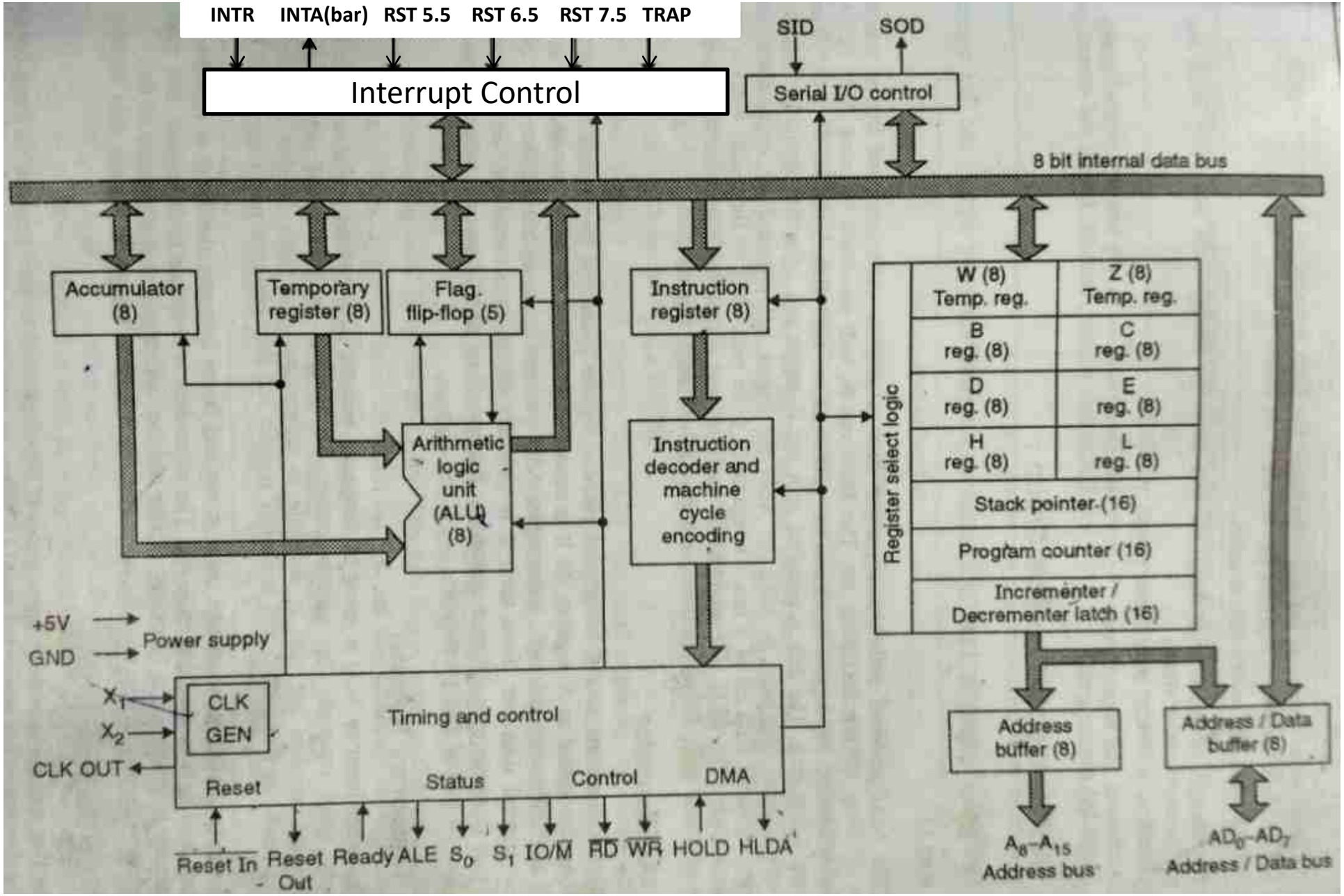
Architecture of 8085



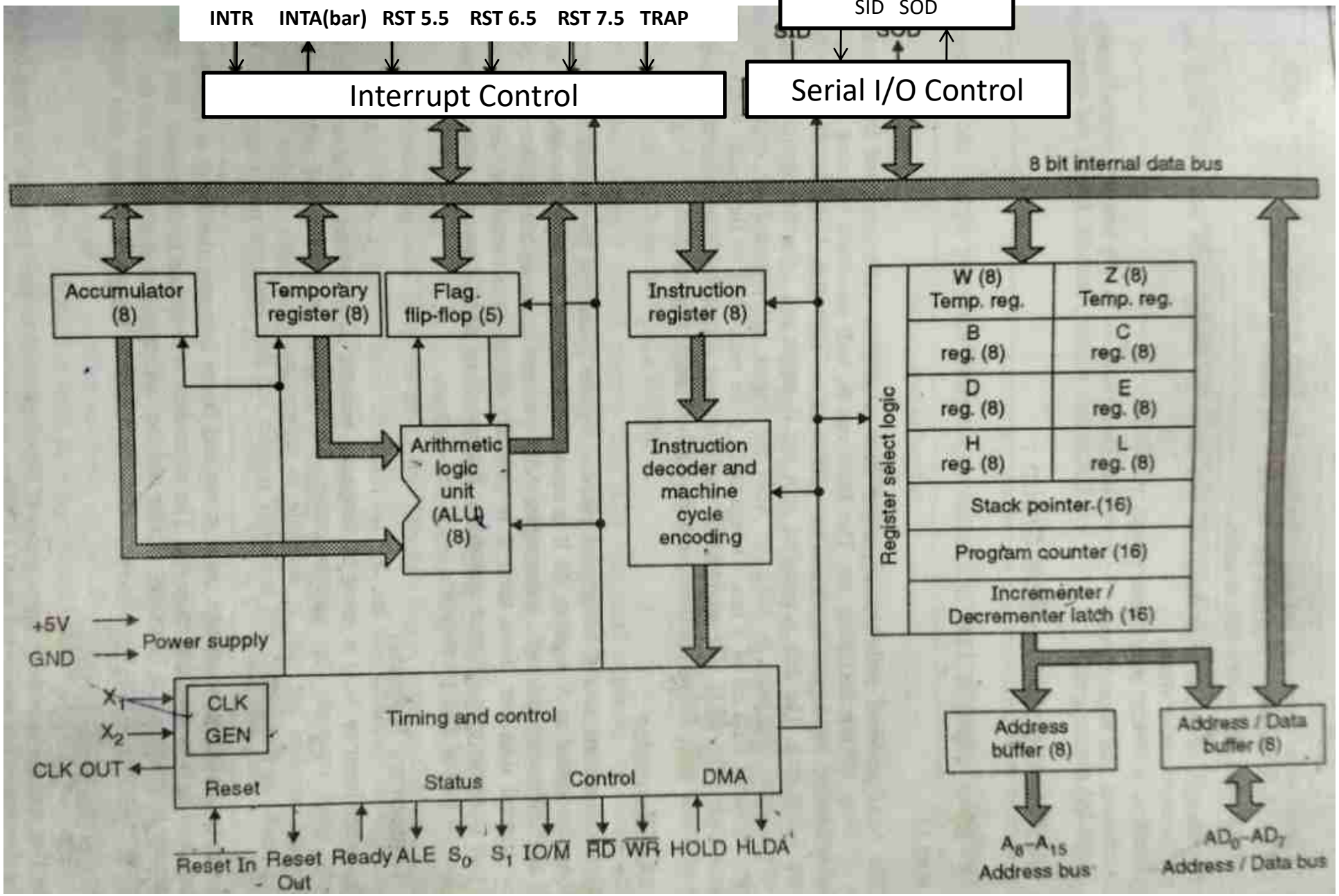
Architecture of 8085



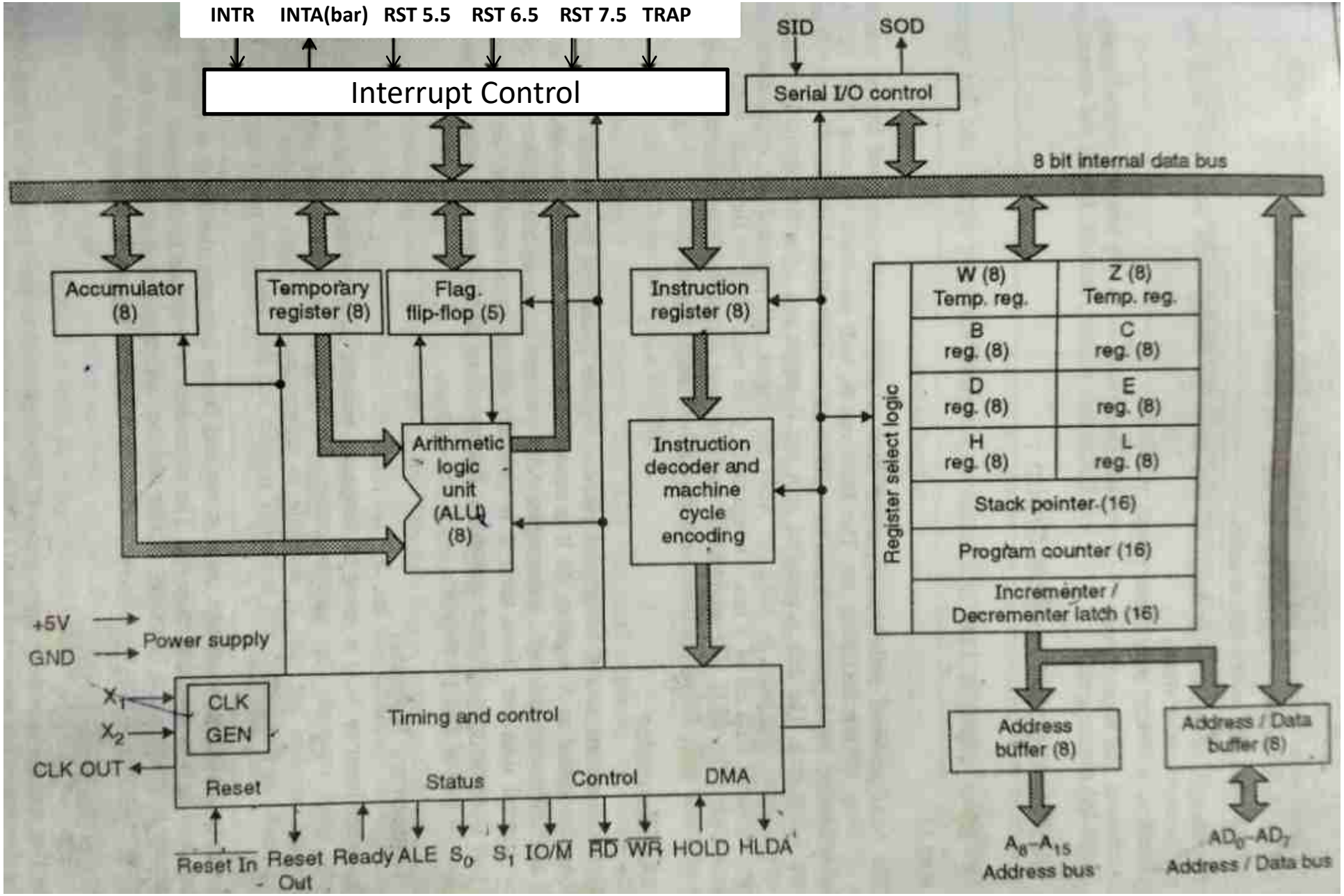
Architecture of 8085



Architecture of 8085



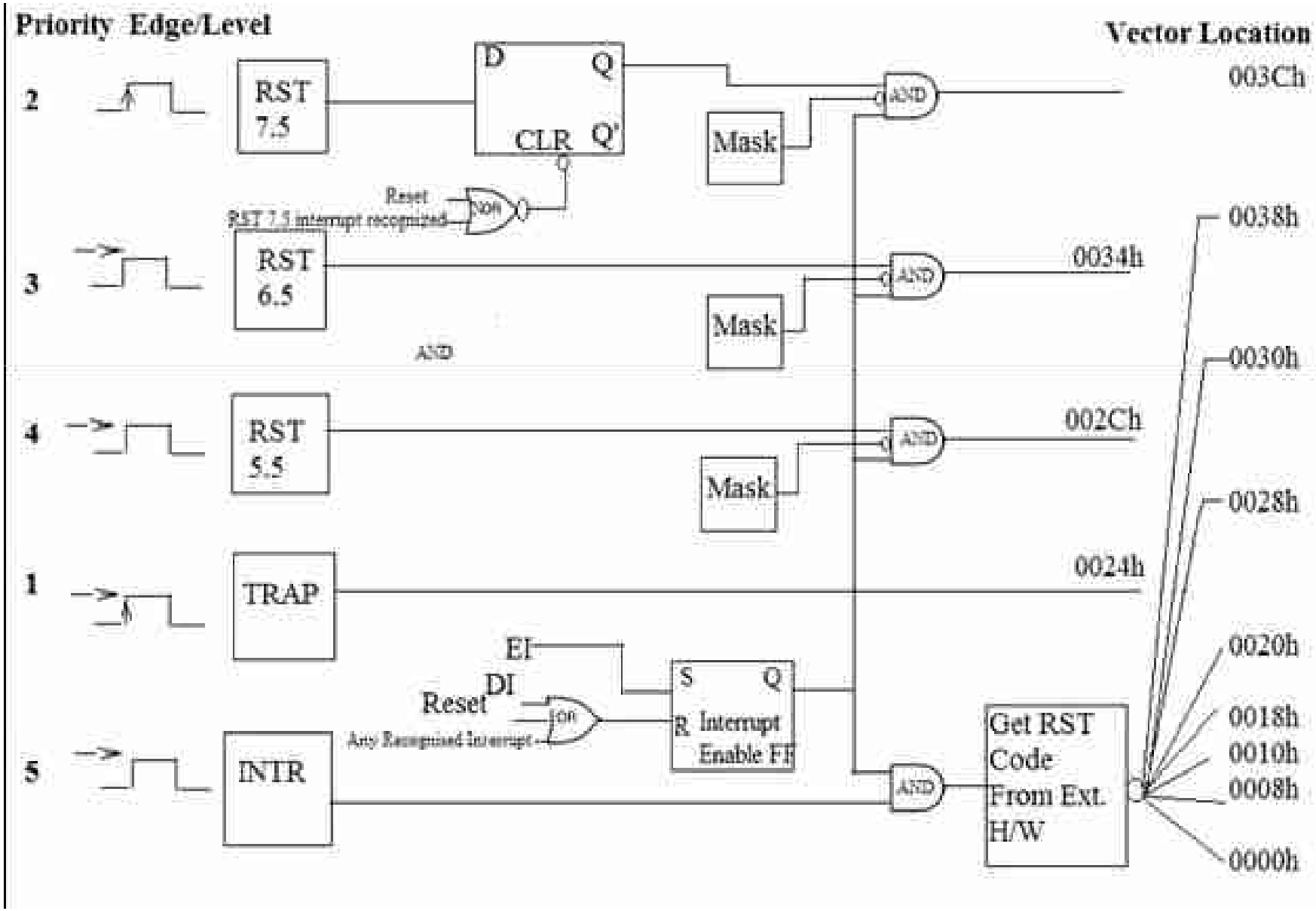
Architecture of 8085



Interrupt Control Group (Summary Table)

Interrupt Type	Trigger	Priority	Maskable	Provide Acknowle-dgement	Vector Address
TRAP	Edge & Level	1	No	No	0024H
RST 7.5	Edge	2	Yes	No	003CH
RST 6.5	Level	3	Yes	No	0034H
RST 5.5	Level	4	Yes	No	002CH
INTR	Level	5	Yes	Yes	----

Interrupt Structure



Serial I/O Control Group

SOD

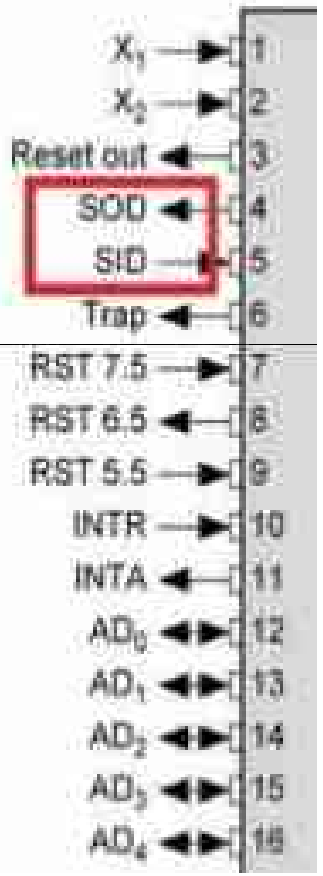
(Serial Output Data line)

The output SOD is set/reset as specified by the SIM instruction.

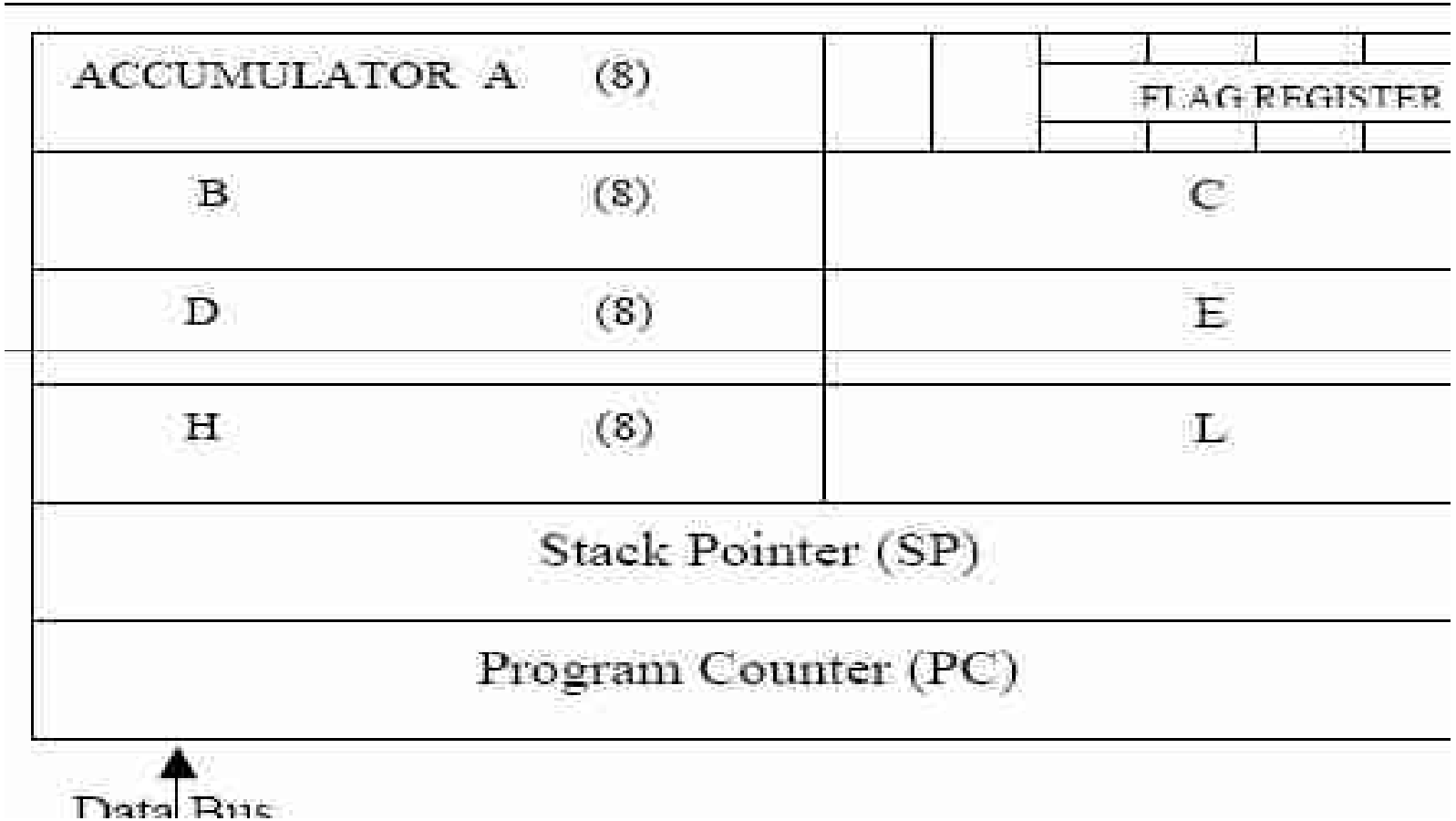
SID

(Serial Input Data line)

The data on this line is loaded into accumulator whenever a RIM instruction is executed.



Register Group



Flag Register (PSW)

- Sign Flag
- Zero Flag
- Auxiliary Carry Flag
- Parity Flag
- Carry Flag

S	Z	X	AC	X	P	X
D_7	D_6	D_5	D_4	D_3	D_2	I

Instruction Register, Decoder, Timing & Control Group

- **Instruction Register –**

✓When an instruction is fetched from memory it is loaded in instruction register.

✓These contents are then provided to decoder for decoding.

Instruction Register, Decoder, Timing & Control Group

- **Instruction Decoder-**

✓It accepts bit pattern from instruction register, decodes it & gives decoded information to control logic.

✓ The information includes

- ➢what operation is to be performed,
- ➢ who is going to perform it,
- ➢how many operand bytes the instruction contains, etc.

Instruction Register, Decoder, Timing & Control Group

- **Timing & Control Unit-**

✓It accepts information from instruction decoder & **generate microsteps** to perform it.

✓This block also accepts clock inputs, performs sequencing & synchronising operation.

Arithmetic & Logical Group

This group consist of **ALU, Accumulator (Reg. A), Temporary register & Flag Register**.

- **ALU** (Arithmetic & Logic Unit)

ALU performs **arithmetic** operations such as **addition, subtraction** & **logical** operations such as **ANDing, ORing & EX-ORing**, etc.

- **Temporary Register**

This register is not available for user. It is only used internally by microprocessor.

Arithmetic & Logical Group

- **Flag Register**

✓It is nothing but a group of flip-flops used to give status of different operations result.

✓It will give status if an operation is performed in ALU.

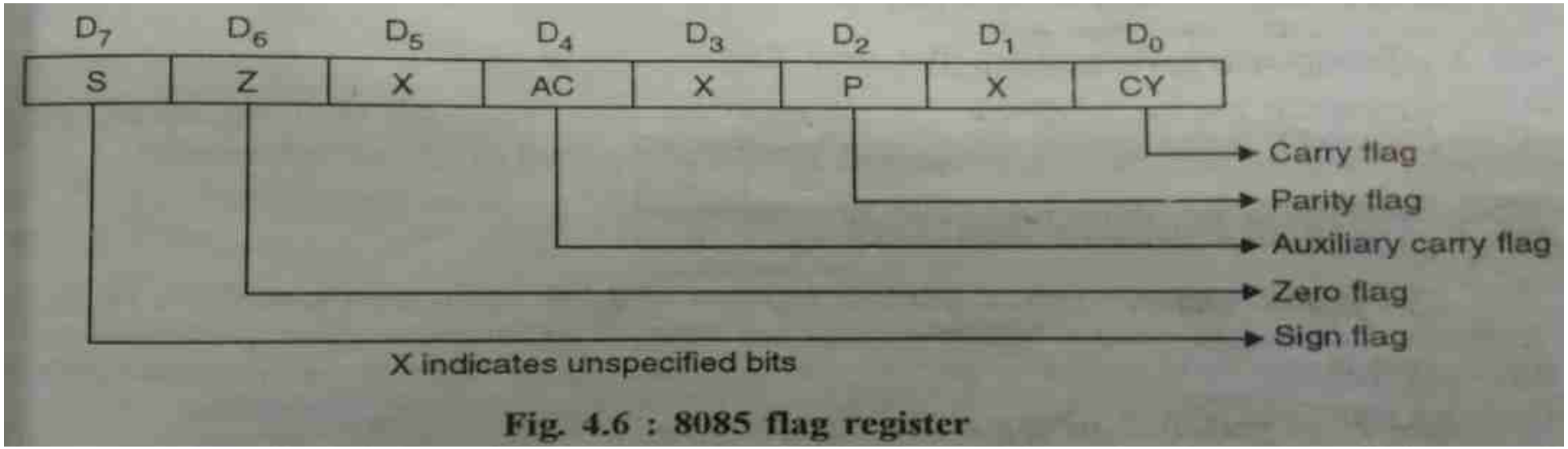


Fig. 4.6 : 8085 flag register

The 8085 Addressing Modes

The various ways of specifying the data to be operated on, are called as **addressing modes**.

Following are addressing modes of 8085

1. Immediate addressing.
2. Register addressing.
3. Direct addressing.
4. Indirect addressing.
5. Implied addressing.

- **Immediate addressing**

  In this mode, data to be used is immediately given in the instruction itself.

  Example: **MVI B, 12H**

- **Register addressing**

  In this mode, data to be operated is in general purpose register.

  Example: **MOV A, B**

- **Direct addressing**

  In this addressing mode the operand is given by direct address where the data is present.

  Example: **LDA C200H**

- **Indirect addressing**

  In this addressing mode the instruction does not have address of the data to be operated on. But instruction points where the address is stored

  Example: **MOV A, M**

- **Implied addressing**

  It does not require any operand.

  Example: **STC, RAL, RAR**

Thank You!