Course	ECE502 VLSI Design	Semester	Monsoon Semester 2024
Faculty Name(s)	Mazad Zaveri	Contact	mazad.zaveri@ahduni.edu.in
School	SEAS	Credits	3
GER Category:	GER, but not one of the above specified Categories	Teaching Pedagogy Enable:NO	P/NP Course: Can not be taken as P/NP

Schedule

Section 1	09:30 am to 11:00 am	Tue	01-08-24 to 26-11-24
	11:00 am to 12:30 pm	Thu	01-08-24 to 26-11-24

Prerequisite	ECE209 Digital Design OR EVD210 Computer Organisation/CSC201 Computer Organisation & CSE2XX Computer Organization and Architecture/CSE206 Computer Organization and Architecture OR Student should have some knowledge of basic electronic/semiconductor devices (Diodes, BJT), and use of tool: LTSpice
Antirequisite	Not Applicable
Corequisite	Not Applicable

Course Description	This is an elective for the BTech CSE/ICT program (can be taken by BS in CS students, if they have the pre-requisite), and an elective for the MTech CSE program. This course will cover: Trends in VLSI industry; MOS Cap; IV characteristics of MOSFET; CMOS inverter and VTC characteristics; CMOS standard and compound gates and transistor sizing; skewed gates, RC delay analysis of CMOS gates; Gate layout and Lambda rules; Logical effort method for delay analysis; power dissipation (dynamic and static power), Pseudo-NMOS gates, pass-transistor gates, dynamic logic circuits – domino gates, etc.
Course Objectives	To learn and understand the basic concepts related to the design and analysis of digital CMOS VLSI circuits and gates
Learning Outcomes	Students will be able to: (1) Undserstand the aspects related to VLSI technology scaling, functioning of MOSFETs, and fundamental concepts related to the design of digital CMOS gates and logic-styles (2) Analyze the operation, performance and power, of digital CMOS logic gates (3) Design, simulate and chatacterize (using schematic editor and spice tool) digital CMOS logic gates (4) Build the layout of digital CMOS logic gates (using EDA tool), by applying lambda based design rules
Pedagogy	Regular lectures, surprise quizzes, and assignments (including simulations and small projects), and exams
Expectation From Students	Regularly attend lectures

Assessment/Evaluation	• End Semester Examination:
	  ◦ End-Sem Exam - 30%
	• Other Components:
	  ◦ Projects/Assignments - 30%
	  ◦ Quiz/Viva/ClassParticipation - 40%

Attendance Policy	As per Ahmedabad University Policy. As per SEAS policy

Project / Assignment Details	Will be declared in class, in due course of time
Course Material	Reference Book • Semiconductor Device Fundamentals, Robert F. Pierret, 1st Edition, Pearson, Year: 2006, • Semiconductor Device Fundamentals, Robert F. Pierret, 1st Edition, Pearson, Year: 2006,
Additional Information	--All Quizzes would be surprise mode, and make-up quizzes would NOT be allowed. --Make-up lectures will NOT be provided. --Make-up mid-term exams (if applicable) would be allowed, in case of only medical leave, which is approved and notified by the appropriate authority / UG Chair of the School of Engineering and Applied Science. (Mode of make-up for the mid-term exam would be decided by the instructor.) --There will be no make-up final exam.

Session Plan

NO.	TOPIC TITLE	TOPIC & SUBTOPIC DETAILS	READINGS,CASES,ETC.	ACTIVITIES	IMPORTANT DATES
1	Introduction to VLSI	Introduction to CMOS VLSI and very basic intro to MOSFET structure	Lecture notes and material given by instructor	Lecture	
2	Introduction to VLSI and Technology Scaling	Trends in VLSI industry and VLSI technolgy scaling; Gate Leakage; Sub-threshold leakage; Solutions: high-k dielectrics, fin based transistors; Power density;	Lecture notes and material given by instructor	Lecture	
3	Introduction to MOSFET	3D view / layout of Inverter; Concepts of metal layers, poly layer, connectivity, contacts; parasitic resistance and capacitance of metal layers, etc Dimensions of interest in planar MOSFET (such as tox, W, L, M1 pitch) and FinFET (such as fin width, fin height, gate-length, fin-extension; fin ptich, gate pitch)	Lecture notes and material given by instructor	Lecture	
4	Introduction to MOSFET and simulation tool	Mask layers for inverter; Concepts related to top-view (layout), and some basic lambda rules for a transistor; Area and Perimeter for Source/Drain; Simulation of IV Characteristics of NMOSFET (Introduction to use of LTspuce tool; Schematic design, Setting the NMOS parameters, and Dual DC Sweep)	Lecture notes and material given by instructor	Lecture and Simulations	
5	MOSFET - Regions of operation	Regions of operation of MOSCAP; Regions of operation of NMOSFET; NMOSFET IV characteriatics; IV equations; Numerical to find Ids;	Lecture notes and material given by instructor	Lecture	
6	MOSFET IV characteristics	Details of ideal IV characteristics of NMOS and PMOS transistors; Numericals and discussions on the variables and constants in IV equations; Comparison of ideal IV shape with simulated IV shape;	Lecture notes and material given by instructor	Lecture	

7	Introduction to digital CMOS gates	Numericals (finding Ids and Vds); Concept of current mirror; Standard unit-sized Inverter and its sizing; Schematic design (topology) of standard CMOS gates (NAND2, NOR2)	Lecture notes and material given by instructor	Lecture	
8	CMOS gates	CMOS compound gates (schematic design and transistor sizing); Introduction to input patterns/transistions (needed for pattern dependent delay analysis)	Lecture notes and material given by instructor	Lecture	
9	Simulation of CMOS gates	Transient simulation of Inverter (in tool LTspice); Use of PWL volage source; Use of .MEAS commands and .PARAM; Characterizarion of: propagation delay (tpdLH and tpdHL), trise, tfall, energy and power;	Lecture notes and material given by instructor	Lecture and Simulations	
10	Simulation of CMOS gates	Simulation of VTC of inverter (DC sweep simulation); Measurement of VOH, VOL, VIH, VIL, Noise Margins, inverter's threshold; Use of .MEAS commands for the same; Introduction to high-skew and low-skew inverters	Lecture notes and material given by instructor	Lecture and Simulations	
11	Simulation of CMOS gates	Simulation of VTC for skewed inverters; Simulation of NAND2 gate; Measurement of Input pattern/transition dependent delay;	Lecture notes and material given by instructor	Lecture and Simulations	
12	Project	Discussion on project/assignment	Material given/discussed by instructor	Discussions on project	
13	Project	Discussion on project-1 (small project, to find the optimal Wp and Wn for a given cascade of inverters); Regions of operations (OFF, LIN, SAT) for NMOS and PMOS within the VTC of inverter	Material given/discussed by instructor	Discussions on project	

14	Other logic styles	Resistive-load NMOS inverter; Pseudo-NMOS inverter; RC modeling (for estimating approximate delay); Nuemrical/example for inverter RC equivalent, and estimating approx delay; Numerical/example for RC equivalent for cascade of gates; Concept of FO4 delay (figure of merit);	Lecture notes and material given by instructor	Lecture	
15	RC delay analysis	Pattern-dependent RC delay Analysis (Example based on RC equivelent model for NAND2 gate); Basic concepts related to understanding layouts, Euler diagram (Arc/vertices and traversal; PMOS and NMOS diffusion strip) (Example: Inverter layout; NAND2 layout)	Lecture notes and material given by instructor	Lecture	
16	Layout of CMOS gates	Layouts of compound gate, cascade of inverters, tri-state inverter; Concepts of: shared S/D areas in the layout; continuity in diffusion strip vs separate transistors	Lecture notes and material given by instructor	Lecture	
17	Layout of CMOS gates	Layout of Compound gate, drawn in Electric VLSI tool; Concepts related to drawing transistor of different sizes (with or without share regions) Checks - Layout vs Schematic (LVS) and DRC (design rule check based on lambda rules)	Lecture notes and material given by instructor	Lecture and Simulations	
18	Layout of CMOS gates	Lambda rules corresping to all layers were covered (Well, Active, Poly, Contacts, Metal) Example of pattern dependent RC delay analysis (for compound gate)	Lecture notes and material given by instructor	Lecture	
19	RC delay analysis	Example of pattern dependent RC delay analysis (for compound gate); Concepts related to Pass-Transistor switch and transmission gate; Design NAND2, NOR2, using pass-transistor logic;	Lecture notes and material given by instructor	Lecture	

20	Project	Discussions on Project-2 (related to creating layout of standard or compound gate in Electric VLSI tool)	Material given/discussed by instructor	Discussions on project	
21	Other logic styles	Pass-Transistor Logic gates (Design of compound gates, based on Shannon's expansion) Introduction to Logical Effort Methodology for delay analysis	Lecture notes and material given by instructor	Lecture	
22	Logical Effort Method of delay analysis	Calculating g (logical effort) and p (parasitic delay) for standard gates, compound gates, and skewed gates;	Lecture notes and material given by instructor	Lecture	
23	Logical Effort Method of delay analysis	Use of Logical effort method for paths with and without branches; transistor/gate sizing;	Lecture notes and material given by instructor	Lecture	
24	Static and Dynamic Power	Concepts related to static and dynamic power dissipation in CMOS gates	Lecture notes and material given by instructor	Lecture	
25	Dynamic Logic Circuits	Concepts related to pre-charge phase and evaluate phase; Problems with cascading of such gates;	Lecture notes and material given by instructor	Lecture	
26	Viva	Viva		Viva	