Compiler Design Notes

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Control Flow Analysis

Why Control Flow Analysis?

Helps to understand structure of Control Flow Graph (CFG), To detect loops in the CFG, Dominator Information,Dominator Frontier Information required for Single Static Assignment (SSA) form. Interval Information used in Data Flow Analysis, Control Dependence Information used in Parallelization.

Dominators

1. We write (d dom n) if every path from initial node n_0 to node n passes through node d. A node dominates itself.
2. Node x strictly dominates node y if x dominates y and $x \neq y$.
3. x is immediate dominator of y if x is closest strict dominator of y.

Algorithm to find Dominators

Let us denote the set of Dominators of node n as $D(n) = OUT(n)$. These sets are very helpful to construct the dominator tree quickly.

- Start with n_0 such that $D(n_0) = \{n_0\}$.
- for each $n \in N - \{n_0\}$ do the following:
  - First set $D(n) = N$.
  - Take intersection of all the outsets of the predecessors of n denoted by $IN(n) = \bigcap_{p \in pred(n)} OUT(p)$.
  - $D(n) = IN(n) \cup \{n\}$.
- Repeat until $D(n)$ stabilizes for all n.

Back Edges and Natural Loops

Back Edges: Edges whose head dominates the tail are called back edges. To find the back edges, one easy way to look if opposing edges according to dominator tree is present in the graph.
Natural Loops: Given a back edge (n, d), the natural loop of the edge is $d \cup$ all the nodes that reach n without going through d. In this case d is the header of the loop and dominates all the nodes in the loop.

Algorithm for finding the natural loop of a back edge

Let the back edge be (n, d). Then initialize a empty stack. Push n into the stack. Initialize a vector with d in it. Then until the stack is empty, pop the top element and push its predecessors into the stack. If the predecessor is not in the vector, add it to the vector. Continue until the stack is empty. The vector now contains the natural loop.

Depth First Numbering of Nodes in a CFG