An Introduction to Microprocessor Architecture using intel 8085 as a classic processor
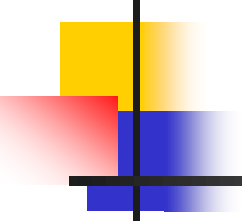
Intel 8085
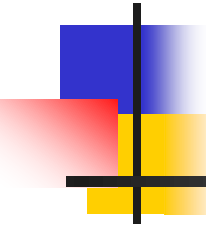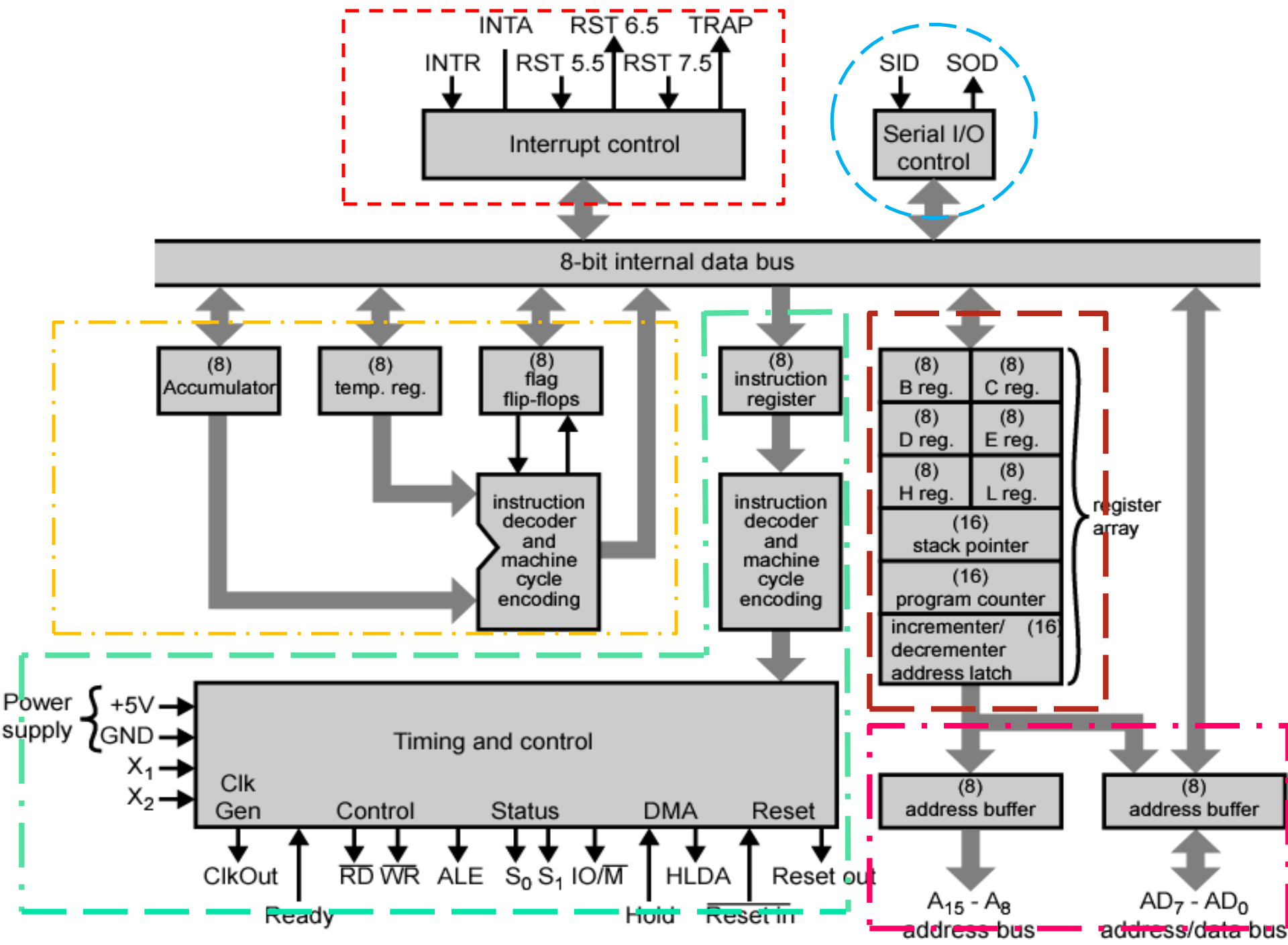
Execution of addition of two numbers in 8085

- ❏ Register group
- ❏ Arithmetic and logical section
- ❏ Instruction register , decoder and control group
- ❏ Address and Address/Data buffers
- ❏ Interrupt control group
- ❏ Serial I/O group.

Register Group

➤ It consists of PIPO registers.

➤ The register contain a set of binary storage cell/filp flop with reading Writing facilities.

➤ It is used for temporary storage of instructions and data/address hence, The number of bits in a register is equal data/address/instruction size

The architecture of 8085 consists of three types of registers.

1. Temporary registers.
2. General purpose register
3. Special purpose register

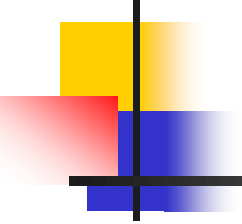# Program Counter- Special purpose register

➢ This 16-bit register deals with sequencing the execution of instructions.

➢ This register is a memory pointer.

➢ The function of the program counter is to point to the memory address from which the next byte is to be fetched.

➢ When a byte is being fetched, the program counter is automatically incremented by one to point to the next memory location

Stack Pointer- Special purpose register

➢ Stack Pointer (SP) The stack pointer is also a 16-bit register, used as a memory pointer.

➢ It points to a memory location in R/W memory, called stack.

➢ The beginning of the stack is defined by loading 16-bit address in the stack pointer.

8-bit Accumulator-Special purpose register

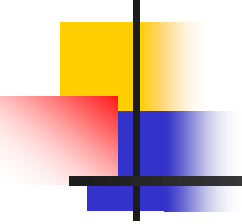➢ It is an 8-bit general purpose register of 8085 but it has some special function that's why is called special purpose register

➢ It has to private one of the operand for any ALU operations.

➢ It has to accumulate the result of ALU operations.

➢ It also works as a via register for I/O accesses i.e. whenever a data is read from input devices , it accumulator and similarly output device gets data from accumulator.

Flag register- Special purpose register

D7	D6	D5	D4	D3	D2	D1	D0
S	Z		AC		P		CY
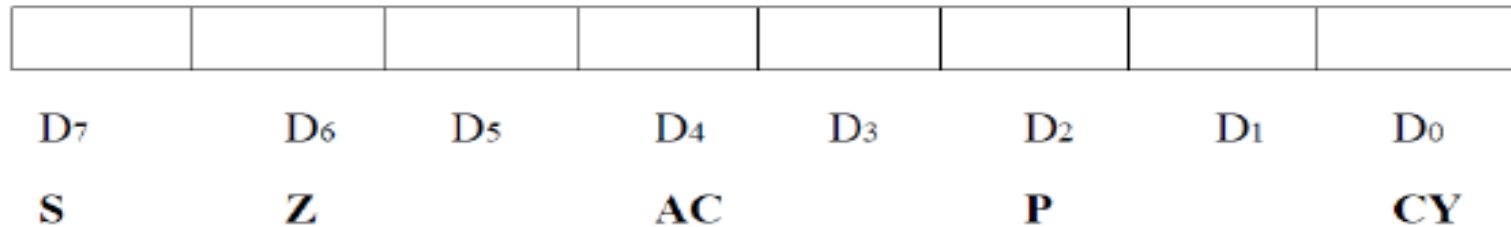
➤ The Flag register of 8085 consists of five flag. They are connected to ALU

➤ When an operation is performed by ALU the result is transferred on internal data bus and status of result will be stored in flip flops.

The Flags register

- There is also a flag register whose bits are affected by the arithmetic & logic operations.
  - S-sign flag
    - The sign flag is set if bit D7 of the accumulator is set after an arithmetic or logic operation.
  - Z-zero flag
    - Set if the result of the ALU operation is 0. Otherwise is reset. This flag is affected by operations on the accumulator as well as other registers. (DCR B).
  - AC-Auxiliary Carry
    - This flag is set when a carry is generated from bit D3 and passed to D4 . This flag is used only internally for BCD operations.
  - P-Parity flag
    - After an ALU operation, if the result has an even # of 1s, the p-flag is set. Otherwise it is cleared. So, the flag can be used to indicate even parity.
  - CY-carry flag
    - This flag is set when a carry is generated from bit D7 after an unsigned operation.
  - OV-Overflow flag
    - This flag is set when an overflow occurs after a signed operation.

Instruction register- Special purpose register

➢ This register is not accessible to the user.
➢ It is not programmable and can not be accessed through an Instruction
➢ It is part of the ALU

Address Buffer , Address/Data Buffer and Increment/Decrement

Address Buffer:

➢ This is 8-bit unidirectional buffer used for address lines.

➢ These are used to drive the higher order address bus

Address/Data Buffer:

➢ This is 8-bit bidirectional buffer used for address and data lines.

➢ These are used to drive the lower order address and data bus

Increment/Decrement register:

➢ This is 16 bit register

➢ It is used to increment or decrement address.

ALU:

➢ It perform arithmetic and logical operations
➢ It include accumulator ,temporary register and five flag registers.
➢ The ALU is not available to the user.
➢ Its ward length depends upon the width of an internal data bus i.e. 8-bit
➢ The ALU is always controlled by timing and control circuits.
➢ It accepts operand from accumulator and temporary register.
➢ It stores results of arithmetic and logic operation in accumulator.
➢ It provide status of result to flag register

Timing and Control section

➤ It is made up of synchronous sequential logic circuit.
➤ It control all internal and external circuits in the microprocessor
➤ It operate with reference to clock signal
➤ It accept information from instruction decoder and generate micro steps to perform it.
➤ The control unit also generates timing signals essential for microprocessor to operate.

Interrupt section

➢ It is a mechanism by which an I/O device or an instruction can suspend the normal execution of the processor and get itself serviced is called Interrupt.

➢ This block accepts different interrupt request inputs such as TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR

➢ INTA is an acknowledge pin for mask able and non- mask able interrupt request.

Serial I/O control group:

➢ This data transferred on to data bus is parallel data , but under certain condition it is advantage to use serial data transfer.

➢ 8085 implements by SID and SOD signals.

➢ SID line is used to received the data serially and SOD line is used to send data serially.

➢ The data on these line is accepted or transferred under software control