Indian Institute of Technology Kharagpur

AUTUMN Semester, 2019
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Assignment-7: Verilog Design of Barrel Shifter and Multiple-of-three Detector

Full Marks: 20

Time allowed: 3 hours

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your Verilog source code files(s) and Verilog testbench(es). Name your submitted zipped folder as `Assgn_8_Grp_<Group_no>.zip` and (e.g. `Assgn_8__Grp_25.zip`). Inside each submitted source and testbench files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. Liberally comment your code to improve its comprehensibility.

1. [**Bidirectional Barrel Shifter**] Design (using Verilog), simulate (using an appropriate Verilog testbench) and implement an 8-bit *Bidirectional Barrel Shifter* circuit. The interface of your circuit should be the following:
   `module barrel_shifter (input [7:0] in, input [2:0] shamt, input dir, output [7:0] out)`,
   where `dir = 1` for left shifts and `dir = 0` for right shifts. (10 marks)

2. [**Multiple-of-three Detector FSM**] Design (using Verilog), simulate (using an appropriate Verilog testbench) and implement a simple finite state machine (FSM) that in every clock cycle reads an input bit, and outputs a bit which indicates whether the binary number read till that point, including the most recently read bit (the number is considered to be read from the MSB side), is divisible by three. The input number is to be considered an unsigned integer. The FSM has one input control signals which resets it to the initial state, and this signal is applied at the start of operations. (10 marks)