Indian Institute of Technology Kharagpur

AUTUMN Semester, 2019
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Assignment-8: Verilog Design of Sequential Multipliers

Full Marks: 20

Time allowed: 6 hours

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your Verilog source code files(s) and Verilog testbench(es). Name your submitted zipped folder as `Assgn_8_Grp_<Group_no>.zip` and (e.g. `Assgn_8__Grp_25.zip`). Inside each submitted source and testbench files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. Liberally comment your code to improve its comprehensibility.

1. [**Sequential Unsigned Binary Multiplier (left-shift version)**] Consider the iterative multiplication of two n-bit unsigned integers, $X = \sum_{j=0}^{n-1} x_j 2^j$ and $Y = \sum_{j=0}^{n-1} y_j 2^j$, to form the $2n$-bit product $P = X \cdot Y$. Multiplication proceeds by calculating the partial products (associated with corresponding right-shifts) as: $P_{i+1} = P_i + x_j 2^i Y$ for each bit x_j of the multiplier, with $P_0 = 0$ and $P_n = P$. Design (using Verilog), simulate (using a proper Verilog testbench), and implement on FPGA an **6-bit sequential unsigned binary multiplier** following the above scheme. The input-side operand registers used in the datpath of your multiplier should have "parallel load" capabilities such that the 6-bit operands can be loaded in each of them instantaneously. The interface of your design should be:
`module unsigned_seq_mult_LS (input clk, input rst, input load, input [5:0] a, input [5:0] b, output reg [11:0] product);`, where the signal names suggest their functionality. (5 marks)

2. [**Sequential Unsigned Binary Multiplier (right-shift version)**] Now, design, simulate, and implement on FPGA the above multiplier using an alternative scheme that considers right-shifting of the partial products:
$$P_i = P_i + x_j Y \quad \text{and} \quad P_{i+1} = 2^{-1} P_i$$
The interface should be `module unsigned_seq_mult_RS (input clk, input rst, input load, input [5:0] a, input [5:0] b, output reg [11:0] product);`.
Other details remain the same. (5 marks)

3. [**Sequential Signed Binary Multiplier (Booth Multiplier)**] Design (using Verilog), simulate and implement on FPGA a circuit for multiplication of two 6-bit two's complement integers, using the *Booth Multiplication Algorithm*. Write a testbench to simulate it, and demonstrate its operation on the FPGA. The input-side operand registers used in the datpath of your multiplier should have "parallel load" capabilities such that the 6-bit operands can be loaded in each of them instantaneously. Come up with a proper interface for your design. (10 marks)