DESIGN A OP-AMP IN 180NM CMOS TECHNOLOGY

- Introduction :- operational amplifier is an versatile and essential component in analog electronics. It is an integrated circuit that can amplify weak electric signals or dc – coupled high gain electronic voltage amplifier with differential inputs (inverting and non-inverting) and single ended outputs. It's input impedance is very high and output impedance is low.

➢ Op-amps are used in various configuration such as integrator, differentiator, and summing amplifier.

Given Specification :

- Gain — 40 V/V
- Gain-Bandwidth (UGB) — 2 GHz
- Band-Width (BW) — 50 MHz
- Load Capacitance (CL) — 100 fF
- Phase Margin — >=90deg
- Vout (dc) — 1 V

Design process :-

Step 1 :

- Assume ,
- Length (L) = 360nm , Gm/Id = 15 ,
- BW = 1/[2*pi*CL*Rout]
- Rout = 1/[2*3.14*100*10^-15*50*10^6]
- Rout = 31.85 Kohm ,

Step 2 :

- Gain = Gm*Rout

- Gm = Gain/Rout ,
- Gm = 40/31.85*10^3
- Gm = 1.256 mS ,
- Gm/Id = 15
- Id = 1.256*10^-3/15
- Id = 83.7 uA ,
- Graph between Vgs and Gm/Id from ADT (Analog Designer Toolbox)
- Vgs = 585.5 mV
- Graph between Id/W and Gm/Id from ADT

- Id/W = 5.275
- W(1,2) = 15.87 um ,

Step 3 :

- Graph Between Id/Gds1 and Gm/Id from ADT
- Id/Gds1 = 5.072
- Gds1 = 16.5u
- ro1 = 1/Gds1
- ro1 = 60.6 Kohm
- Rout = ro1 || ro3

- ro3 = Rout/[1-Rout/ro1]
- ro3 = 67.13 Kohm ,
- Gds3 = 1/ro3
- Gds3 = 14.89u
- Ratio , Id/Gds3 = 5.62
- Graph Between Gm3/Id and Id/Gds3 from ADT
- Gm3/Id = 12.52
- Graph Between Gm3/Id and Id/W from ADT
- Id/W = 2.398

- W(3,4) = 34.9 um ,

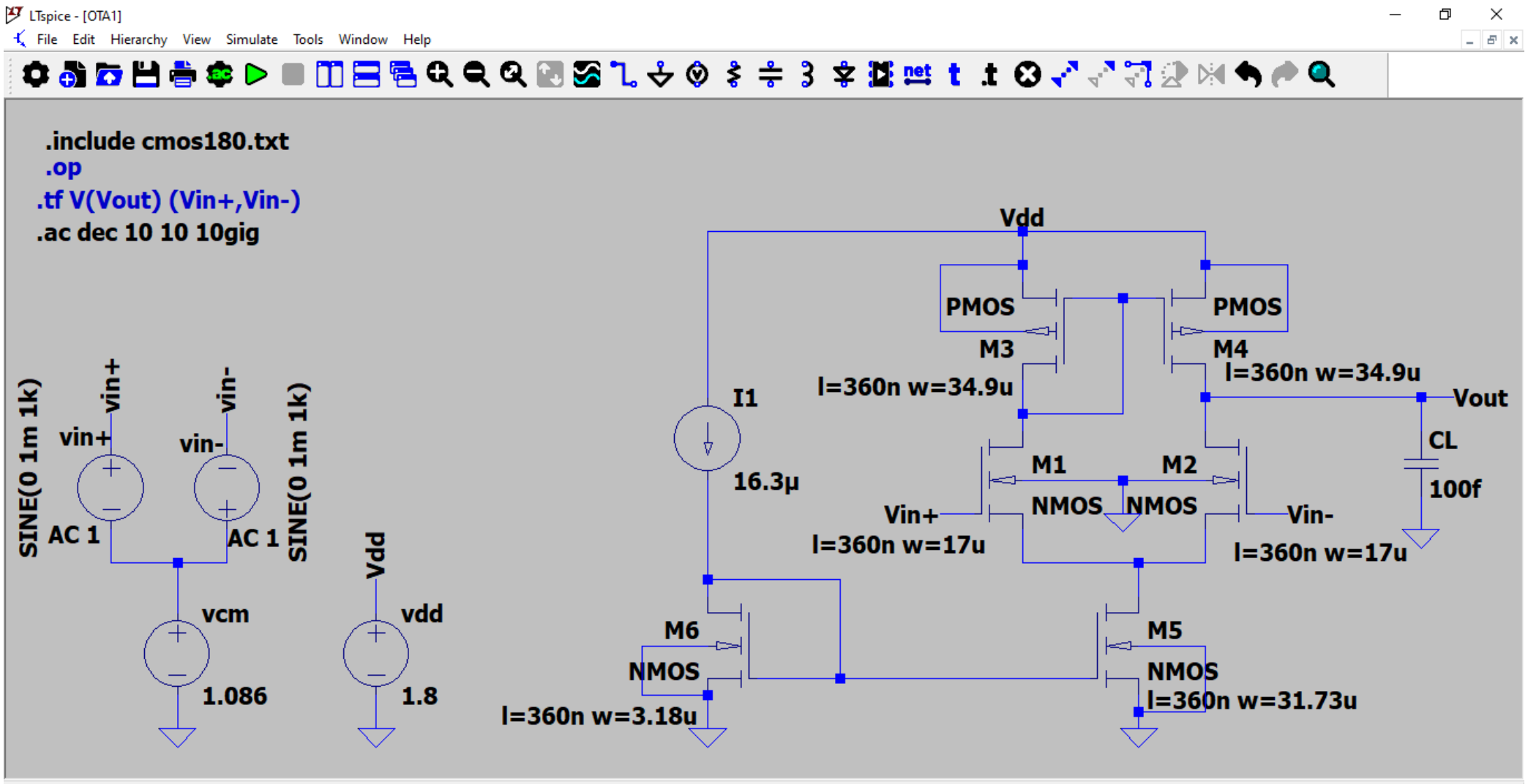
Step 4 :

- Iss = 2* Id
- Iss = 167.4 uA
- Assume , Gm/Iss = 15
- Graph Between Gm/Iss and Vgs(5) from ADT
- Vgs(5) = 585.5mV
- Graph Between Gm/Iss and Iss/W from ADT
- Iss/W = 5.275
- W(5) = 31.73 um

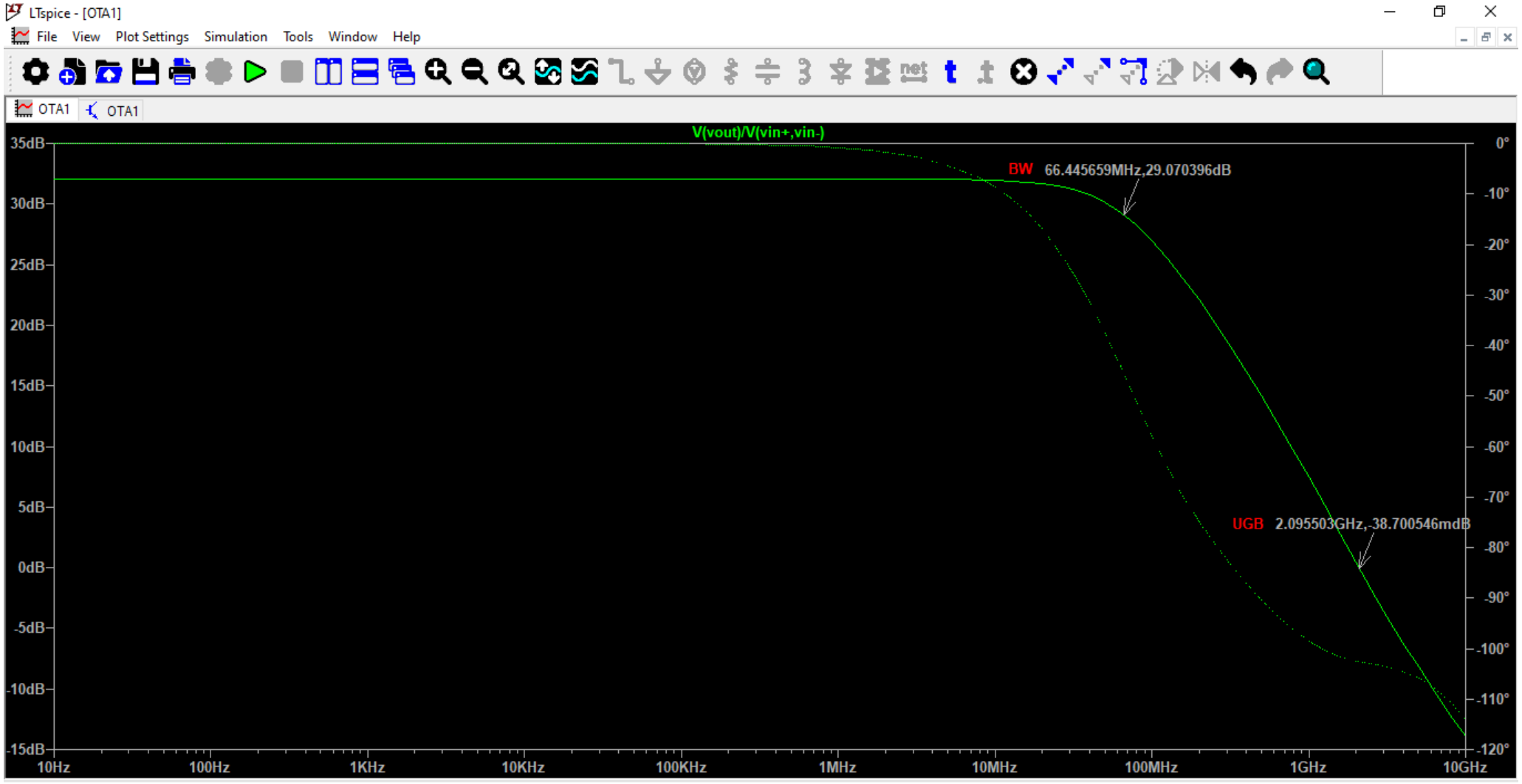
Step 5 :

- Current mirror in transistor M6 ,
- I = Iss/10
- I = 16.3 uA
- W(6) = W(5)/10
- W(6) = 3.18 um

➢ Schematic of single stage operational Amplifier.



➢ Ac Analysis of single stage operational Amplifier



➢ Transient Analysis of Single Stage Op-Amp

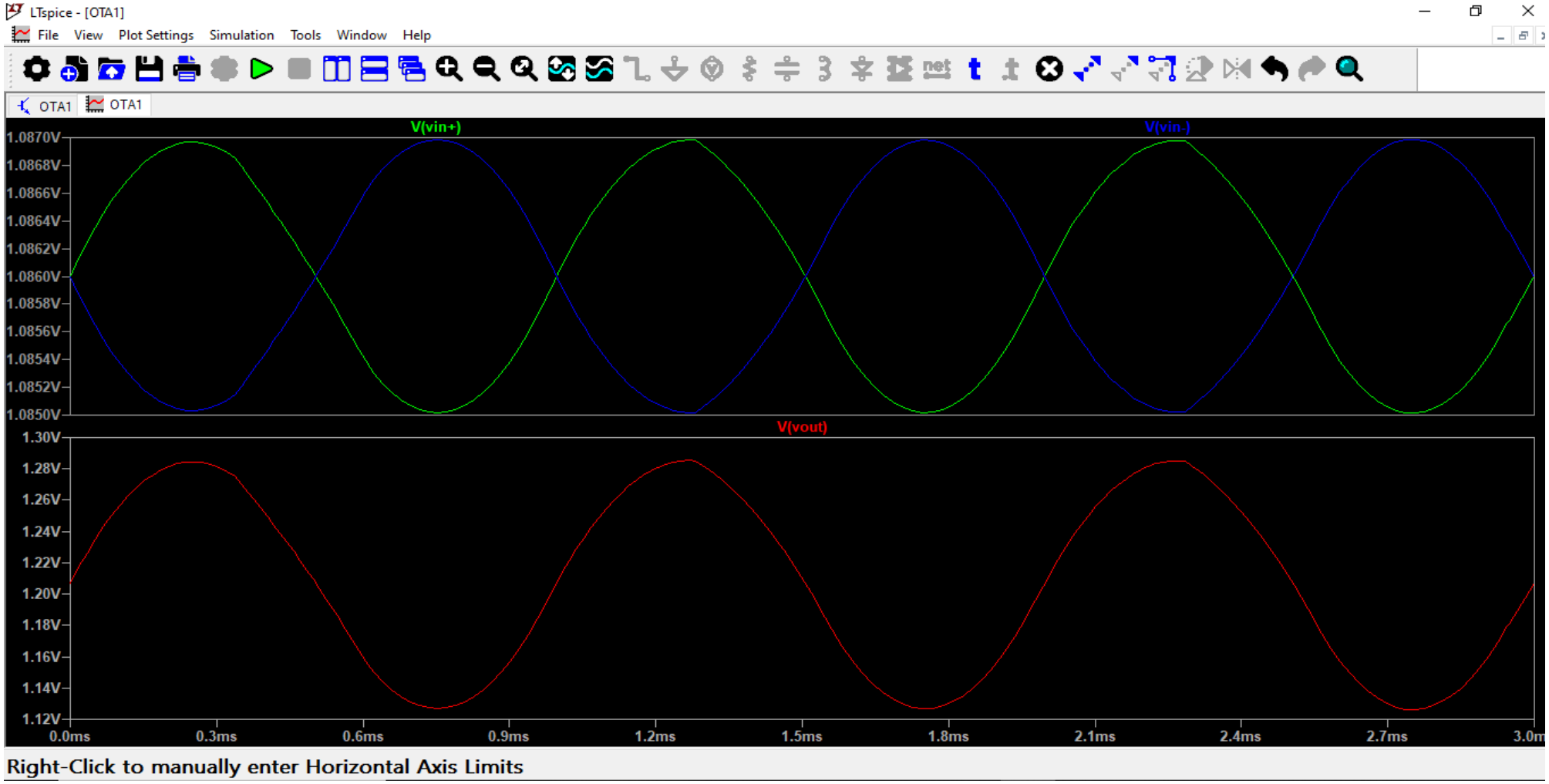


TABLE 1: TRANSISTOR SIZES

Device	Length(L)	Width(W)	W/L
NM1	360nm	17um	47.2
NM2	360nm	17um	47.2
NM5	360nm	31.7um	88.0
NM6	360nm	3.18um	8.8
PM1	360nm	34.9um	96.9
PM2	360nm	34.9um	96.9

TABLE 2: RESULTS

Specs	Given	Achieved
Dc gain	40 V/V	40.45 V/V
Band-width (BW)	50 MHz	66.4 MHz
Gain-Bandwidth (UGB)	2 GHz	2.09 GHz
Vout (Dc)	1 V	1.2 V
Power Dissipation (Pd)	Unspecified	307.2 uW
Load Capacitance (CL)	100 fF	100 fF
Current (Iss)	Unspecified	170.6 uA
Phase Margin (PM)	>= 90 deg	107 deg