Lab 10

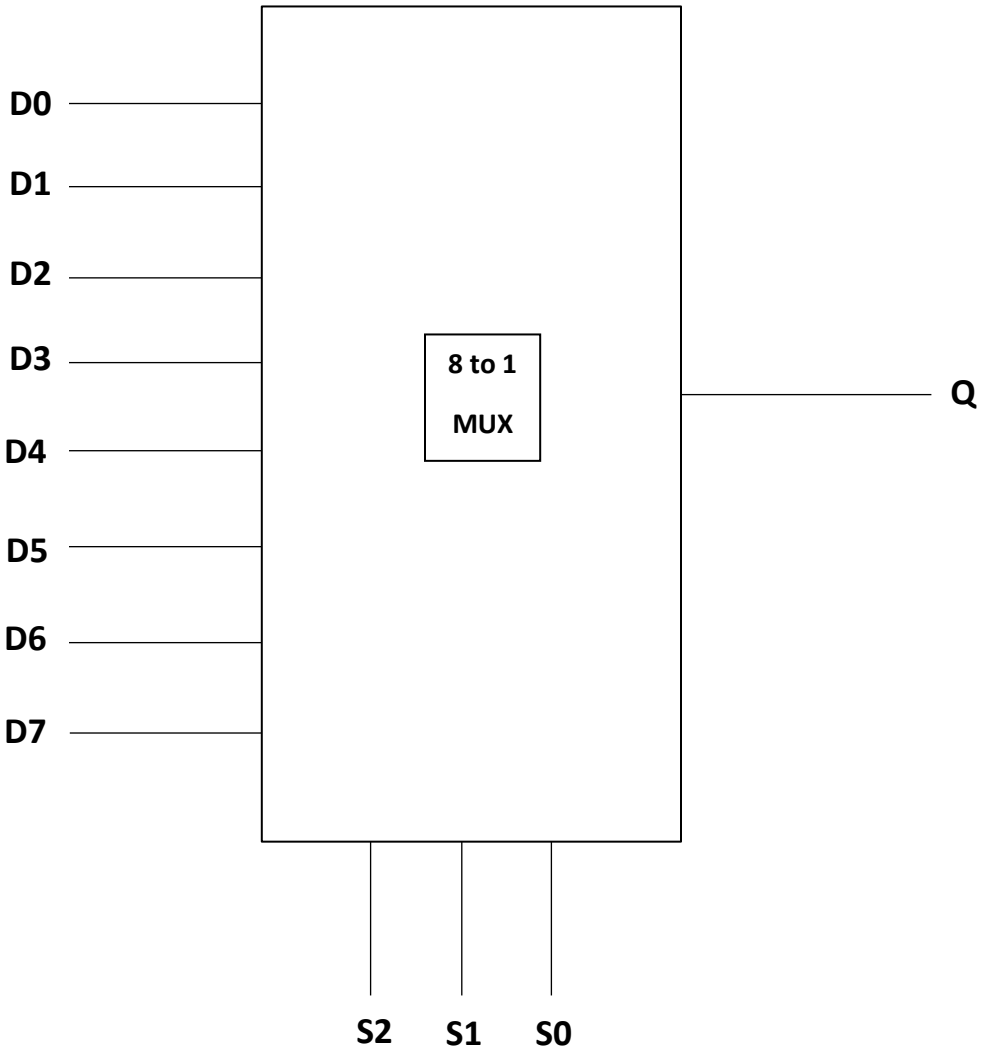
To Design and Implement Multiplexer & Demultiplexer

Tasks

1. **Construct a logic circuit for 8 to 1 multiplexer with the help of truth table. Also write the Boolean expression for output(s). Simulate your circuit to verify the outputs.**

8 to 1 Mux

a) Block Diagram



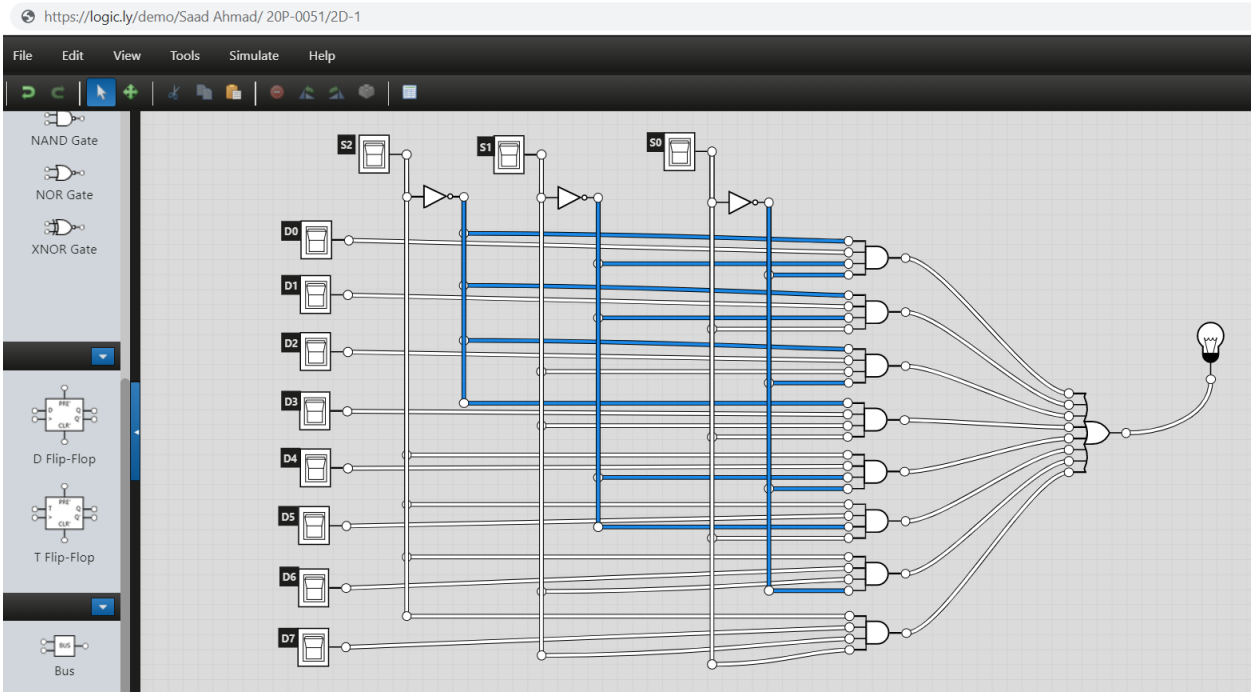
b) Truth Table

S2	S1	S1	Q
0	**0**	**0**	**D0**
0	**0**	**1**	**D1**
0	**1**	**0**	**D2**
0	**1**	**1**	**D3**
1	**0**	**0**	**D4**
1	**0**	**1**	**D5**
1	**1**	**0**	**D6**
1	**1**	**1**	**D7**

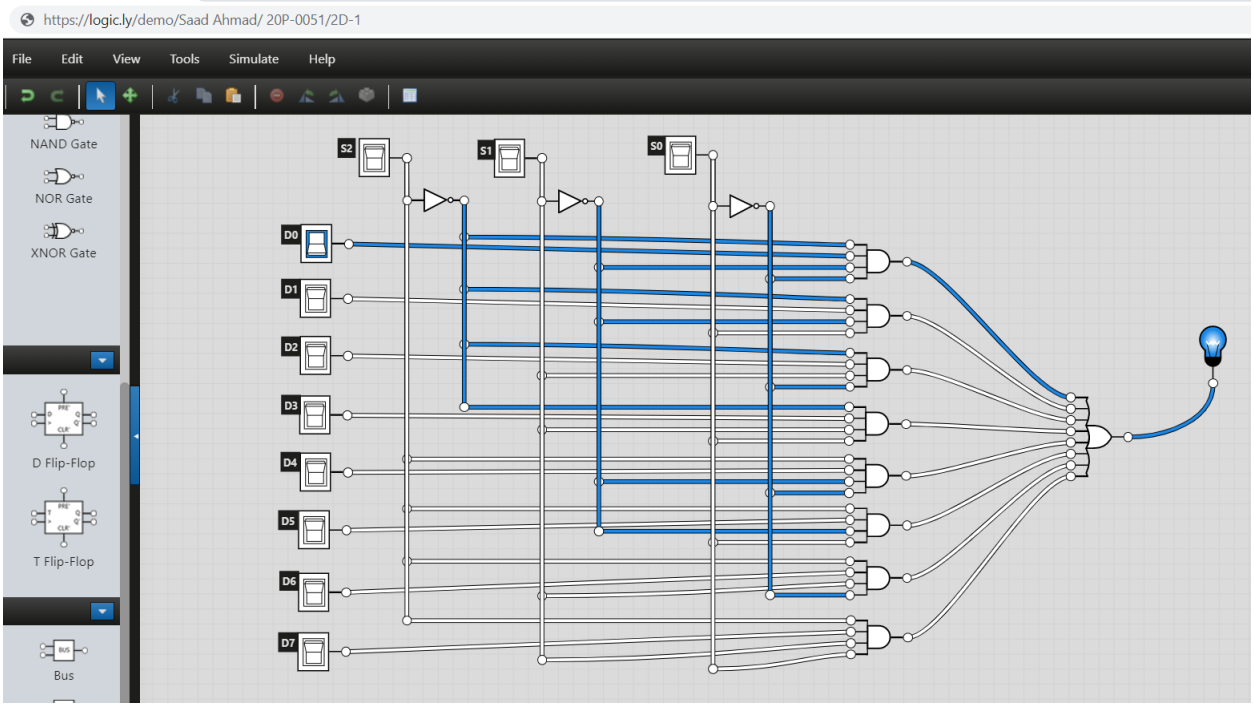
c) Boolean Expression

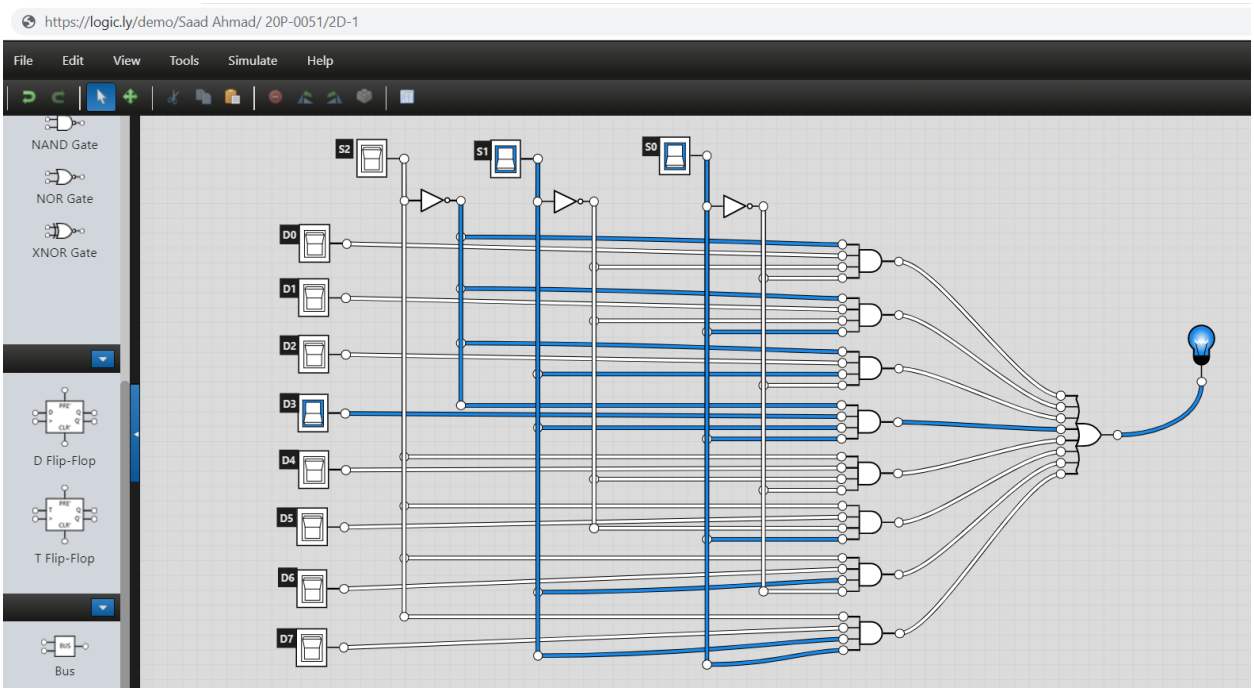
Q = S2’.S1’.S0’.D0 + S2’.S1’.S0.D1 + S2’.S1.S0’.D2 + S2’.S1.S0.D3 + S2.S1’.S0’.D4 + S2.S1’.S0.D5 + S2.S1.S0’.D6 + S2.S1.S0.D7

d) Logic Diagram (from logicaly or hand drawn)



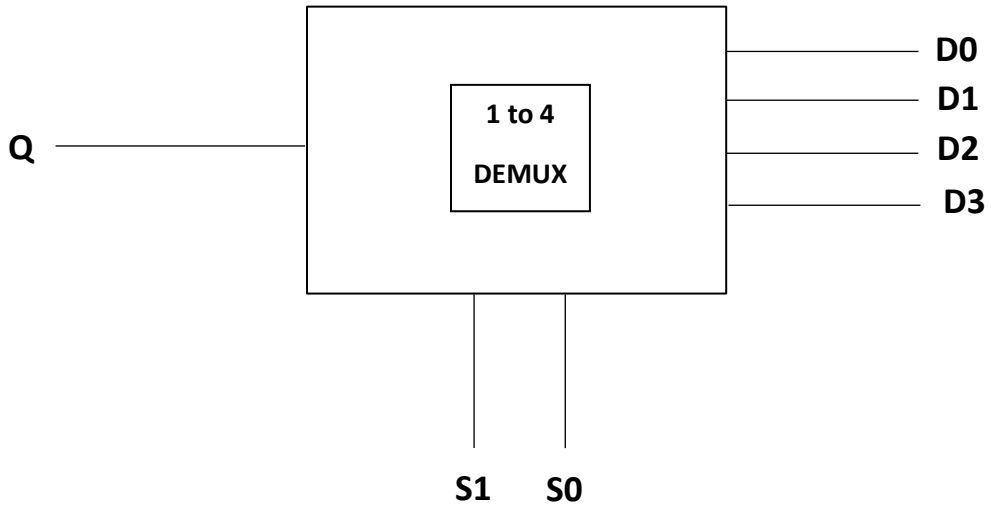
e) Software Simulation





2. **Design a logic circuit for 1-to-4-line Demultiplexer. Also write the Boolean expression for output(s). Simulate your circuit to verify the outputs.**

a) Block Diagram



b) Truth Table

S1	S0	Q
0	0	D0
0	1	D1
1	0	D2
1	1	D3

c) Boolean Expression

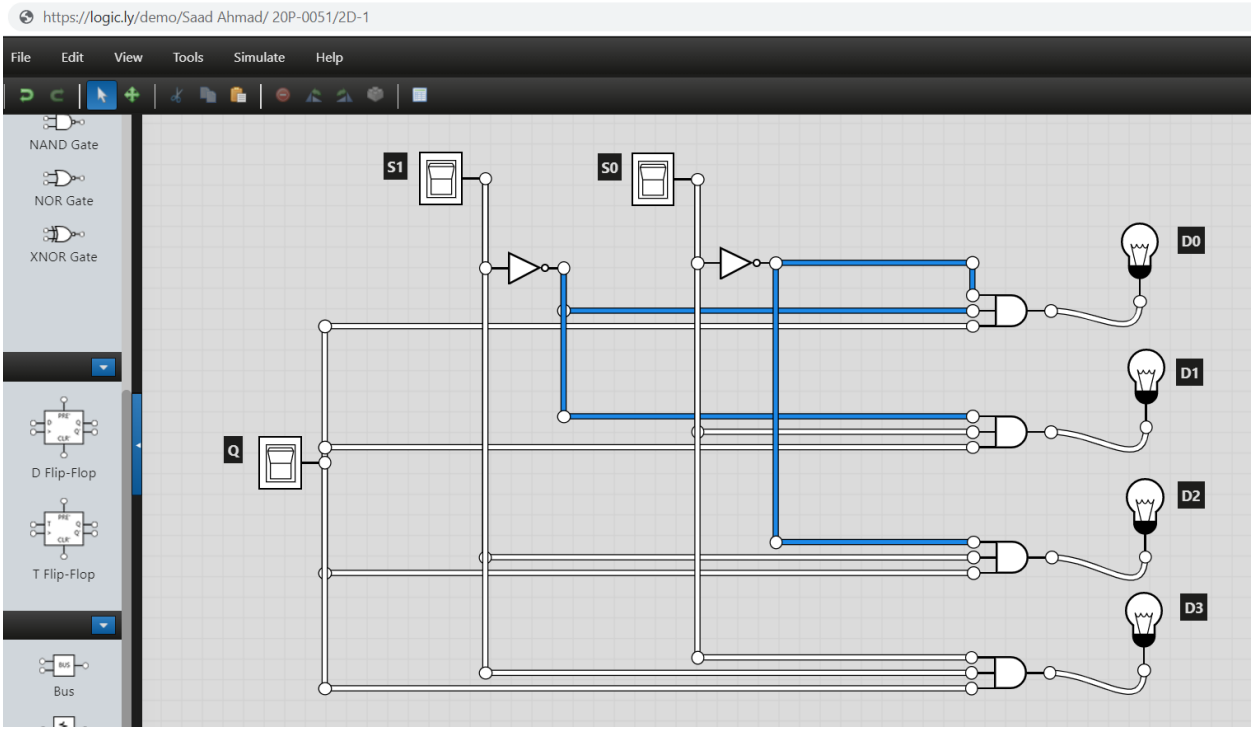
D0 = S1'. S0'. Q

D1 = S1'. S0. Q

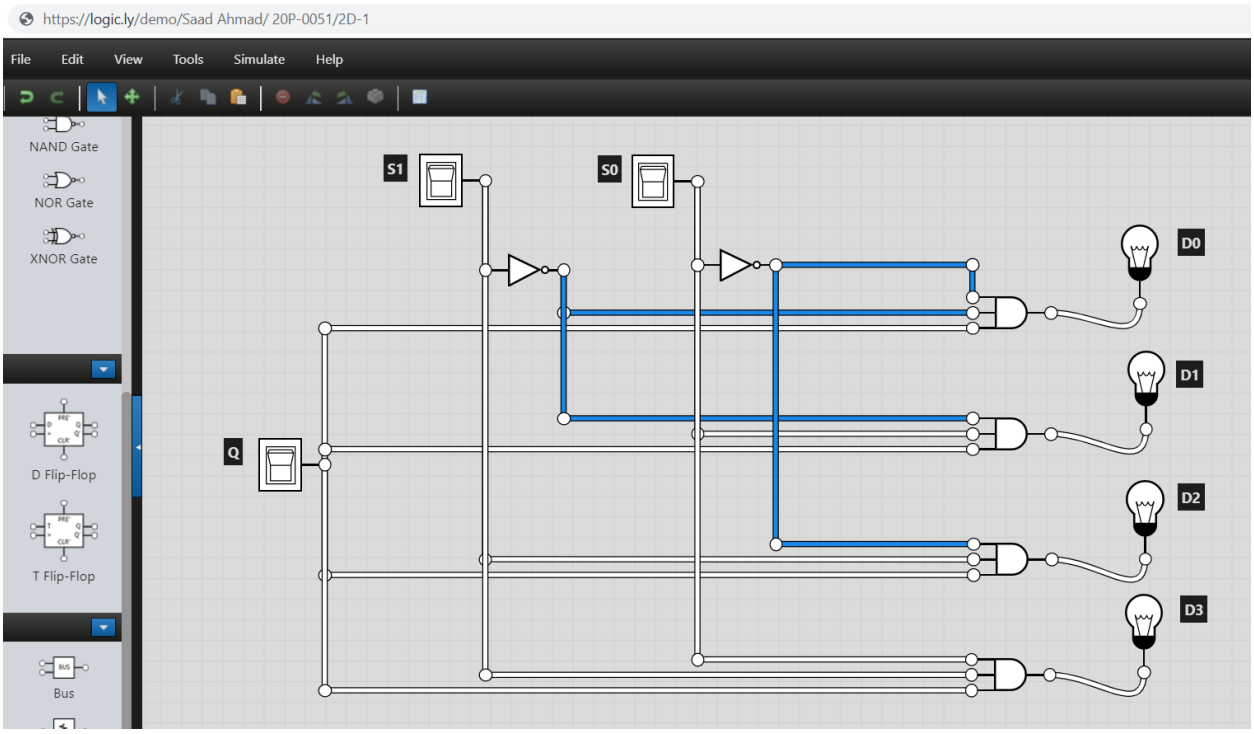
D2 = S1. S0'. Q

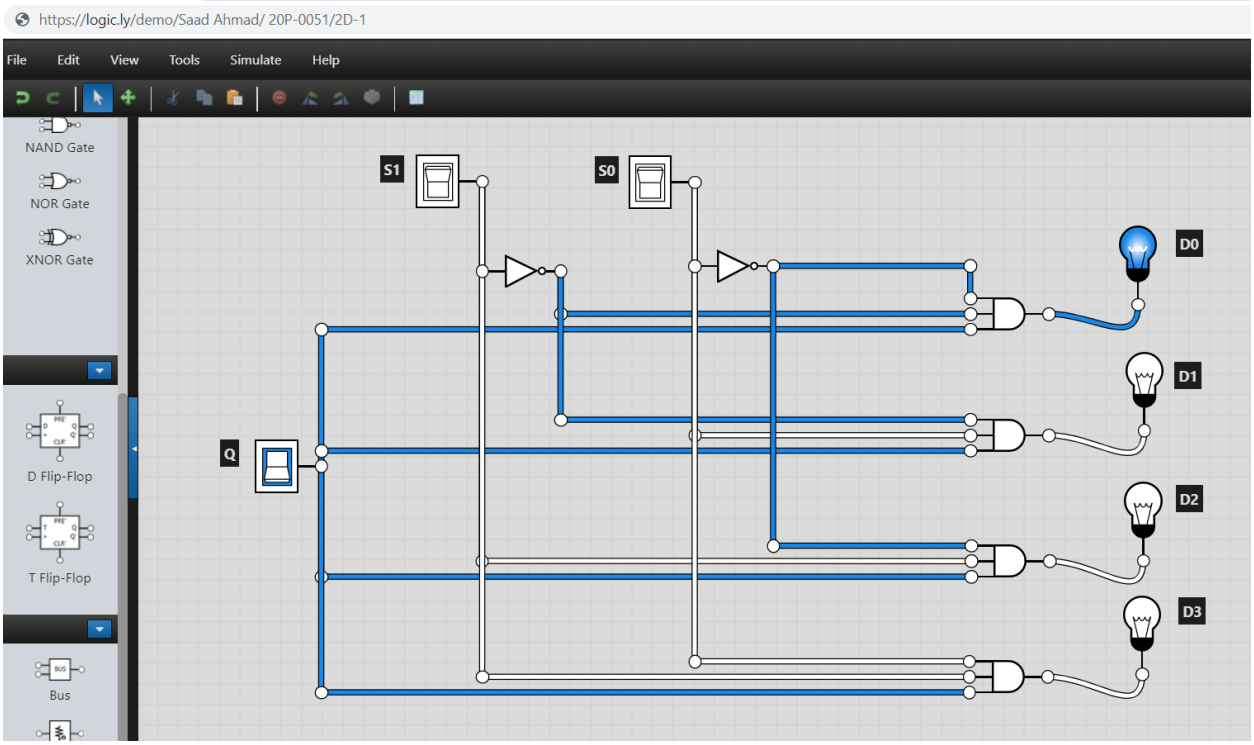
D3 = S1. S0. Q

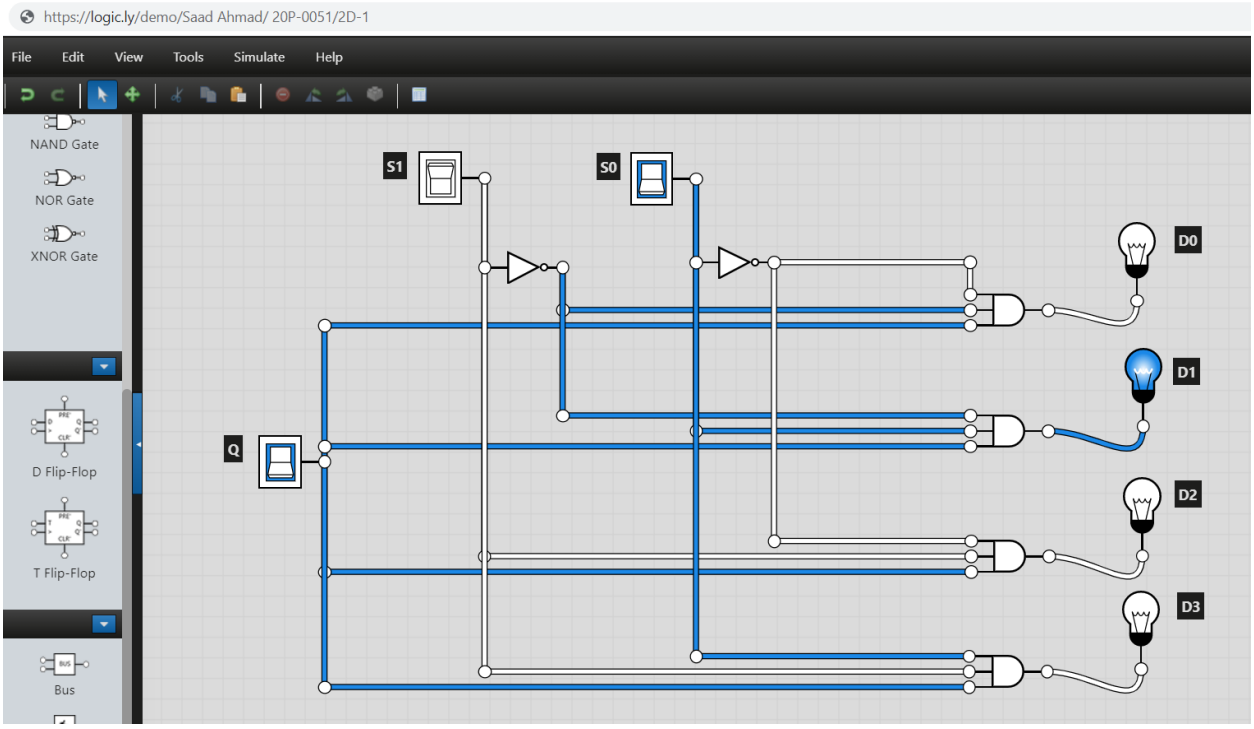
d) Logic Diagram



e) Software Simulation




https://logic.ly/demo/Saad Ahmad/ 20P-0051/2D-1
File
Edit
View
Tools
Simulate
Help
NAND Gate
NOR Gate
XNOR Gate
D Flip-Flop
T Flip-Flop
Bus
S1
S0
Q
D0
D1
D2
D3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S1
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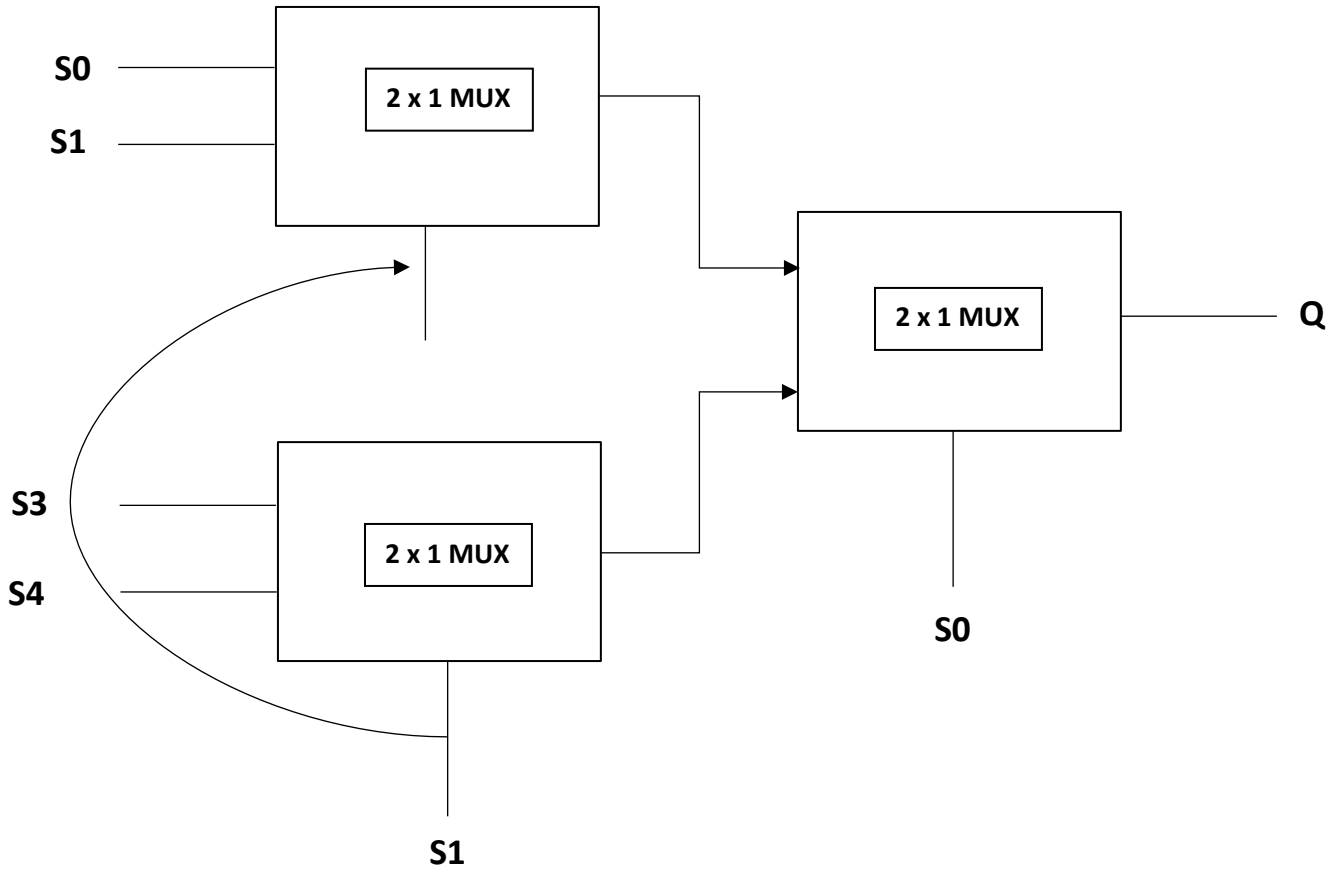
Q
D0
D1
D2
D3

3. **Design a circuit for 4 to 1 Multiplexer using 2 to 1 Multiplexer(s). You can take help from google or the link below. Just ignore the coding language discussed in the link.**
https://bravelearn.com/design-of-4x2-multiplexer-using-2x1-mux-in-verilog/

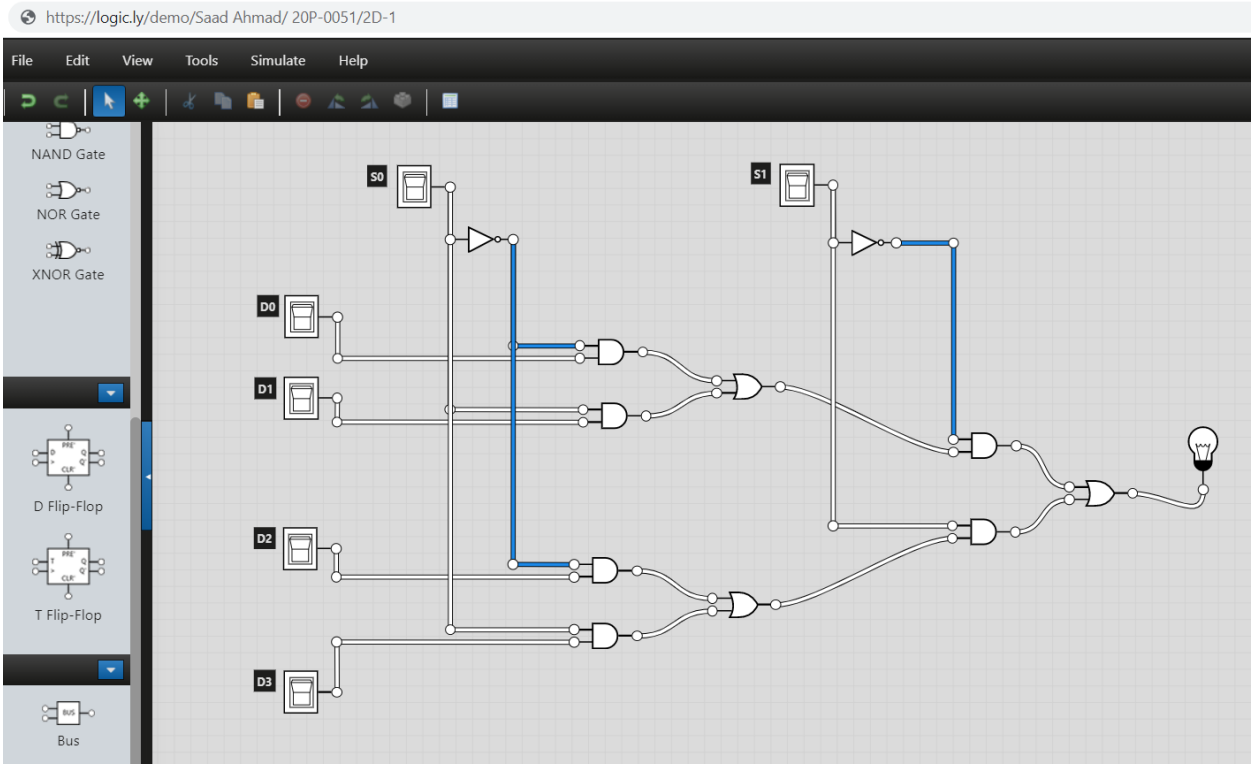
a) Block Diagram

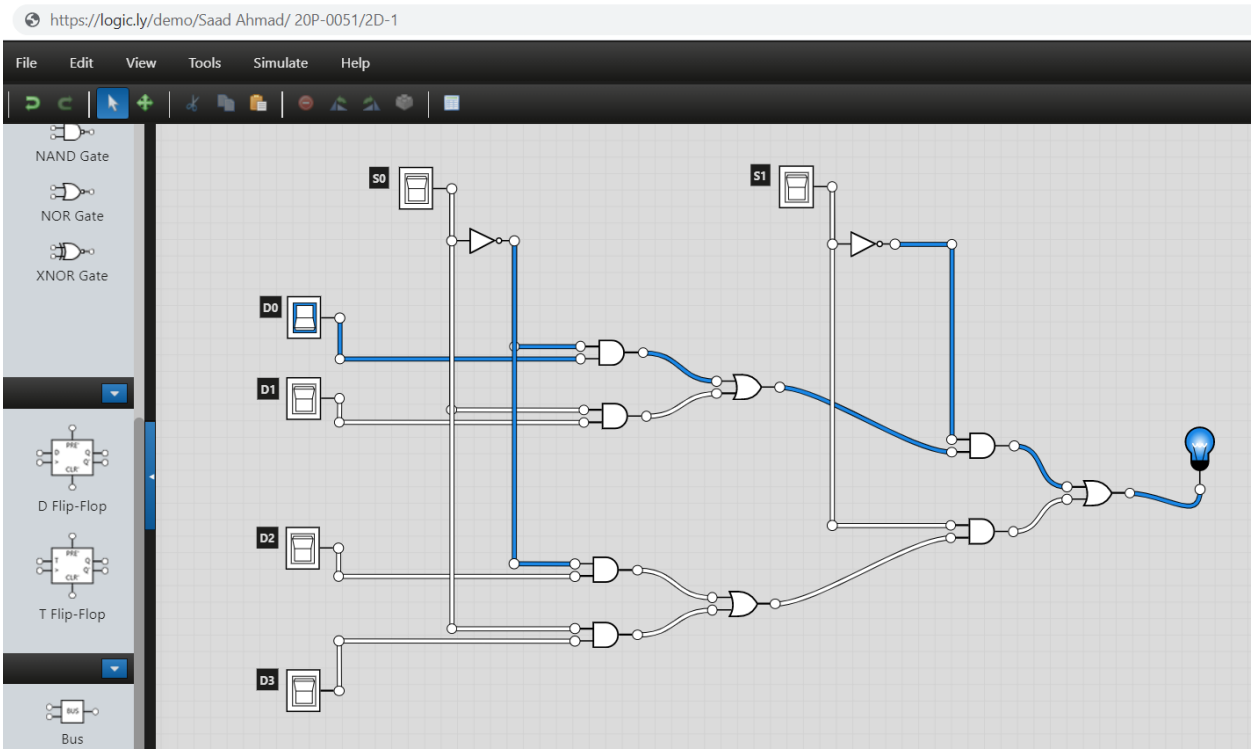


b) Truth Table

S1	S0	Q
0	0	D0
0	1	D1
1	0	D2
1	1	D3

c) Logic Circuit (on the basis of 2 to 1 Muxes used/follow the block diagram to draw this circuit)
*You need to connect three **2 x1 Multiplexers** in order to make one **4x1 Multiplexer**.*

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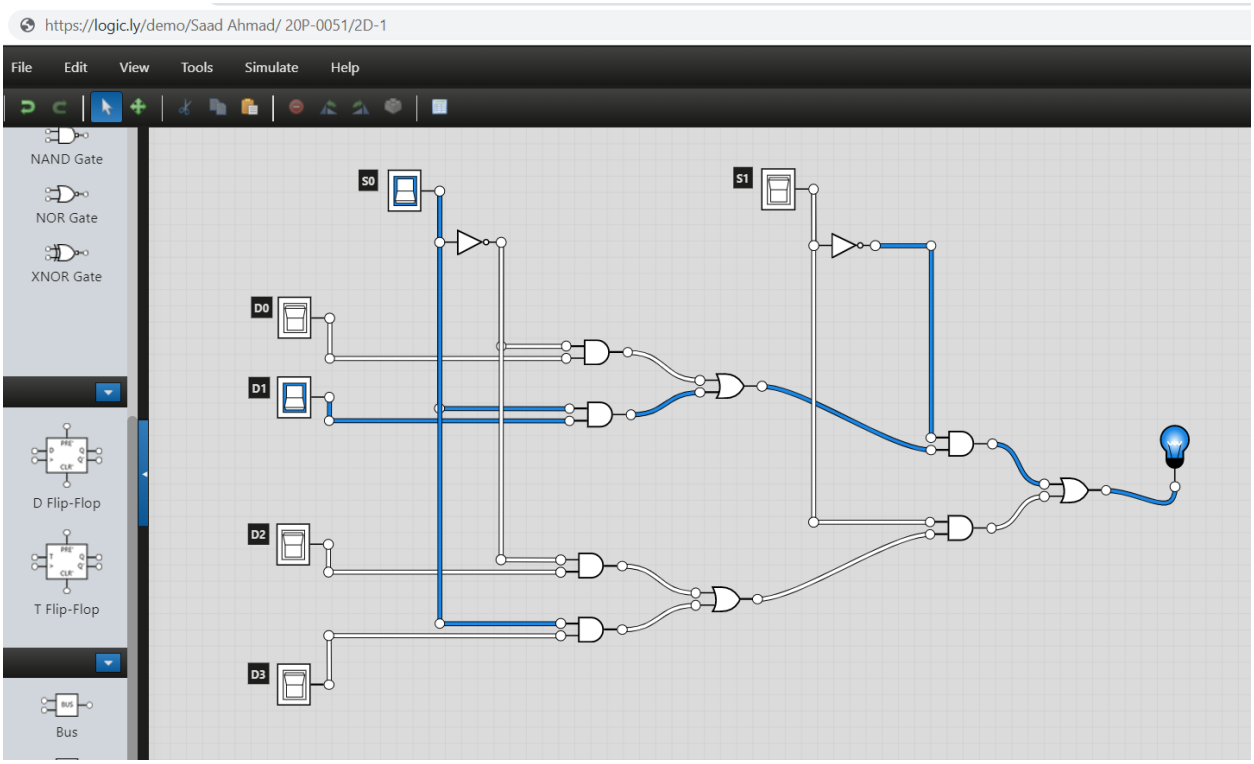
S0
S1
D0
D1
D2
D3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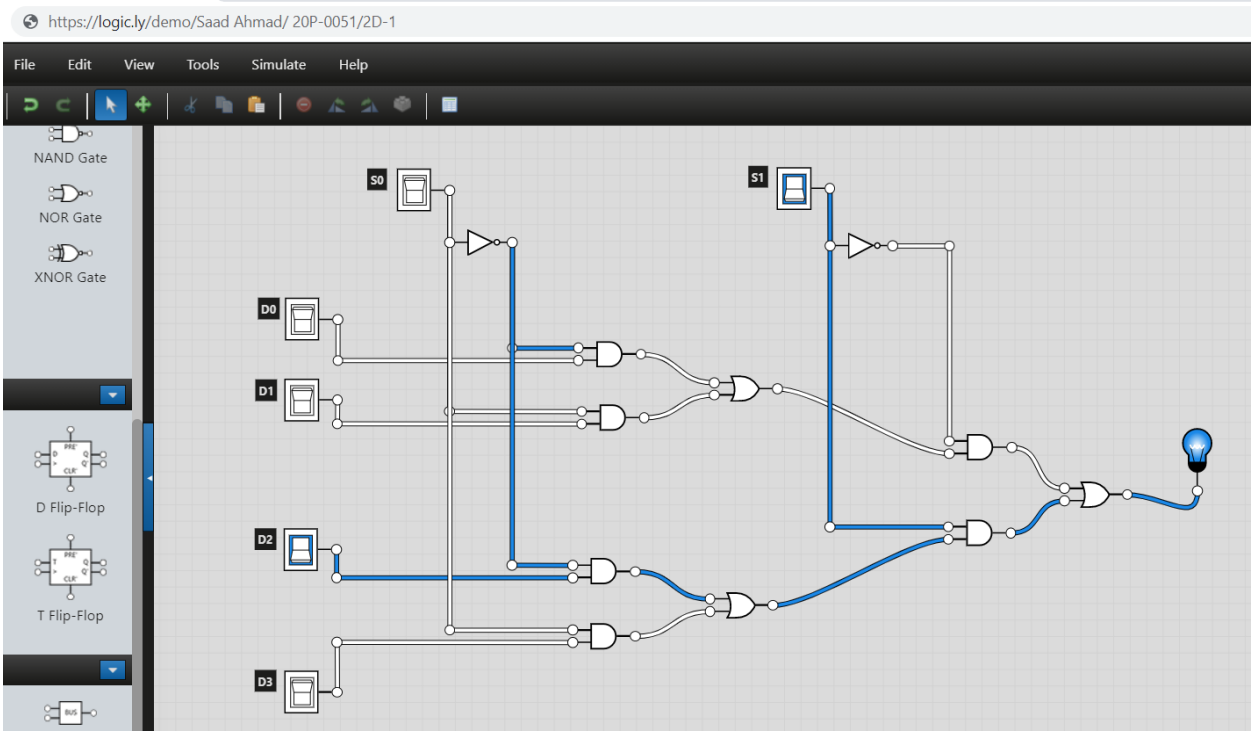
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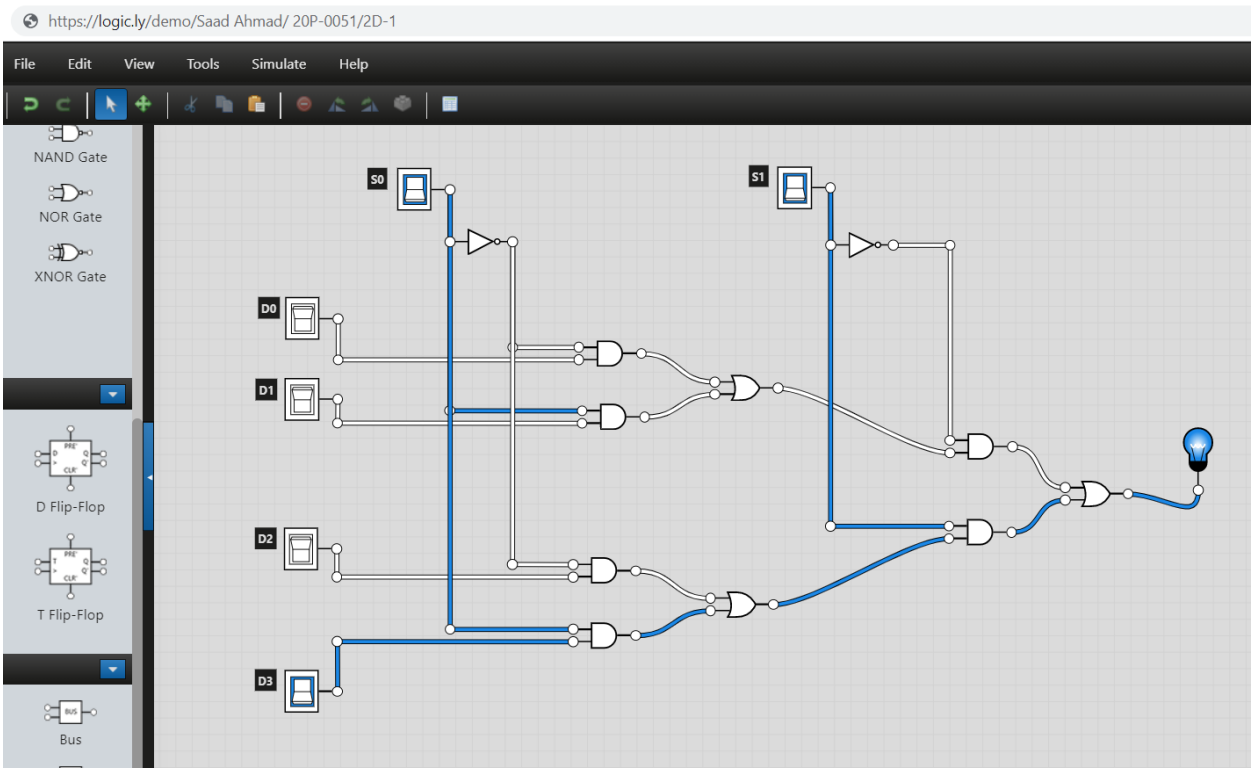
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