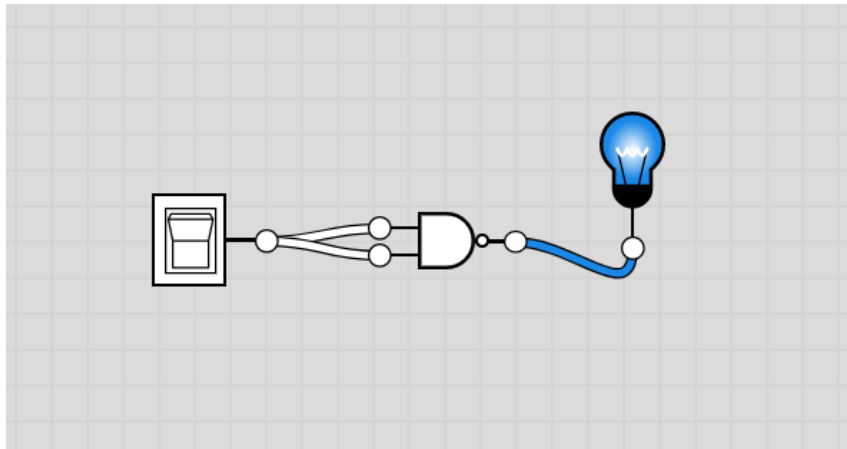


## Using NAND Gate to make other logic gates:

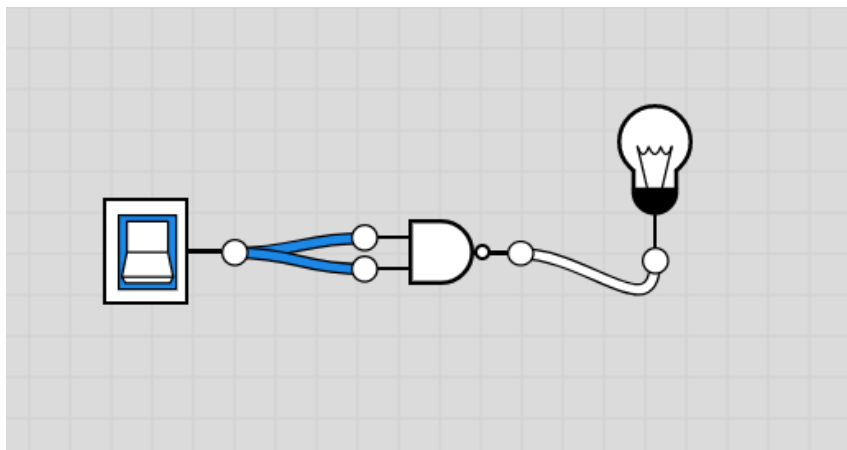
### NOT Gate:

#### Combination#1



Input	Output
0	1

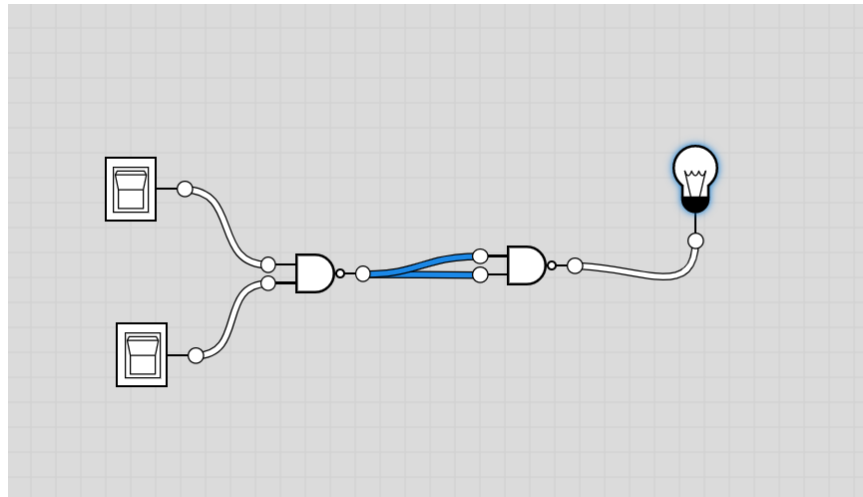
#### Combination#2



Input	Output
1	0

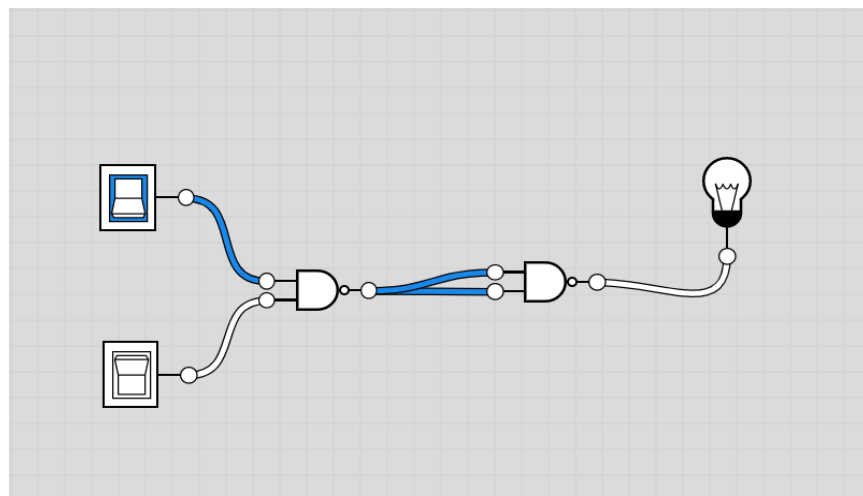
## AND Gate:

### Combination#1



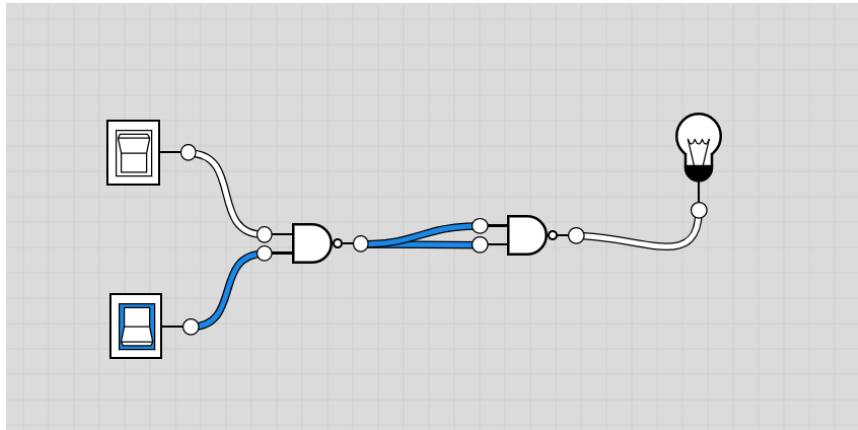
Input 1	Input 2	Output
0	0	0

### Combination#2



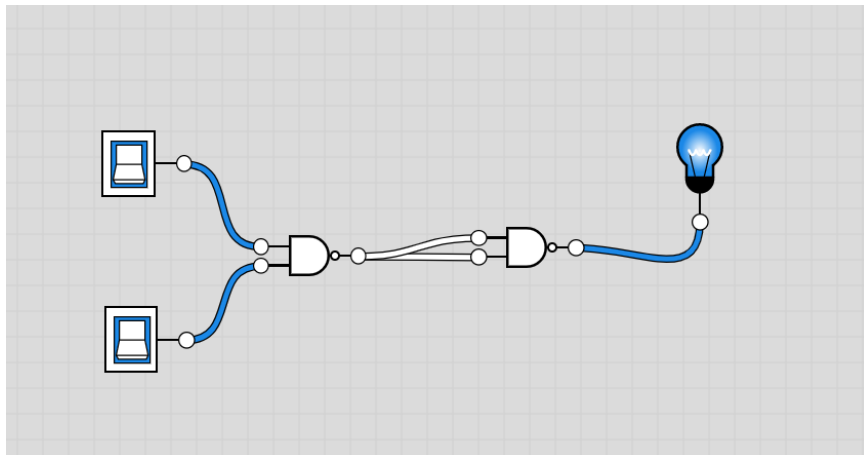
Input 1	Input 2	Output
1	0	0

### Combination#3



Input 1	Input 2	Output
0	1	0

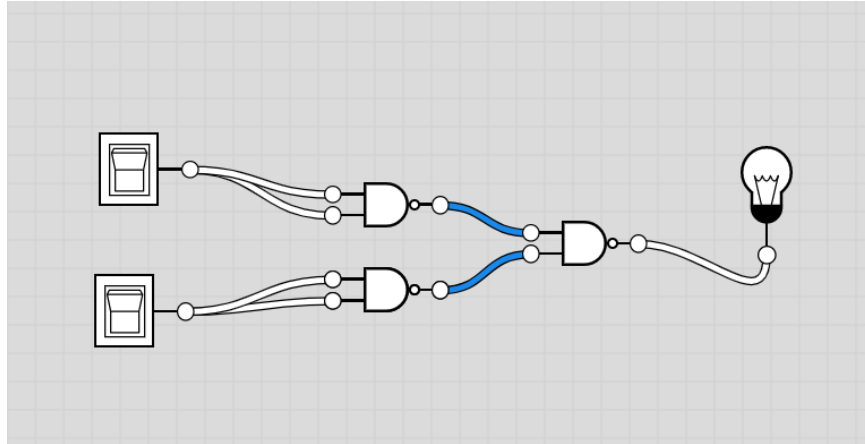
### Combination#4



Input 1	Input 2	Output
1	1	1

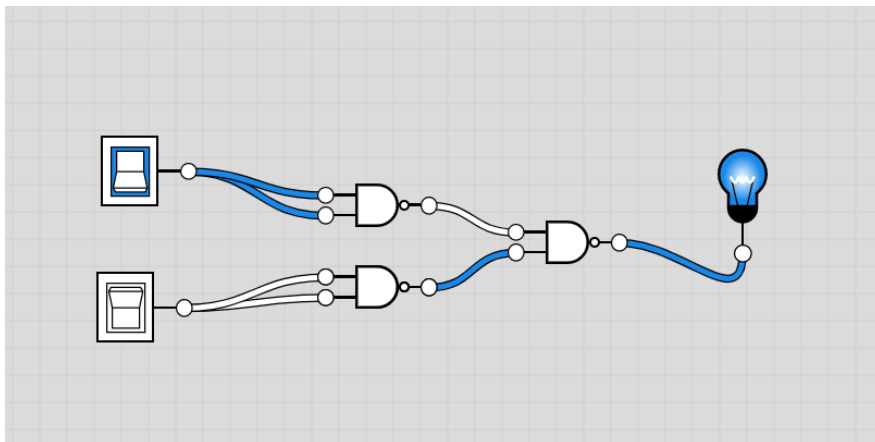
## OR Gate:

### Combination#1



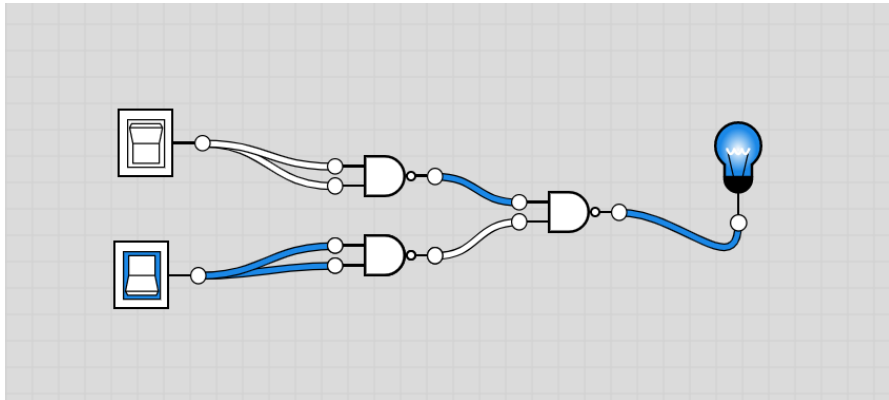
Input 1	Input 2	Output
0	0	0

### Combination#2



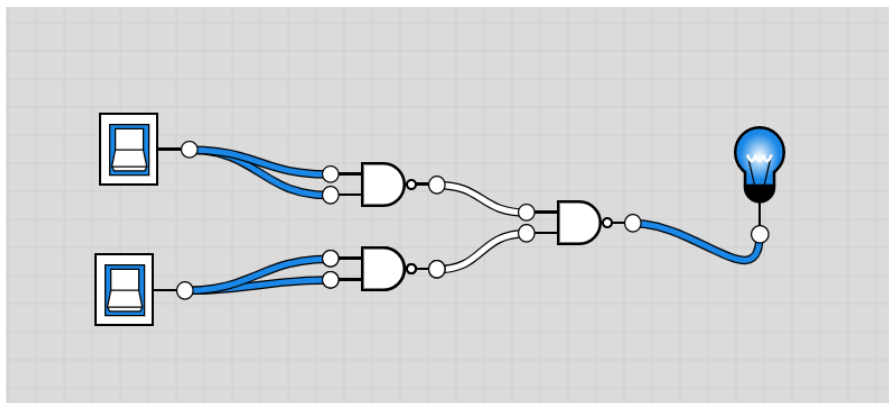
Input 1	Input 2	Output
1	0	1

### Combination#3



Input 1	Input 2	Output
0	1	1

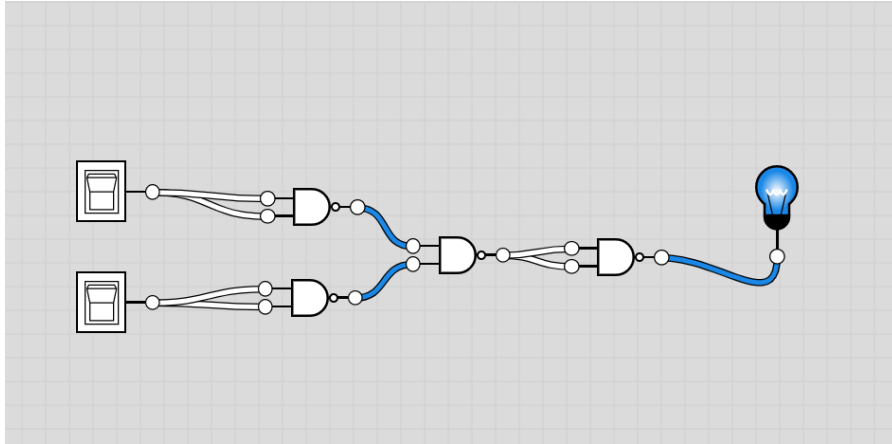
### Combination#4



Input 1	Input 2	Output
1	1	1

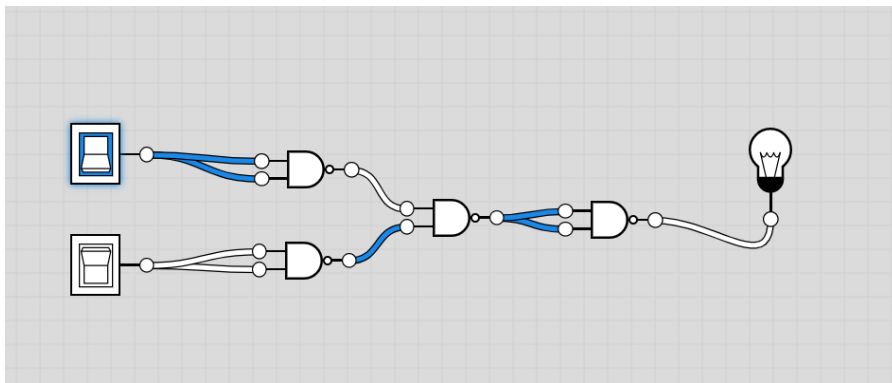
## NOR Gate:

### Combination#1



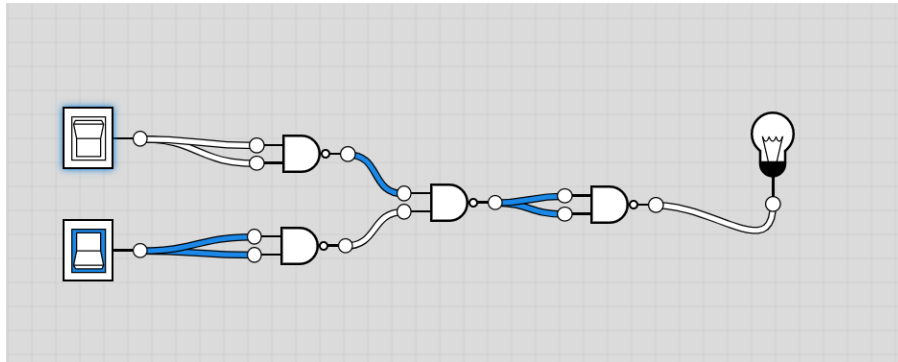
Input 1	Input 2	Output
0	0	1

### Combination#2



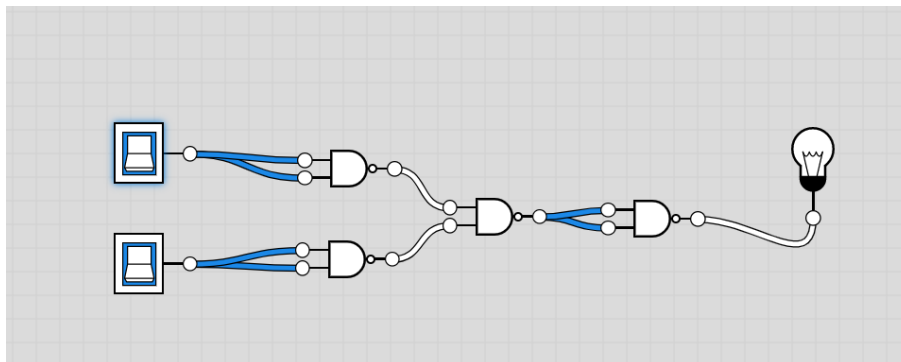
Input 1	Input 2	Output
1	0	0

### Combination#3



Input 1	Input 2	Output
0	1	0

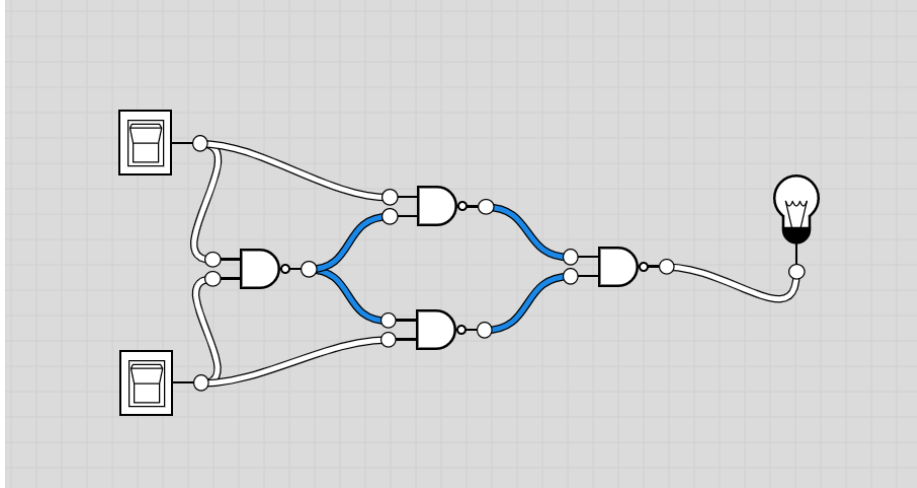
### Combination#4



Input 1	Input 2	Output
1	1	0

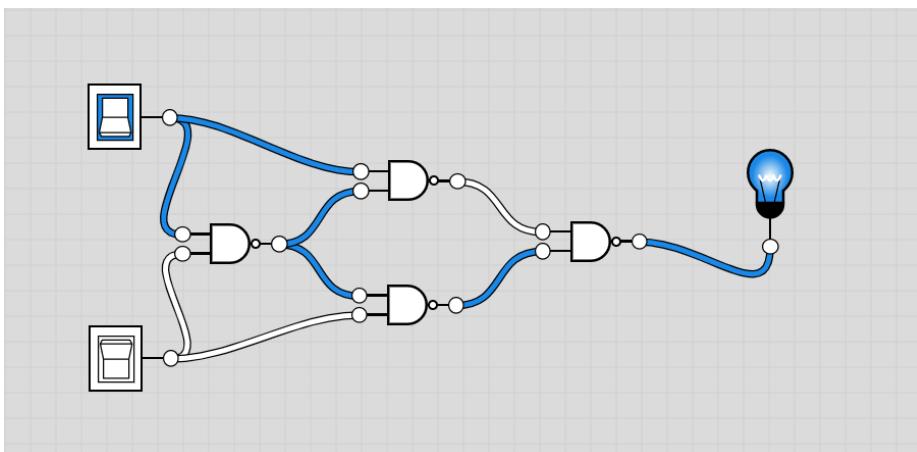
## Ex-OR Gate:

### Combination#1



Input 1	Input 2	Output
0	0	0

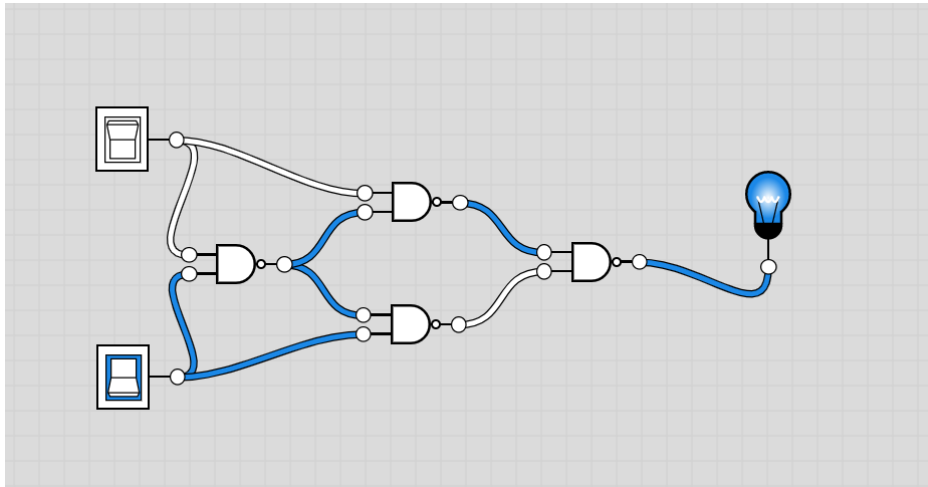
### Combination#2



Input 1	Input 2	Output
1	0	1

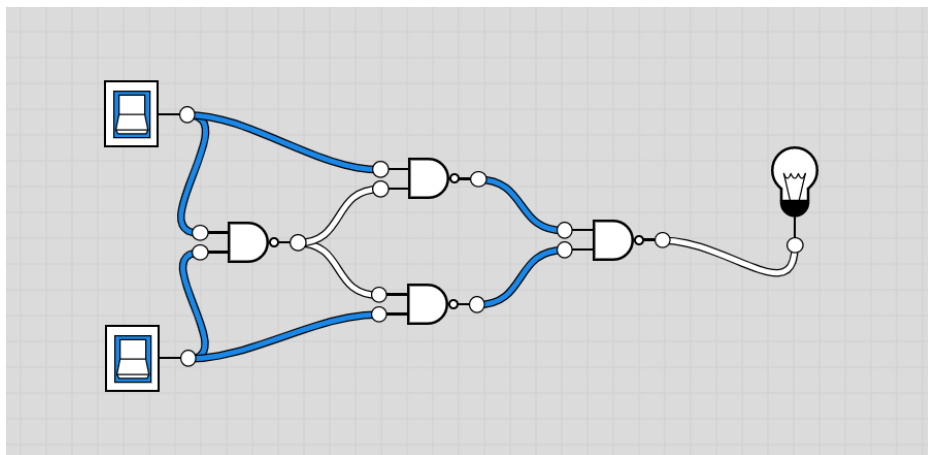


### Combination#3



Input 1	Input 2	Output
0	1	1

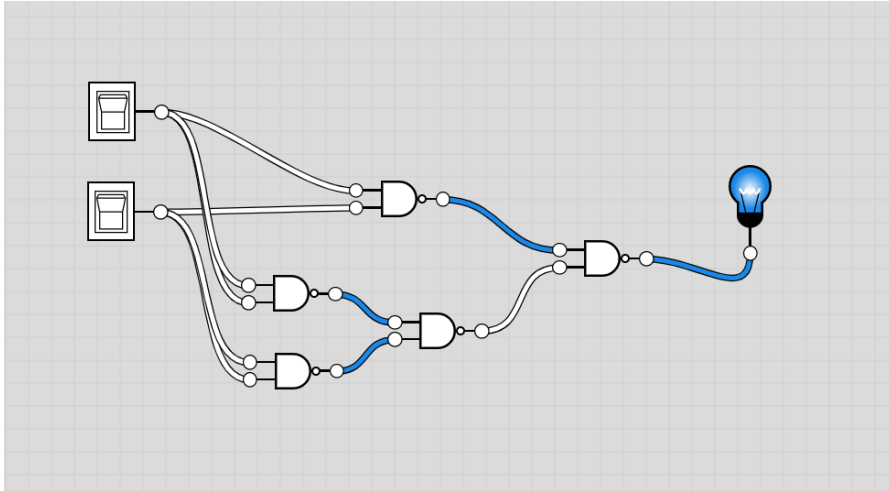
### Combination#4



Input 1	Input 2	Output
1	1	0

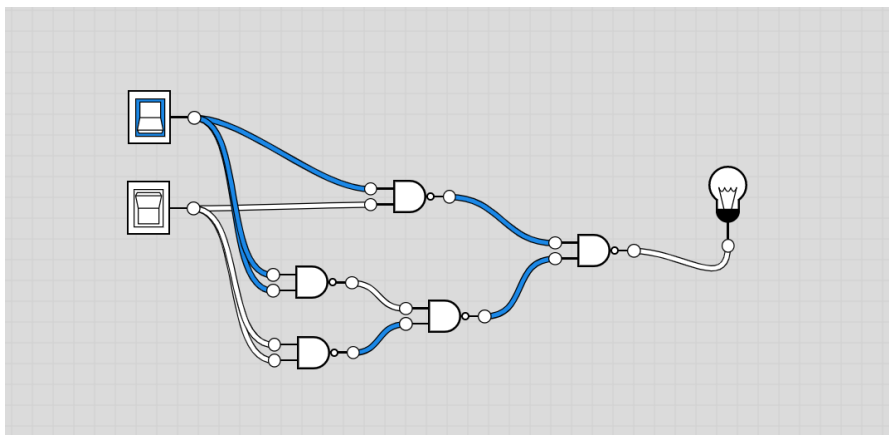
## Ex-NOR Gate:

### Combination#1



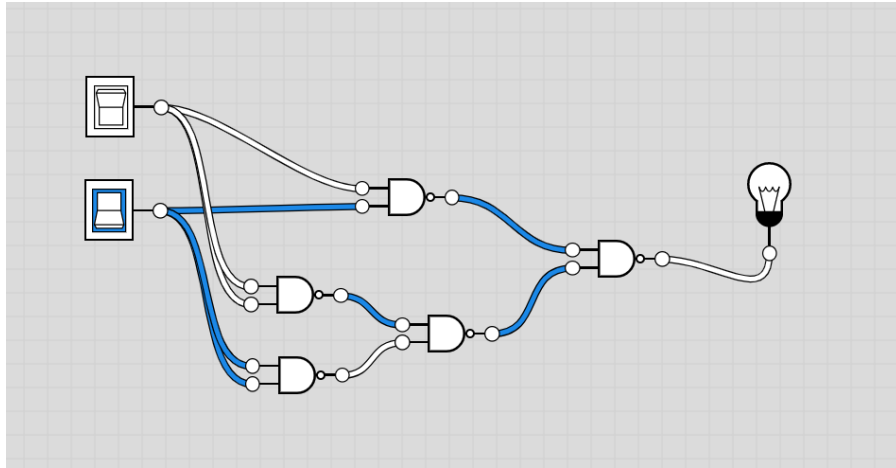
Input 1	Input 2	Output
0	0	1

### Combination#2



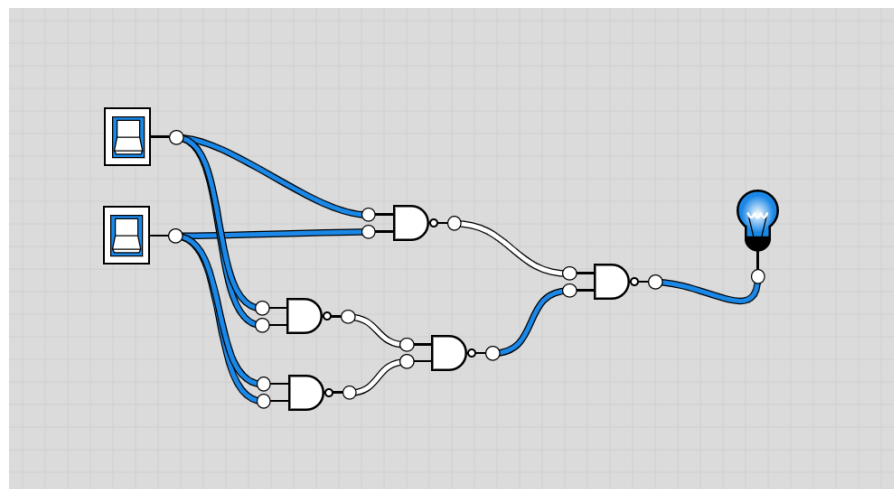
Input 1	Input 2	Output
1	0	0

### Combination#3



Input 1	Input 2	Output
0	1	0

### Combination#4



Input 1	Input 2	Output
1	1	1