INTEGRATED SDR/DDR–SDRAM CONTROLLER

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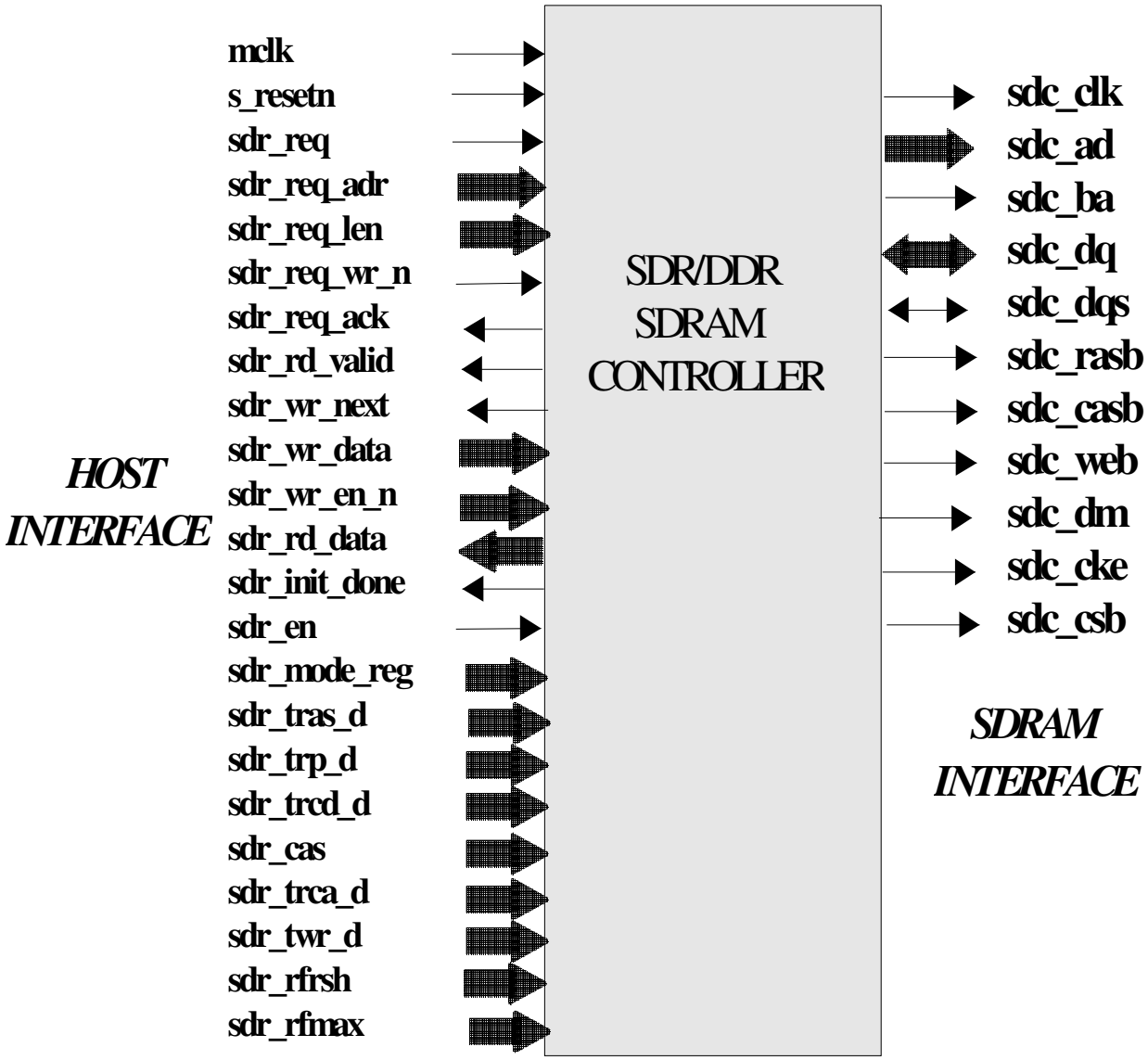
Introduction:–

The sdr/ddr sdram controller is a single controller for single data rate and double data rate sdrams.It supports load_mr,auto_referesh,precharge,act_row,reada,writea, burst_stop and nop commands.It can be programmed for burst lengths of 2,4 and 8 and CAS latencies of 2,2.5 and 3.

Pin Diagram:–

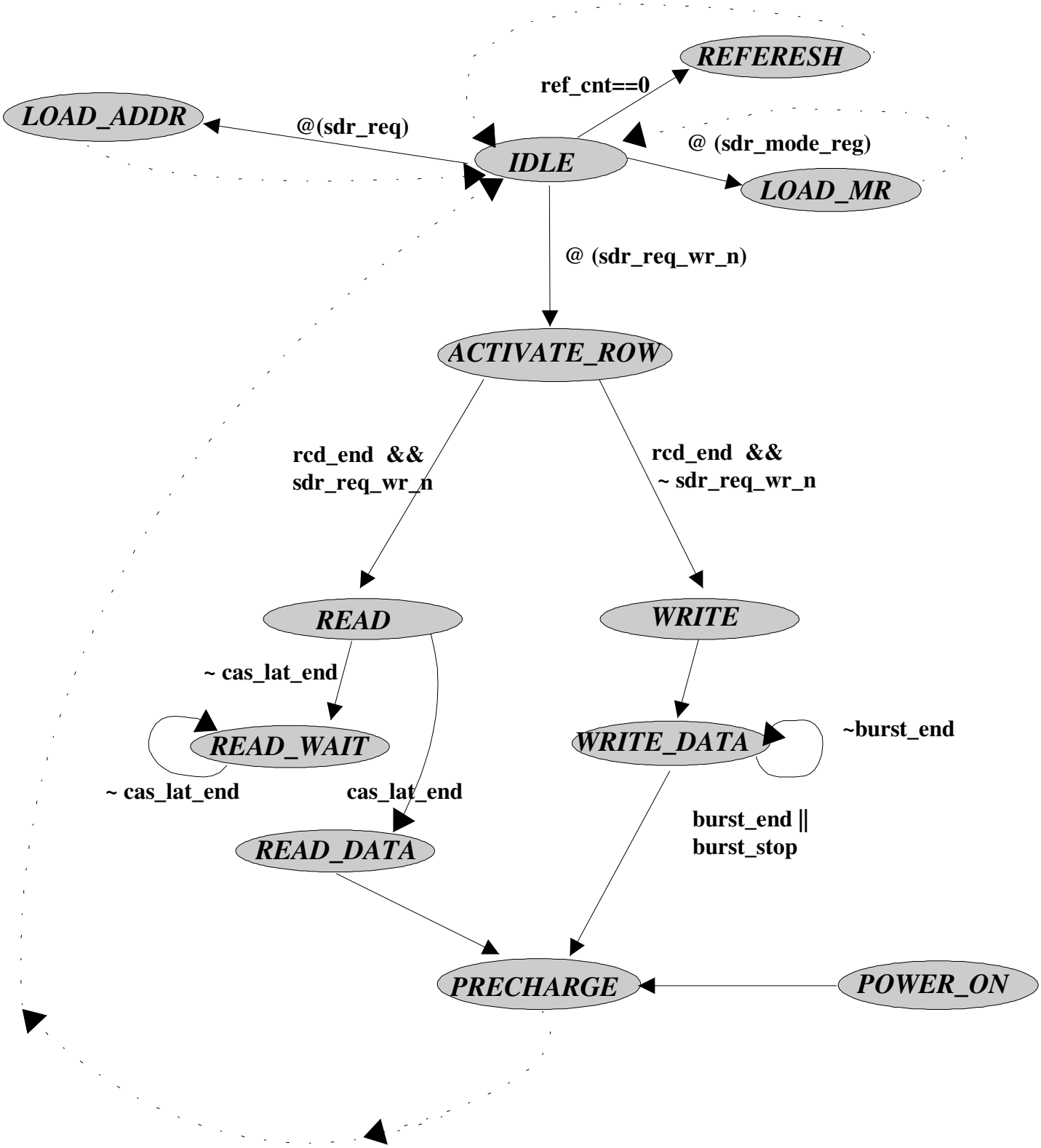


Pin Description:–

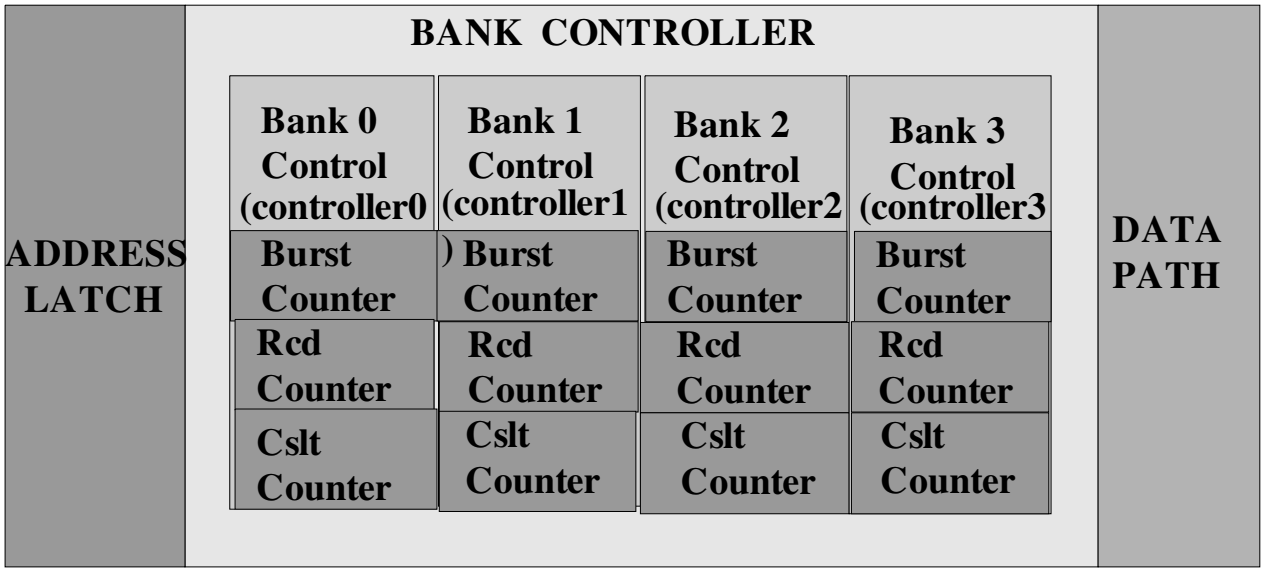
Pin Name	*Pin Direction*	*Pin Description*
----- HOST INTERFACE ----------		
mclk	In	memory clock to controller
s_resetn	In	sysnchronous negative reset
sdr_req	In	to controller
sdr_req_adr	In	to controller(24 bit bus)
sdr_req_len	In	0 (4 bytes or less), 1– (8 to 5 bytes), 2 – (12 to 9 byte), 3 – (16 – 13 bytes)
sdr_req_wr_n	In	0 – write to SDRAM 1 – read from SDRAM
sdr_req_ack	Out	Ack from controller that current read/write started
sdr_rd_valid	Out	valid data on the bus from SDR controller to mermory controller
sdr_wr_next	Out	present next write data
sdr_wr_data	In	32 bits data to SDR controller
sdr_wr_en_n	In	4 bits – byte enables
sdr_rd_data	Out	32 bits data read.
sdr_init_done	Out	initialization complete.
sdr_en	In	enable/disable SDRAM (power_down?)
sdr_mode_reg	In	12 bits mode register data.
sdr_tras_d	In	4 bits, Tras delay in clock cycs for SDRAM
sdr_trp_d	In	4 bits, Trp delay
sdr_trcd_d	In	4 bits, Trcd delay
sdr_cas	In	3 bits Cas latency for SDRAM
sdr_trca_d	In	4 bits, Trca delay
sdr_twr_d	In	4 bits, Twr delay
sdr_rfrsh	In	12 bits, refresh time per row.
sdr_rfmax	In	3 bits, number of rows to refresh per burst.

Pin Name	*Pin Direction*	*Pin Description*
------ SDRAM INTERFACE ----------		
sdc_clk	Out	**Clock for sdram**
sdc_ad	Out	**Address bus**
sdc_ba	Out	**Bank address**
sdc_dq	Inout	**Data bus**
sdc_dqs	Inout	**Data strobe**
sdc_rasb	Out	**Row address select**
sdc_casb	Out	**Column address select**
sdc_web	Out	**Write enable**
sdc_dm	Out	**Data mask**
sdc_cke	Out	**Clock enable**
sdc_csb	**Out**	**Chip select**

State Diagram :–

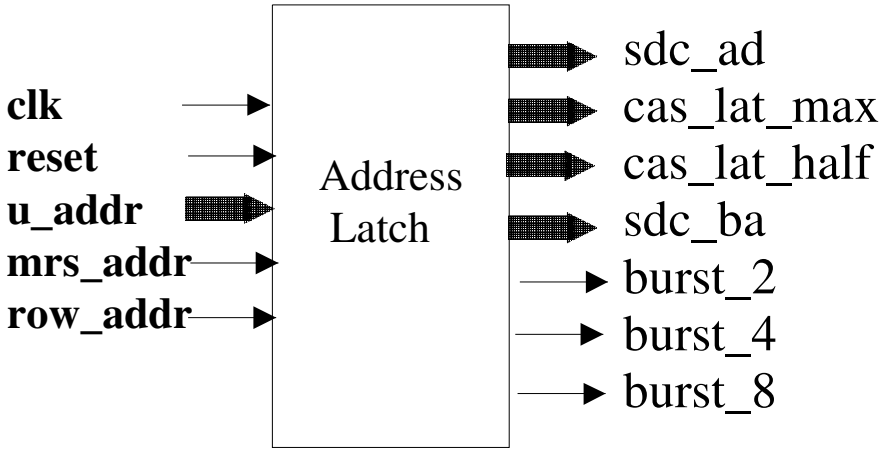


Block Diagram:–



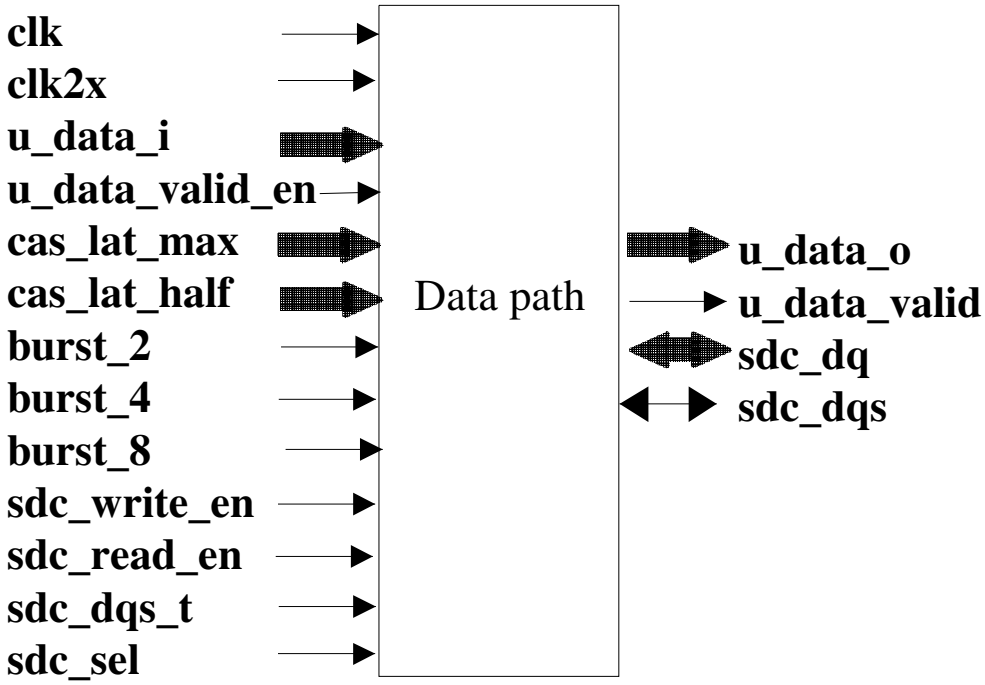
Block Level Description :–

Address Latch Module



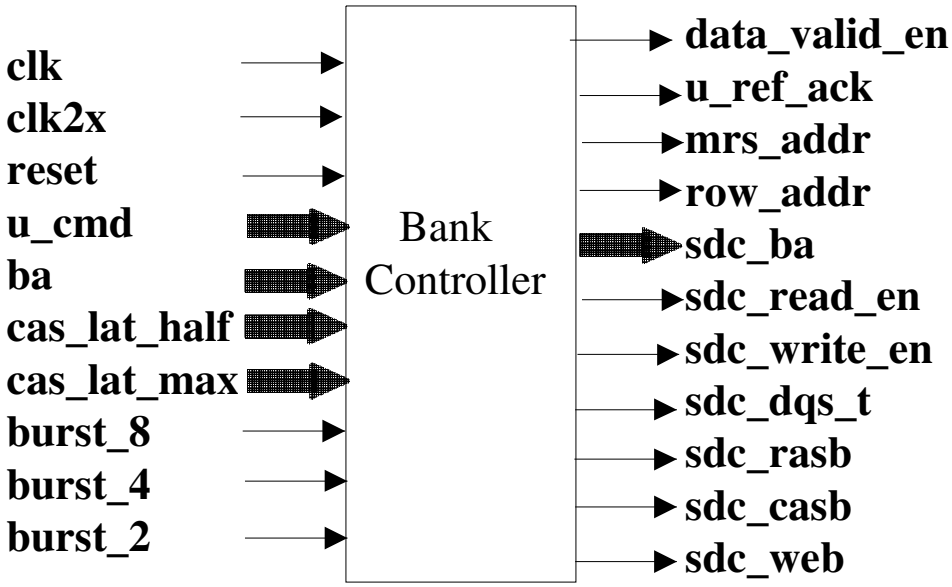
This module takes the address input from host(22bits) and gives out data for ***mode register*** on "sdc_ad" when "mrs_addr" input is high,determines the bank, cas latency,burst length and puts it on the corresponding outputs.When "row_addr" input is high (activate row),"sdc_addr" will have row address on it otherwise column address.

Data Path Module



This module controls the data on the datbus(sdc_dq) according to the "sdc_sel" input during the "write" cycle.If "sdc_sel" is high (single data rate),it will write/read data on every positive edge of the clock else it will write/read data on both the edges of the clock. It also generates data strobe signal on "sdc_dqs" for ddr−sdram, data_valid signal on "u_data_valid" indicating the host that the data on "u_data_o" is valid during read cycle.

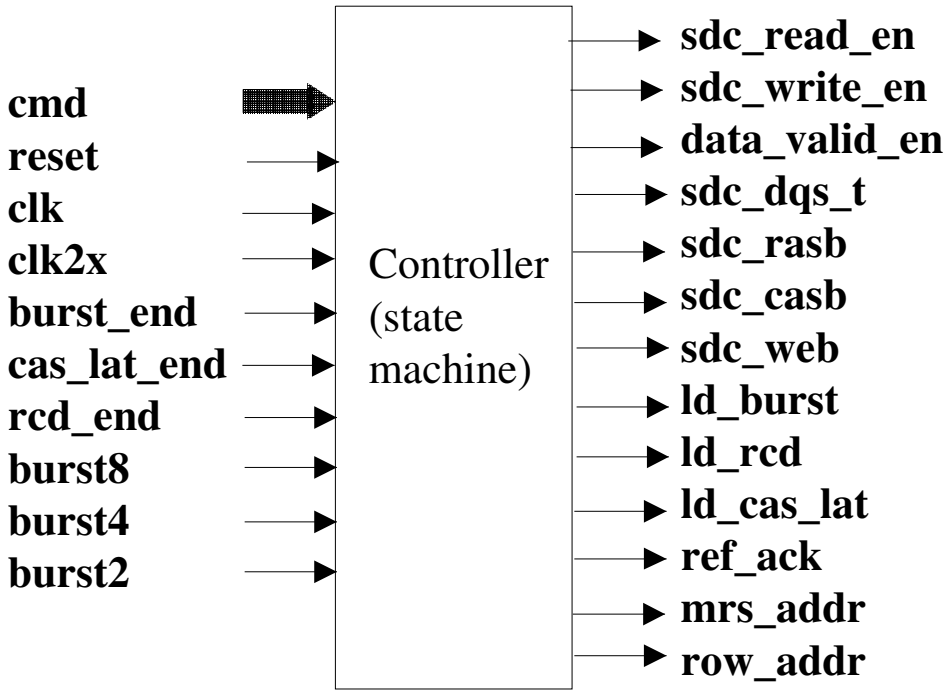
Bank Controller Module



The Bank controller module has 4 controllers for each bank.

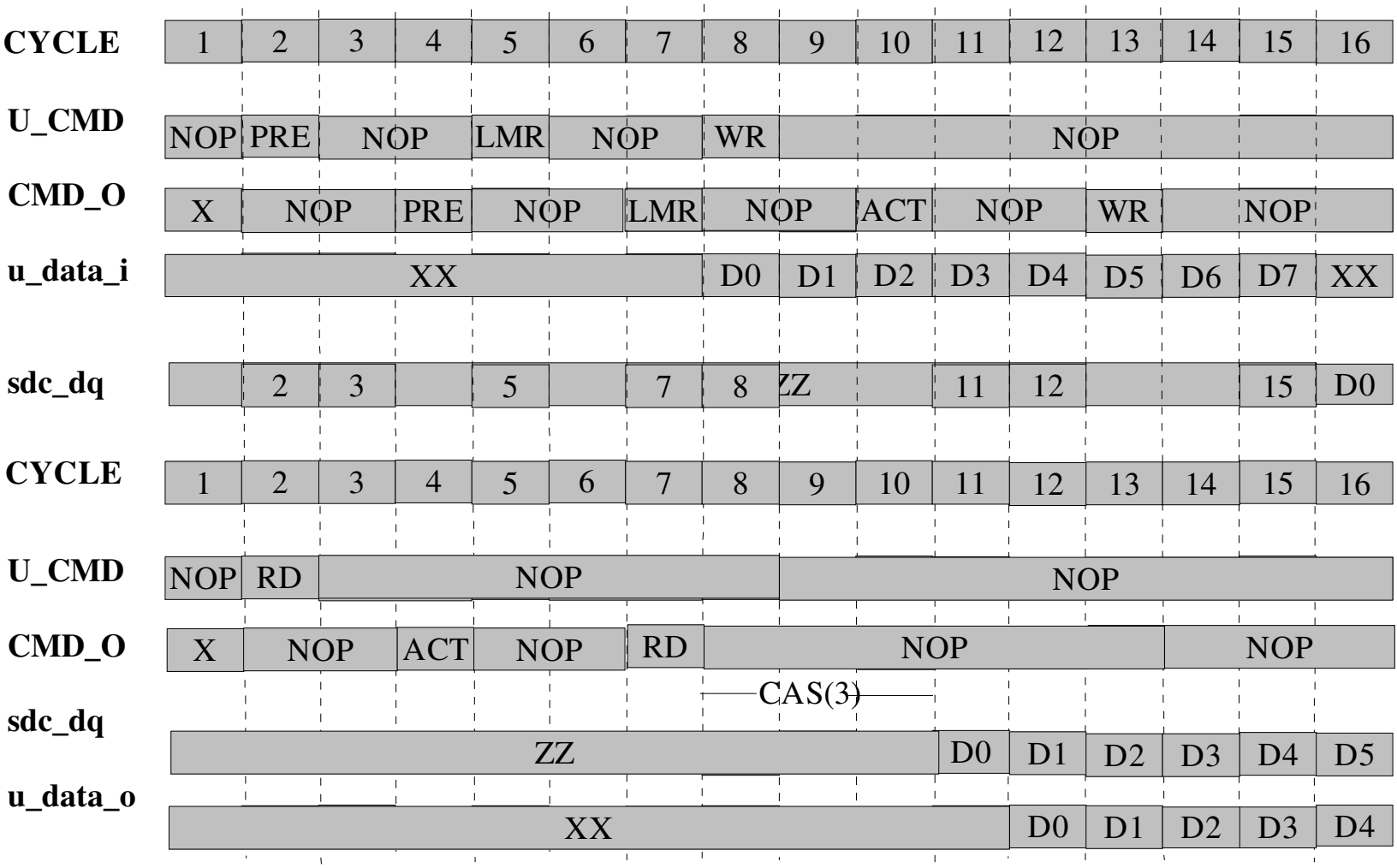
It takes the command input and gives to appropriate controller depending on the bank address.It generates the commands for sdram on"sdc_rasb,sdc_casb,sdc_web". It also gives read &write enable,data valid enable signals for data path module, mrs_addr &row_addr for address latch module. It also gives bank address to the sdram.

Controller Module

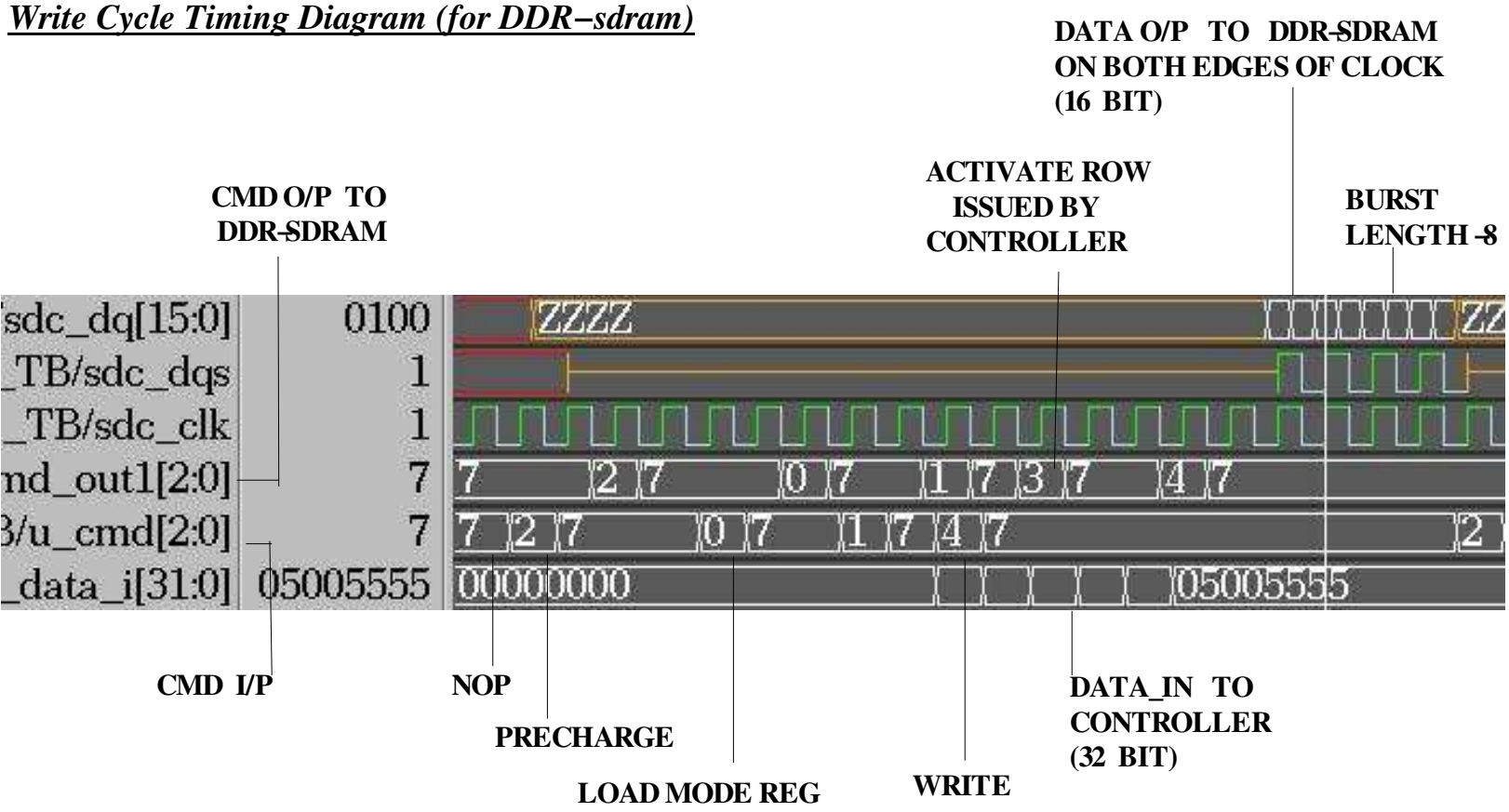


This module gets command from the bank controller depending on the bank address.It loads the burst,rcd,cas latency counters and starts them.It generates the commands for sdram for any particular bank.

Pipeline Diagram :–



Write Cycle Timing Diagram (for DDR–sdram)



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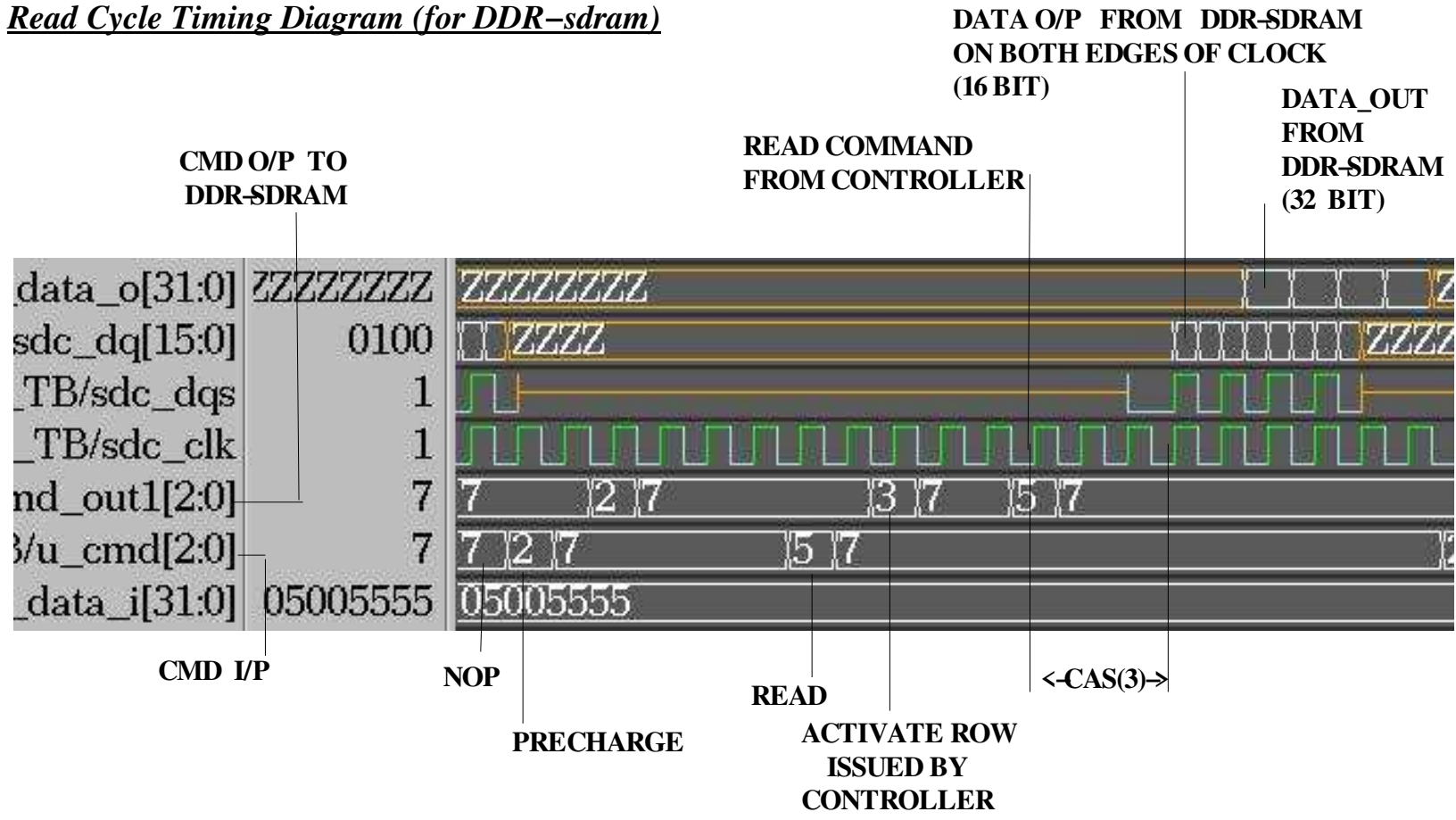
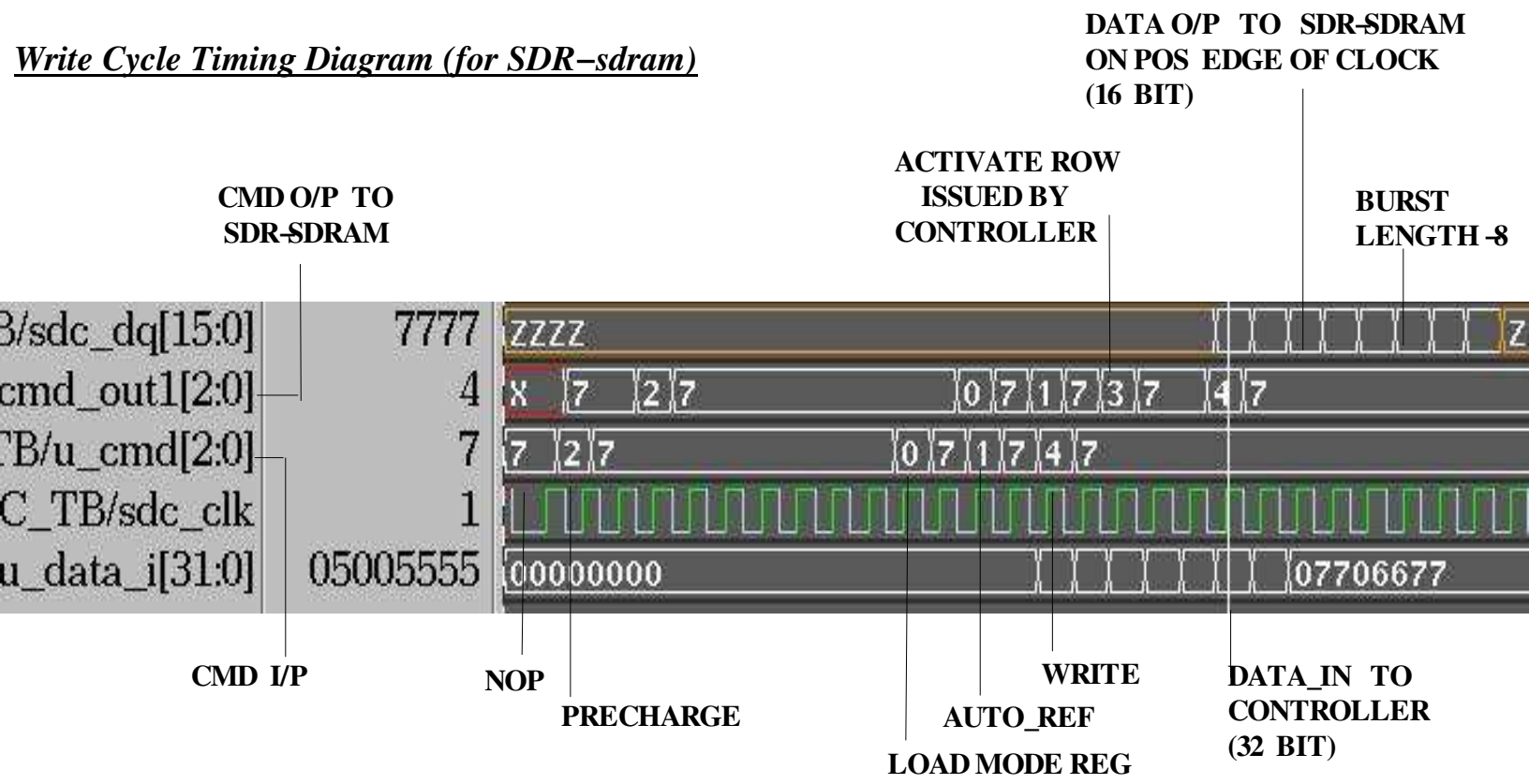


Write Cycle Timing Diagram (for SDR–sdram)



Read Cycle Timing Diagram (for SDR–sdram)