Ne rien inscrire dans ce cadre

Prénom .....

Nom .....

Promotion .....

Groupe .....

Promotion L3 INT

Module Architecture des ordinateurs

Code cours TI6 06I-RAT

Rattrapage - 1h

21/06/2019 10H30 – 11H30

Sujet proposé par : **DAMESTOY Jean-Paul**

Calculatrice autorisée : ☒ **OUI** ☐ **NON**

Documents autorisés : ☐ **OUI** ☒ **NON** **Type de documents :**

Ordinateur portable autorisé : ☐ **OUI** ☒ **NON**

Internet : ☐ **OUI** ☒ **NON**

Traducteur électronique, dictionnaire : ☐ **OUI** ☒ **NON**

Consigne :

Merci de restituer uniquement : **les copies quadrillées**

Rappel :

- Tous les appareils électroniques (téléphones portables, ordinateurs, tablettes, montres connectées …) doivent être éteints et rangés.
- Il est interdit de communiquer.
- Toute fraude ou tentative de fraude fera l'objet d'un rapport de la part du surveillant et sera sanctionnée par la note zéro, assortie d'une convocation devant le conseil de discipline. Aucune contestation ne sera possible. Tous les documents et supports utilisés frauduleusement devront être remis au surveillant.
- Aucune sortie de la salle d'examen ne sera autorisée avant la moitié de la durée de l'épreuve.

Ne rien inscrire dans ce cadre

Exercise 1: a small MCQ to start … (6 points)

1. If we consider a representation of the signed numbers in complement to 2 over 8 bits, the range of numbers that can be represented is:
   a. [-127, +127]
   b. [0, 256]
   c. [-128, +127]

2. If we consider a direct addressing mode, the field **X** of the instruction **LOAD D R1 X** encodes:
   a. An immediate value
   b. The address in the central memory of a word containing the operand
   c. The address in the central memory of a word containing itself the address of the word containing the operand
   d. A register number

3. An 8-bit string is used to code:
   a. 128 different states, this string is called a byte
   b. 256 different states, this string is called a byte
   c. 256 different states, this string is called a quartet

4. The string 1000 1001 encodes the value:
   a. +137 in binary
   b. 89 in hexadecimal
   c. -9 according to the signed 8-bit value convention
   d. +137 according to the agreement of the 8-bit complement to 2
   e. -119 according to the agreement of the 8-bit complement to 2
   f. 211 in base 8

5. The instruction **ADD Im R1 X** makes an addition between:
   a. R1 and an operand contained in the addressed word X
   b. R1 and the immediate value X
   c. R1 and an operand whose address is contained in the address word X

6. An address bus with a width of 16 can be used to address:
   a. 65 536 bytes of an addressable memory per byte
   b. 2 048 bytes of an addressable memory per byte
   c. 16 384 4-byte words from a memory addressable per byte

Exercise 2: integer representation (4 points)

1. Convert the numbers 3167_{10} and 219_{10} in hexadecimal.
2. Convert the numbers $3AE_{16}$ et $6AF_{16}$ in decimal.

Exercise 3: interrogation and interruption input/output modes (6 points)

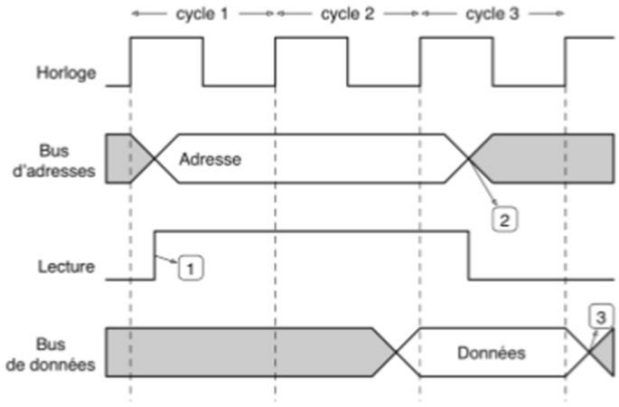
An input/output device makes 10 requests per second, each of which requires 5 000 processor instructions to be processed.

1. Input/output is by interruption. It takes a thousand processor instructions to save the context and start the request processing manager, and another thousand processor instructions to load the context and return to the main process. How many instructions per second does it take to manage I/O?

2. Input/output is now done by interrogation. The processor takes advantage of a pre-existing periodic interruption every hundredth of a second to scan the device and see if there is a request to process. There is therefore no additional cost for context switching. Each query requires five hundred processor instructions, in addition to processing the request if it is present. How many instructions per second does it take to manage I/O?

<u>Exercise 4</u>: calculation of bus flow rates (4 points)

1. Using the following figure (synchronous bus), calculate the flow rate of the bus during a reading operation knowing that its frequency is 100 MHz and that the bus transfers 16 bits at a time.



2. A bus has a frequency of 500 MHz and the memory can send 64 bits on each clock edge (up and down). Calculate the maximum flow rate, ignoring memory access times (assume that all cycles are occupied by data).