COMPUTER ARCHITECTURE
2020 - 2021

TD n°4 - Correction

Exercise 1:

We consider a 2 MB main memory where each byte is separately addressable (→ address = "number of bytes from 0"):

1. Calculate the address, in octal, of the sixth element of an array whose first element's address is 77_8, and whose elements are all 16 bits long.
2. Calculate, in decimal, the number of bytes before the address 77_8.
3. Calculate the size of this memory by expressing it in 16-bit words, then in 32-bit words.

Exercise 2:

If the address register of a memory has 32 bits, calculate:

1. The number of addressable words if 1 word = 1 byte
2. The highest possible address for these 1-byte words
3. The number of addressable words if 1 word = 32 bits
4. The highest possible address for these 32-bit words

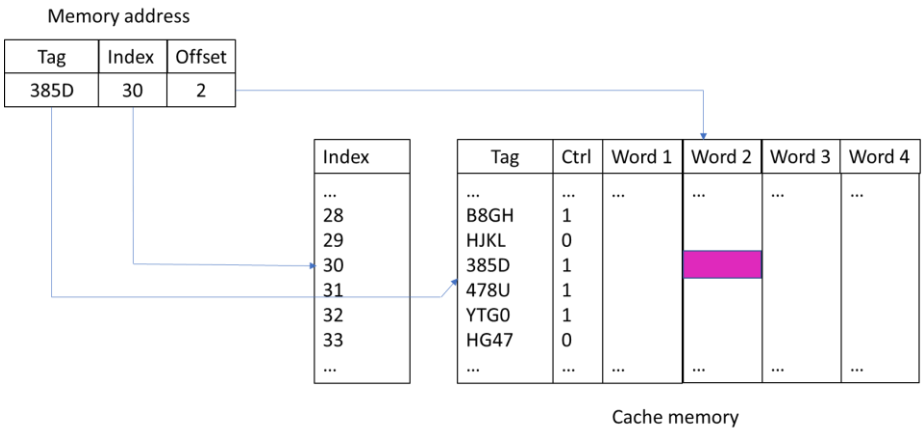
Exercise 3:

A RAM memory, connected to the processor, has a cycle time of 20 ns for the first access and 10 ns for the next three accesses which are accelerated. Each access extracts 8 bytes.

What is the bandwidth of the information transfer between the memory and the processor?

Exercise 4:

As a reminder, a word in a cache memory is accessed via an address that indicates its belonging block (label), its place in the block (offset) and the place of this block in the cache (index) as shown in the following figure.



A processor has a direct-match cache memory with four entries and the following features:

- Memory addresses are 16 bits long.
- Each memory word is 32 bits long.
- The main memory is byte addressable.
- Each cache entry contains a block of four words.

1. What is the capacity of the main memory in KB and K words?
2. What is the length of the label?
3. What is the real size of the cache?

Exercise 5:

A cache has lines of 8 bytes. The access time to the main memory during a line transfer is 50 ns for the first byte and 5 ns per subsequent byte for the rest of the line.

1. What is the average time to retrieve a line if the cache is **write-through**? If 30% of the cache lines are modified, what is the average retrieval time of a line if the cache is **write-back**?
2. If, on average, each line is modified three times, how much time does each cache spend writing the data back to main memory when the line is replaced? At how many rewrites per line is the **write-back** cache more interesting