Optimal Charging of Capacitors

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***Abstract*—Charging a capacitor from a voltage source with internal resistor is one of the basic problems in circuit theory. In recent years, this simple problem has attracted some interest in the area of low-power digital circuits. The efficiency, i.e., the energy stored in the capacitor versus the energy delivered by the source is one of the key measures. The common believe that the source has to deliver twice the capacitor energy holds true only for a linear circuit with step function as source voltage. In this paper we compute several optimal solutions with respect to time and efficiency. The case of nonlinear capacitors is discussed in some detail.**

The source voltage can depend on time in a rather involved manner. However, replacing the voltage source by a current source simplifies the problem significantly since the current has to be constant over time regardless of the characteristic of the capacitance. This result should have implications on the circuit technique employed for low-power circuits.

Furthermore, if leak conductances in parallel to the capacitor are taken into account, the achievable minimal energy dissipation is limited and, if ramps are used for charging, an optimal charging time different from infinity occurs.

***Index Terms*—Adiabatic charging.**

I. Introduction

N THE ADVENT of low-power circuits low-loss charging of linear capacitors from a real source (ideal source with internal resistor) was reconsidered (Fig. 1). This problem was coined as adiabatic switching [1]. Although charging a capacitor is a problem for undergraduates and everything seemed known, the question of how to shape the input voltage to reach a given capacitor voltage and minimize the energy loss in the resistor was posed only recently [6]. Even more, as an input voltage one usually applies step functions but there was no firm reasoning for that.

It turned out that ramp functions can reduce the loss significantly (see [4]). However, this result is not quite correct, as noted in [6]. We will show the correct optimal solution of a nonlinear circuit in Section II. For completeness, we consider charging in the interval $[0,\ T]$ and $[0,\ \infty)$, compute the optimal source voltages, and compare the efficiencies.

Today, this circle of problems is called quasiadiabatic switching but the analysis reveals that replacement of voltage sources by current sources can simplify the circuit structures.

For VLSI circuits nonlinear capacitors are of importance. We restrict our discussion to the nonlinearity of the capacitor of $C(v) \sim (1/(v(t) - V_0)^m)$, which includes the case $C(v) \sim (1/(V_0 - v(t))^m)$ for even m and $C(v) \sim (1/(v(t) + V_0)^m)$ [7]. In fact, the comparison of Figs. 1 and 3 shows the drain-bulk and drain-gate capacitors are charged.

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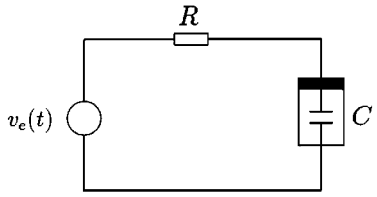

Fig. 1. Circuit for charging a capacitor

II. Method

The input voltage for a given optimality criterion is computed by The methods used are variational calculus and Pontrjagin's maximum principle. This material is well established in mathematics and control and we refer to the literature for details [3]. The procedure to compute the input voltage $v_i(t)$ is the following.

1) Given the dynamical system

$$\frac{dx}{dt} = a(x) + b(x)v(t)$$

with a, b, x scalars.

2) Define the Hamilton function

$$H(\lambda,\ x,\ v,\ t) = -L(x,\ v) + \lambda(a(x) + b(x)v(t)). \quad (1)$$

The time integral of $-L(x,\ v)$ is to be minimized. For the case of loss minimization it measures the power in the resistor, in our case, $L(x,\ v) = -(v_i(t) - v_c(t))^2/R$. If minimal time charging is to be achieved, the function is simply one.

3) Solve

$$\frac{\partial H}{\partial v_i} = 0 \quad (2)$$

for v_i.

4) Solve

$$\frac{d\lambda}{dt} = -\frac{\partial H}{\partial x} \quad (3a)$$

$$\frac{dx}{dt} = \frac{\partial H}{\partial \lambda} \quad (3b)$$

with $x(0) = x_0$, $x(T) = x_T$ given.

Consider the circuit in Fig. 1 with given elements R, $C(v)$. Our goal is to compute an input function $v_i(t)$ such that $v_C(T) = V_H$ for $v_C(0) = 0$.

In addition we require the following

1) minimal time charging with bounded input voltage $|v_i| \leq V_{\max}$, which is reasonable for circuits;
2) low-energy loss in the resistor

$$\min_{v_i(t)} \frac{(v_R)^2}{R} \qquad v_C(T) = V_H.$$

Both problems have different solutions: one is well known and the other not quite as well known.

To compare the energy consumption of the resistor for different input signals the efficiency η is introduced as the ratio of the energy stored in the capacitor and the energy delivered by the source

$$\eta = \frac{E_C}{E_Q}.$$

III. Minimal Time Charging

The solution of optimization problems with bounded input signals is difficult in general but very simple for the considered RC circuit. To solve the minimal time problem, the function L reduces to one [3]. As a result of Pontrjagin's maximum principle, H has to be maximized by $v_i(t)$ for every t. It follows for the optimal input signal v_*

$$\lambda b(x) v_* > \lambda b(x) v_i.$$

v_i is chosen according to

$$v_i(t) = \begin{cases} +V_{\max}, & \lambda b(x) > 0 \\ -V_{\max}, & \lambda b(x) < 0 \\ \text{undef.}, & \lambda b(x) = 0 \end{cases}.$$

It can be shown (see [3] for further results) that for a linear system of order n with real eigenvalues, a minimal time control consists of at most $n-1$ switchings between $V_{\max}$ and $-V_{\max}$. Therefore, for the first-order system at hand, which has one real eigenvalue, one switching determines the minimal time charging. This is exactly the step input function. Note that this solution holds true also for nonlinear capacitors.

The efficiencies for different types of $C(v)$ for constant input voltage V_i are computed from

$$E_C = \int_0^T v_C(t) C(v_C) \frac{dv_C(t)}{dt}\, dt = \int_0^{V_H} v_C(t) C(v_C)\, dv_C$$

and the energy of the source

$$E_Q = \int_0^{V_H} V_i C(v_C)\, dv_C.$$

We obtain the following solutions ($x = V_H/V_0$, $y = V_i/V_0$):

- $C(v) = (C_0 V_0^k/(v - V_0)^k)$, k even

$$\eta = \frac{1}{k-2}\,\frac{1}{y}\,\frac{(x-1)^{(k-1)} + kx - 1 - x}{((x-1)^{(k-1)} + 1)} \tag{4a}$$

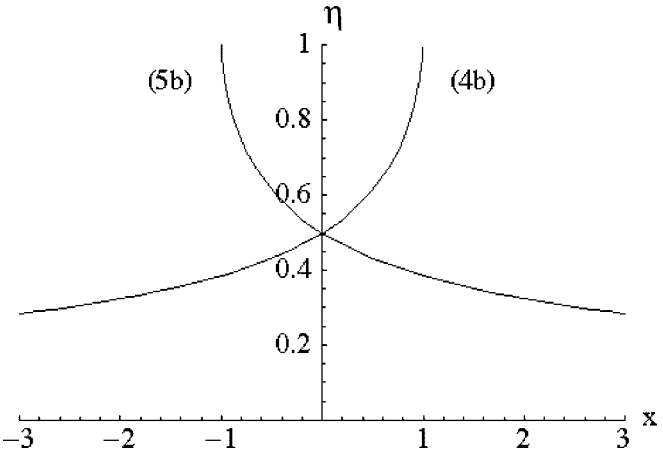

Fig. 2. Efficiency for nonlinear charging over x ($y = 1$)

and for $k = 2$

$$\eta = \frac{1}{y}\left(1 + \left(\frac{1}{x} - 1\right)\log(1-x)\right); \tag{4b}$$

- $C(v) = (C_0 V_0^k/(v + V_0)^k)$

$$\eta = \frac{1}{k-2}\,\frac{1}{y}\,\frac{1 + x(k-1) - (1+x)^{(k-1)}}{1 - (1+x)^{(k-1)}} \tag{5a}$$

and for $k = 2$

$$\eta = \frac{1}{y}\left(-1 + \left(1 + \frac{1}{x}\right)\log(1+x)\right); \tag{5b}$$

- $C = \text{const}$

$$\eta = \frac{1}{2}\,\frac{V_H}{V_i}. \tag{6}$$

During charging $x < y$ holds. The system settles for $x = y$. In the linear case the efficiency can never be larger than $1/2$. For nonlinear capacitors this is not the case. Depending on the ratio x efficiencies close to one are possible. However, (4b) holds for a junction capacitance in reverse mode. In this case, $x < y$ holds and, hence, the efficiency drops below $1/2$. Equations (4b) and (5b) are depicted in Fig. 2.

Note that all solutions for the settled system do not depend on the characteristic of the resistor, in particular it can be nonlinear. This is due to the infinite settling time. The efficiency depends only on the capacitor.

IV. Loss Minimization

A. Linear Capacitor

1) Optimal Solution: To compute $v_i(t)$ for a reduction of the energy loss in R, we require $v_C(0) = 0$ and $v_C(T) = V_H$. The Hamiltonian function is given by

$$H = \frac{(v_i(t) - v_C(t))^2}{R} + \lambda(t)\frac{1}{\tau}(v_i(t) - v_C(t)). \tag{7}$$

TABLE I
EFFICIENCY OF CHARGING A LINEAR CAPACITOR BY A CURRENT SOURCE, EQ (11)

τ/T	0	0.1	0.2	0.3	0.4	0.5
η_{sr1}	1	0.83	0.71	0.62	0.55	0.5

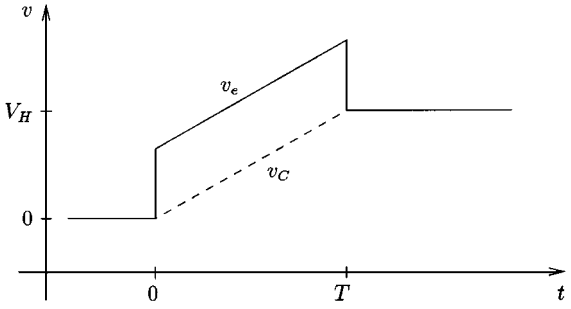

Fig. 3. Input signals for maximum efficiency of linear circuit.

From (2) we obtain $v_i = (2\tau v_C(t) - R\lambda(t)/2\tau)$. This is substituted in (3). From the solution of (3), the capacitor voltage follows as

$$v_C(t) = \frac{V_H}{T}t. \tag{8}$$

Together with the solution for λ: $\lambda(t) = -(2\tau^2 V_H/RT)$, we obtain for the optimal input voltage

$$v_i(t) = \frac{\tau + t}{T}V_H. \tag{9}$$

The input function consists of a step function and a ramp (Fig. 3)

$$v_i(t) = \frac{\tau V_H}{T}\,\sigma(t) + \frac{V_H}{T}\,t. \tag{10}$$

The voltage drop at the resistor is constant for $0 < t \leq T$

$$v_R = \frac{\tau V_H}{T}\,\sigma(t). \tag{11}$$

Therefore, the current $i_R = v_R/R$ is also constant. One concludes that low-power charging is realized easily by driving the capacitor from a current source.

At $t = T$ capacitor stores the energy ($E_C(0) = 0$)

$$E_C = \tfrac{1}{2}\,CV_H^2 \tag{12}$$

while the loss in R is given by

$$E_R = \frac{\tau^2 V_0^2}{RT} = i_R^2 RT. \tag{13}$$

This yields an efficiency of (index sr for step-ramp function)

$$\eta_{sr1} = \frac{E_C}{E_C + E_R} = \frac{1}{1 + 2\dfrac{\tau}{T}}. \tag{14}$$

Some values of η_1 are given in Table I.

From Table I, one concludes that charging C with $v_i(t)$ taken from (9) improves efficiency as compared to an input voltage step function for

$$\tau < 0.5T.$$

TABLE II
OVERALL EFFICIENCY OF CHARGING A LINEAR CAPACITOR BY A CURRENT SOURCE OR STEP RAMP INPUT VOLTAGE

τ/T	0.1	0.2	0.3	0.4	0.5	1.0	1.25
η_{sr2}	0.98	0.94	0.89	0.83	0.78	0.57	0.5

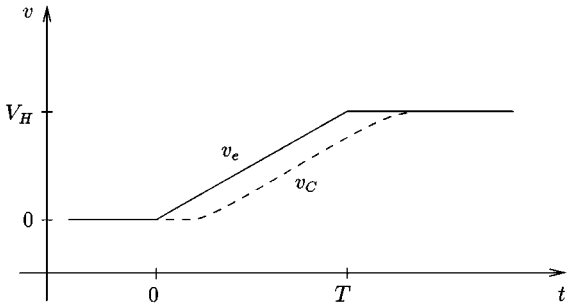

Fig. 4. Input voltage for quasioptimal charging

Here, we have assumed an efficiency of charging with a step voltage of $\eta_{\text{Step}} = 0.5$. This holds only for $t \to \infty$. For other t the efficiency is determined by $\eta_{\text{Step}} = 0.5(1 - \exp T/xt) = 0.5V_H/V_i$. We omit this detail. The charging time has to be at least twice the time constant of the system.

For $t > T$ the input voltage has to be continued in some way. Note that the optimization problem for variable T has as solution $T \to \infty$, which amounts to charging with zero current. One way to continue the input voltage is shown in Fig. 3. T The supply voltage v_i is reduced to $v_C(T)$. The charging process stops immediately. Energy is not consumed anymore.

If we hold the input voltage a the level $v_i(T) = (\tau + T/T)V_H$, the capacitor is further charged up to $v_C = v_i$. This is reasonable, for $|V_H - v_C(t)|$ small. In this case the resistor consumes

$$E_{R2} = \frac{\tau^3 V_H^2}{2RT^2}$$

and the capacitor stores

$$E_{C2} = \frac{C\tau}{2T^2}(2T + \tau)V_H^2.$$

Using $x = \tau/T$ the overall efficiency is given by

$$\eta_{sr2} = \frac{E_C + E_{C2}}{E_C + E_{C2} + E_R + E_{R2}} = \frac{(1+x)^2}{x^3 + 3x^2 + 2x + 1}. \tag{15}$$

Numerical values are presented in Table II.

2) Quasi-Optimal Solution: Now compare the above results with the quasi-optimal solution $v_i(t) = kt$ as given in the literature (Fig. 4). In this case $v_C(t)$ evolves as

$$v_C(t) = k(t - \tau) + k\tau \exp\left(-\frac{t}{\tau}\right).$$

TABLE III
EFFICIENCY OF CHARGING A LINEAR CAPACITOR BY A RAMP VOLTAGE

τ/T	0.1	0.2	0.3	0.4	0.42	0.5	1.0
η_{r1}	0.82	0.69	0.60	0.52	0.50	0.46	0.28

TABLE IV
OVERALL EFFICIENCY OF CHARGING A LINEAR CAPACITOR BY A RAMP VOLTAGE

τ/T	0.1	0.2	0.3	0.4	0.5	1.0
η_{r2}	0.85	0.76	0.70	0.66	0.63	0.57

Hence, the voltage at the resistor is not constant. The efficiency for the interval $[0, T]$ reads

$$\eta_{r1} = \frac{(x\exp(1/x) - x - \exp(1/x))^2}{\exp\ 1/x(\exp\ 1/x + 2x + 2xh2 - 2x^2\exp\ 1/x)}$$

and is independent of k. Numerical values are listed in Table III.

For the interval $[0, \infty)$ we obtain

$$\eta_{r2} = \frac{\exp\ 1/x}{\exp\ 1/x + 2x\ \exp\ 1/x + 2x^2\ \exp\ 1/x}$$

with some values in Table IV.

We conclude from our results that energy loss optimal charging of a linear capacitor is done best by a input signal $v_i(t) = (t + \tau/T)V_H$ $(t < T)$ or, equivalently, a constant current source $i_i = (\tau V_H/TR)$ in $t \in [0, T]$ and zero otherwise.

For a periodic signal v_C, the efficiency can be increased for $\tau < 0.5T$ and it gets larger the smaller τ/T is.

A ramp function $v_i = kt$ slightly decreases the efficiency as long as one considers only time intervals $t < T$ (Tables I and III). A significant decrease on η is observed if the time interval $0 \le t < \infty$ is considered (Tables II and IV).

B. Nonlinear Capacitor $C(v) \sim 1/(v - V_0)^2$

The solution for the optimal control problem for nonlinear capacitors cannot be computed in closed form for arbitrary capacitors. However, for the technical interesting case of a MOSFET gate capacitor $C(v) \sim (1/(v - V_0)^2)$ and $C(v) \sim (1/\sqrt{V_0 + v})$ and some others, a closed form solution is possible.

The differential capacitance is given by

$$C(v_C) = \frac{C_0}{(V_0 - v_C)^2}$$

which yields the differential equation

$$C(v_C)\frac{dv_C(t)}{dt} = -v_C(t) + v_i(t).$$

As a Hamiltonian function we use ($\tau = RC_0$, $[\tau] = V^2 s$)

$$H = \frac{(v_i - v_C)^2}{R} + \frac{\lambda}{\tau}(v_i - v_C)(V_0 - v_C)^2.$$

The optimal solution is given by

$$v_C(t) = \frac{tV_0V_H}{tV_H + T(V_0 - V_H)}$$

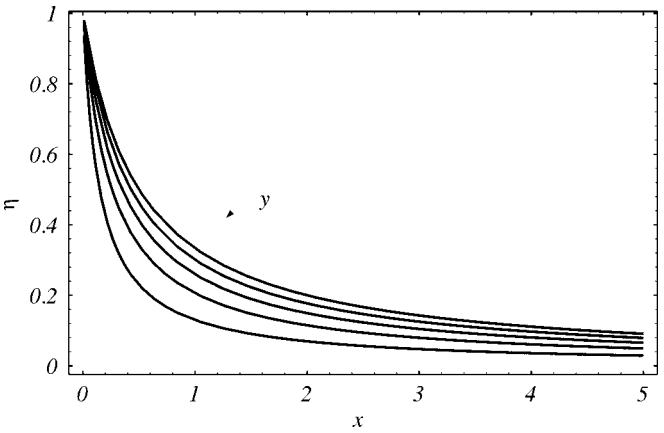

Fig. 5. Efficiency for nonlinear charging over x with curve parameter y

such that the circuit is driven by ($y = V_H/V_0$, $\tilde{t} = t/T$, $x = \tau/(V_0^2 T)$)

$$\begin{aligned} v_i(t) &= V_H \frac{T\tau V_0 - T\tau V_H + t(TV_0^3 + \tau V_H - TV_0^2 V_H)}{TV_0(V_0 - V_H)(T(V_0 - V_H) + tV_H)} \\ &= \frac{\tilde{t}(1 - y + xy) + x - xy}{(1 - y)(1 - y + \tilde{t}y)}. \end{aligned}$$

Again, the voltage drop at the resistor is constant:

$$v_R = \frac{\tau V_H}{TV_0(V_0 - V_H)}.$$

Hence, also in this case, a current source with current $i_R = v_R/R$ yields low loss charging.

During the time interval $[0, T]$ the energy

$$E_R = \frac{\tau^2 V_H}{TR(V_0^2 - V_0V_H)^2}$$

is lost and

$$E_C = \frac{CV_H}{V_0 - V_H} + C\log\frac{V_0 - V_H}{U_0}$$

is stored in the capacitor. This amounts to an efficiency which depends both on $y = V_H/V_0$ and $x = \tau/(V_0^2 T)$

$$\eta_{nl} = \frac{(y-1)((y-1)\log(1-y) - y)}{xy^2 + (1-y)y + (y-1)^2\log(1-y)}.$$

A plot of η_{nl} for different values of x is shown in Fig. 5. For $y \ll 1$, a series expansion at $y = 0$ yields

$$\eta_{nl} \approx \frac{1}{1+2x} + \frac{4xy}{3(1+2x)^2} + O(y^2).$$

Note the correspondence of the first term with the solution for the linear case (14).

TABLE V
EFFICIENCY OF CHARGING A SQUARE ROOT CAPACITOR BY A RAMP VOLTAGE

$T/(C_0R)$	10	30	50	70	90	100
$\eta \quad x=1$	0.59	0.81	0.88	0.91	0.93	0.93
$\eta \quad x=5$	0.65	0.85	0.90	0.93	0.94	0.95
$\eta \quad x=10$	0.69	0.87	0.92	0.94	0.95	0.96

C. Nonlinear Capacitor $C(v) \sim 1/(v+V_0)^{(1/2)}$

For the nonlinear capacitance $C(v) = (C_0\sqrt{V_0}/\sqrt{v+V_0})$ the computation of the optimal input voltage yields $(x = v_C(T)/U_0 = V_H/V_0)$

$$v_i(t) = V_0\left(\frac{t}{T}\sqrt{1+x}+1-\frac{t}{T}\right)^2 - V_0 - \frac{4CR}{T}V_0(1-\sqrt{1+x}) \tag{16}$$

$$v_C(t) = V_0\left(\frac{t}{T}\sqrt{1+x}+x-\frac{t}{T}\right)^2 - V_0. \tag{17}$$

Again, the voltage drop at the resistor is constant

$$v_i(t) - v_C(t) = \frac{4C_0R}{T}v_0(\sqrt{1+x}-1). \tag{18}$$

This simplifies the practical realization of the driving source. The efficiency of the charging process in the time interval $[0, T]$ is given by

$$\eta = \frac{2+\sqrt{1+x}}{24\dfrac{C_0R}{T}+2+\sqrt{1+x}}. \tag{19}$$

As opposed to step function charging, this efficiency comes arbitrarily close to 1 as T increases! Some values for different ratios $x = V_H/V_0$ are listed in Table V.

The computation of the efficiencies for more general exponents k goes along the same line as for the chosen special cases. Details are omitted here.

D. Linear Circuit with Leak Conductance

If we consider a circuit as shown in Fig. 6, which is simply a NOT gate, we see that it has to be described by the linear approximation shown in Fig. 7. This description is a fairly good one. The leak conductance parallel to the capacitor C derives from the closed NMOS transistor. The question may arise as to whether this transistor is necessary, since we will see that such a leak conductance is a grave drawback which limits the achievable amount of energy saving. However, if such a pull down transistor is omitted, a problem occurs when the transmission gate is turned off. The parasitic capacitance parallel to the transmission gate will cause the output voltage to rise to some fraction of the supply voltage, thus causing unwanted energy consumption in following logic stages. This so-called charge sharing is well known from other kinds of dynamic logic [8] and must be avoided by all means. Thus, a pull-down network comprised of a NMOS logic is necessary. Further on, even if there was a way around using these pull down transistors, there will still be leakage through the bulk junctions of the transmission gate transistors. Thus, in any case, we have to deal with a leaky circuit.

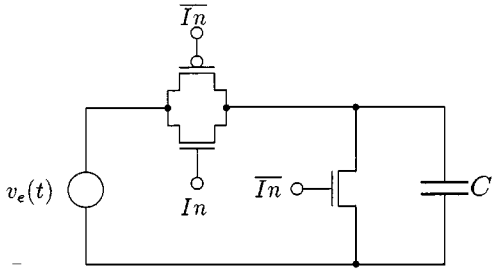

Fig. 6. Adiabatic NOT gate

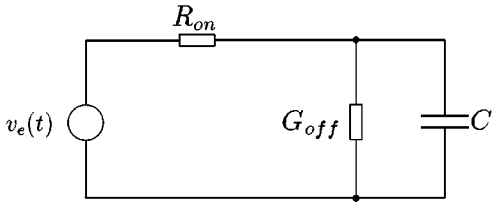

Fig. 7. Linear approximation of NOT gate

1) Optimal Solution: For such a leaky circuit, the computation of the optimal solution yields for the capacitor voltage

$$v_C(t) = V_H\frac{\sinh(\lambda t)}{\sinh(\lambda T)} \tag{20}$$

and for the input voltage required to cause this development of the capacitor voltage $(R_{\text{off}} = 1/G_{\text{off}})$

$$v_i(t) = \left(V_HR_{\text{on}}C\lambda\cosh(\lambda t) + V_H\frac{R_{\text{on}}}{R_{\text{off}}}\sinh(\lambda t) + V_H\sinh(\lambda t)\right)\Big/\sinh(\lambda T) \tag{21}$$

with

$$\lambda = -\frac{\sqrt{R_{\text{on}}+R_{\text{off}}}}{C\sqrt{R_{\text{on}}R_{\text{off}}}} \tag{22}$$

being the solution of the variational problem and V_H being the required voltage rise.

If we define $x = R_{\text{off}}/R_{\text{on}}$ as an abbreviation, the efficiency η is shown in (23) at the bottom of the page.

$$\eta = \frac{x\sqrt{1+x}\sinh(\lambda T)}{-2\cosh(\lambda T) - 2x\cosh(\lambda T) + 2\sqrt{1+x}\sinh(\lambda T) + x\sqrt{1+x}\sinh(\lambda T)}. \tag{23}$$

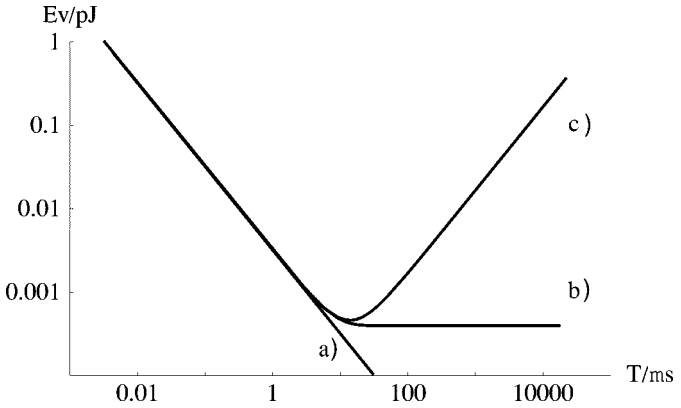

Fig. 8. Energy dissipation per charge/discharge cycle. a) $G_{\rm off} = 0$, optimal driving voltage (9). b) $G_{\rm off} \neq 0$, optimal driving voltage (21). c) $G_{\rm off} \neq 0$, ramping voltage (not optimal); elements: $C = 0.2$ pF, $R_{\rm on} = 3\,{\rm k}\Omega$, $G_{\rm off} = 2$ pS.

Due to the additional loss term $G_{\rm off}$ the current from the supply is no longer constant but is given by

$$i = (v_i - v_C)/R_{\rm on}.$$

Typically, $R_{\rm on} \ll 1/G_{\rm off}$. Then the current is approximately given by

$$i \approx \frac{U_h}{R_{\rm on}} R_{\rm on} G_{\rm off} \left(\sqrt{\frac{1}{R_{\rm on} G_{\rm off}}} \cosh \lambda t + \sinh \lambda t \right).$$

For the numerical values given in the next section, the hyperbolic cosine term dominates. Therefore, the current starts with a nonvanishing value at $t = 0$ and increases slightly.

This current characteristics makes the design of the optimal power supply complicated.

2) Charging with Ramps: For leaky circuits it has been shown that the optimum input waveforms are rather complicated and would be hard to realize. However, linear ramps for the supply will still hold some advantage over the common static supplies. If such a linear ramp is used, the dissipated energy for charging the capacitor C up to a desired voltage V_H will be

$$E_1 = V_H^2 \left[\frac{R_{\rm on} C^2}{T_1} + R_{\rm on} G_{\rm off} C + \frac{1}{3} (R_{\rm on} G_{\rm off}^2 + G_{\rm off}) T_1 \right]. \quad (24)$$

This function will not find its minimal value when T will approach infinity. Instead, there is an optimal ramping time

$$T_{1opt} = C \sqrt{\frac{2R_{\rm on}}{R_{\rm on} G_{\rm off}^2 + G_{\rm off}}} \simeq C \sqrt{\frac{2R_{\rm on}}{G_{\rm off}}} \quad (25)$$

and thus a minimal achievable energy dissipation.

For discharging the capacitor the energy dissipation E_2 is a bit smaller, since the discharging current does not need to be delivered through the load resistor in a whole

$$E_2 = V_H^2 \left(\frac{R_{\rm on} C^2}{T_2} - R_{\rm on} G_{\rm off} C + \frac{1}{3} (R_{\rm on} G_{\rm off}^2 + G_{\rm off}) T_2 \right). \quad (26)$$

The optimum discharging time, therefore, is slightly longer

$$T_{2opt} = C \sqrt{\frac{3R_{\rm on}}{R_{\rm on} G_{\rm off}^2 + G_{\rm off}}} \simeq C \sqrt{\frac{3R_{\rm on}}{G_{\rm off}}}. \quad (27)$$

As can easily be derived from (25) and (27), the ratio between T_{1opt} and T_{2opt} is constant

$$\frac{T_{1opt}}{T_{2opt}} = \sqrt{\frac{2}{3}}. \quad (28)$$

If we use the optimum times both for charging and discharging, the minimum achievable power dissipation will be

$$E_{diss\ \rm min} = \sqrt{\frac{25}{18}}\, V_H^2 C \sqrt{R_{\rm on}(R_{\rm on} G_{\rm off}^2 + G_{\rm off})}. \quad (29)$$

All of these equations will only hold as long as $T \gg R_{\rm on} C$. So we see that energy dissipation can no longer be driven as close to zero as desired. This is, of course, due to the fact that, unlike in the case without leakage, there is static dissipation whenever the capacitor is loaded. Therefore, longer charging times will increase static dissipation, shorter charging times, on the other hand, dynamic dissipation.

Fig. 8 shows a final comparison between the development of power dissipation over charging time when using three different models for loading. Line a) shows the development for a classical leakless circuit. Note that the energy dissipation approaches zero as we increase T toward infinity. Line b) shows the curve for a leaky model when the optimal input waveforms described by (21) are used. This time we clearly see a saturation in the achievable minimum energy dissipation. Finally, line c) shows the development for linear ramps as predicted by (24). The curve shows a minimal value not far from the absolute minimum achievable by using the optimal waveforms, but then steadily increases again.

The circuit shown in Fig. 6 has been simulated using a SPICE level-6 model, which is rather detailed. Measurements have shown the on resistance of the transmission gate to be $R_{\rm on} \approx 3\,{\rm k}\Omega$, the off-conductance of a single NMOS transistor was $G_{\rm off} \approx 2$ pS. The load capacitance plus the parasitic capacitances of the NMOS transistor came to $C \approx 0.2$ pF. The capacitor was charged up to $V_H = 5$ V. For these values, extracted from an existing process, the resulting optimum ramping time is $T_{opt} \approx 12\ \mu$s with a minimum energy dissipation of $E_{V\ \rm min} \approx 1$ fJ per charge/discharge cycle.

Fig. 9 finally shows the simulation results as obtained from HSPICE and, as a comparison in a plain line without sample dots, the plot as predicted by (24) with the measured element values. The two lines do not differ much, the only major difference takes place for short times T where the condition $T \gg R_{\rm on} C$ does not hold any more. This shows clearly that the model of leak conductances describes the limits for adiabatic charging accurately and that the leak conductances are the major parasitic effect determining these limits. Even when complex circuits fabricated in other laboratories [2], [5] are regarded, the existence of an optimum charging time becomes obvious.

For any circuit, this optimum charging time can be found by measuring the three typical values $R_{\rm on}$, $G_{\rm off}$ and C.

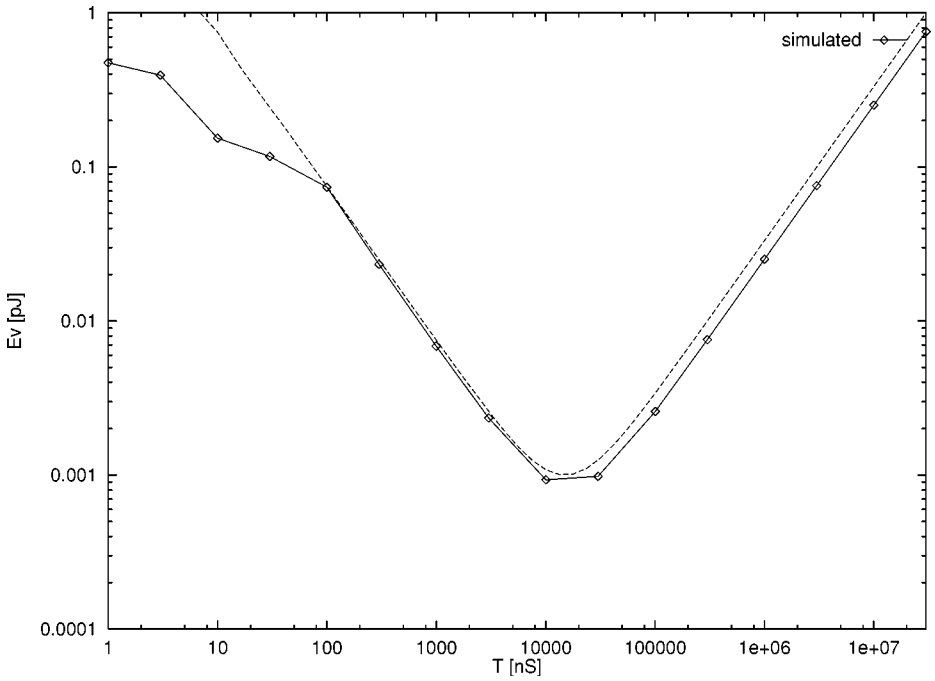

Fig. 9. Energy dissipation per charge/discharge cycle

V. Conclusion

In this paper we have shown how the optimal solution for charging a linear capacitor from a voltage source is computed. As a result, a superposition of a step and a ramp function yields the minimum for energy loss in the resistor. The computed input function is equivalent to driving the circuit from a constant current source. This is supposedly simpler to implement.

The usually applied voltage step function is the minimal time solution.

We have also computed the optimal charging voltage for a MOSFET gate capacitor. Now the input voltage is a rational function of time, but again, the voltage at the resistor is constant and so is the current. Therefore, also in this case a constant current source suffices to minimize the energy loss during charging.

If the unavoidable leak conductances in parallel to the capacitor to be charged are taken into account, it turns out that the optimal charging waveforms, though a linear model is used, are no longer simple ramps. Instead they are exponential functions. For this case even if optimal charging waveforms are used, the dissipated energy can no longer be made arbitrarily small, instead, a limit occurs.

If, despite this fact, linear ramps are used, care has to be taken to choose the correct charging time, since, after a minimal energy dissipation is achieved, if we keep on increasing the charging time the energy dissipation will increase again. The optimal charging time can be derived from three typical values for the charging process.

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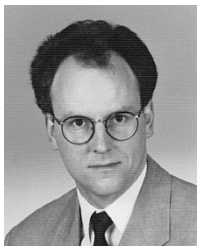

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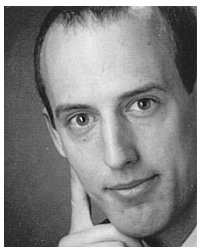

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