CHIPABROS

Team members:

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Akmal Hafizh Musyaffa
M. Azfar A. Yusup

Team background

- Academic Experience

  All of the members just finished 3rd Year as an Electrical Engineering Undergraduate with a basic to intermediate knowledge of ASIC and IC Design Open-Source tools

- Work Experience

  We implemented the layout for a complete RISC-V processor with integrated SRAM, leveraging the open-source sky130 PDK and a full toolchain of OpenLane and OpenRAM.

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Project information

- **Goal**
  We aim to extend the OSU library with **AOI33, OAI33, and MUX4** cells to improve area, delay, and routability in complex designs.
- **Design** - High Level Proposal
  MUX4 selects one of four inputs (x0,x1,x2,x3) based on control signals C0 and C1, outputting M.

  AOI33 computes y = ~((x0·x1·x2) + (x3·x4·x5)), combining two 3-input ANDs with a NOR.

  OAI33 computes y = ~((x0+x1+x2) · (x3+x4+x5)), combining two 3-input ORs with a NAND.

  Physical Design Note: For all gates, the Pull-up (PUN, using pMOS) and Pull-down (PDN, using nMOS) networks will be implemented as complementary CMOS duals to ensure correct logic operation and minimize static power.
- **Application**
  These cells are widely applied in control logic, arithmetic units, and multiplexing circuits to enable efficient and scalable digital designs.

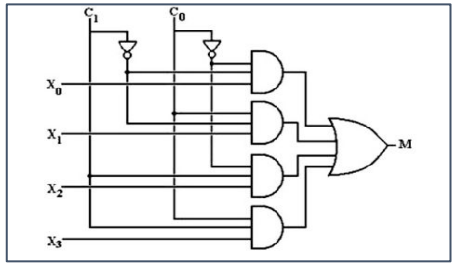

Figure 1 MUX4

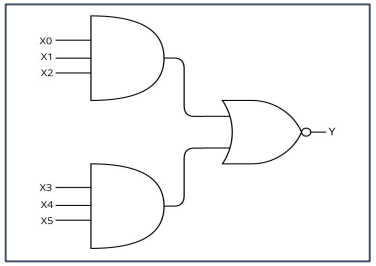

Figure 2 AOI33

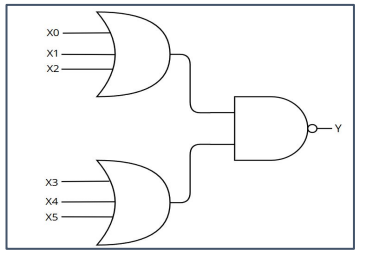

Figure 3 OAI33

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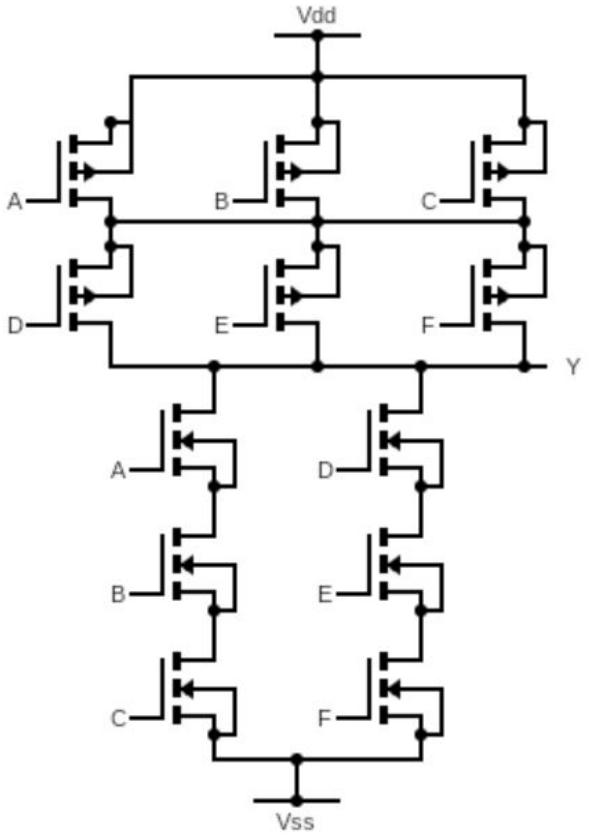

AND-OR-INVERT 3-3

Target Specification for AOI33

Parameter	Targeted Spec.
Drive Strength	1X
Track	9
VDD	3.3V
Input Capacitance	≤ 0.01 pF
Leakage Power	≤ 0.5 nW
Area	≤ 50 μm²
Delay @FO4	≤ 0.3 ns

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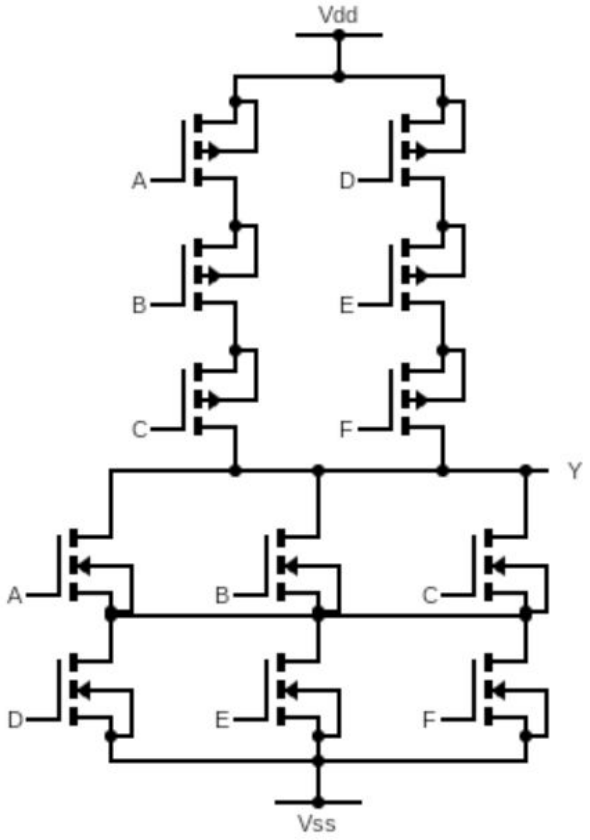

OR-AND-INVERT 3-3

Target Specification for OAI33

Parameter	Targeted Spec.
Drive Strength	1X
Track	9
VDD	3.3V
Input Capacitance	≤ 0.01 pF
Leakage Power	≤ 0.5 nW
Area	≤ 50 μm²
Delay @FO4	≤ 0.3 ns

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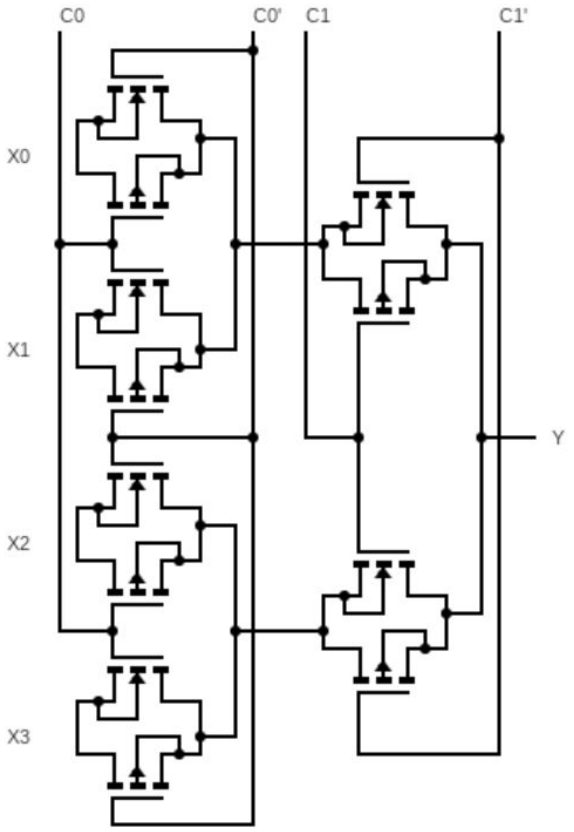

MUX4:1 (Transmission Gate Logic)

Target Specification for MUX4:1

Parameter	Targeted Spec.
Drive Strength	1X
Track	9
VDD	3.3V
Input Capacitance	≤ 0.01 pF
Leakage Power	≤ 0.5 nW
Area	≤ 60 μm²
Delay @FO4	≤ 0.3 ns

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Timeline :

Timeline Chipathon - CHIPABROS														
No	Task List		Phase 2		Phase 3			Phase 4						
			July		August					September				October
		Week	29	30	31	32	33	34	35	36	37	38	39	40
1	Schematic Design & Simulation													
2	Design Layout & DRC Verification + Post Layout Simulation													
3	Characterization													
4	Final Review & Submission													

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Work Distribution :

Member Name	Work Description
Karunia Kurniawan	AOI33 design schematic and layout
Muhammad Wijanarko	OAI33 design schematic and layout
Akmal Musyaffa	MUX4:1 design schematic and layout
Muhammad Yusup	MUX4:1 design schematic and layout

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Reference :

- https://www.researchgate.net/publication/257799438_High_performance_low_power_200_Gbs_41_MUX_with_TGL_in_45_nm_technology
- https://gf180mcu-pdk.readthedocs.io/en/latest/digital/standard_cells/gf180mcu_fd_sc_mcu9t5v0/index.html
- https://courses.cs.washington.edu/courses/cse370/03sp/pdfs/lectures/lecture10.pdf#:~:text=AND,2x2%20AOI%20%2B%20symbol
- https://www.ijirset.com/upload/2015/ncetas15/23_P_ID_31.pdf#:~:text=,power%20consumption%20and%20minimum%20delay

Our Repo :

- https://github.com/azfaray/chipathon_chipabros.git

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