Hardware Circuit Design of Multi-frequency LeNet-5 Convolutional Neural Network

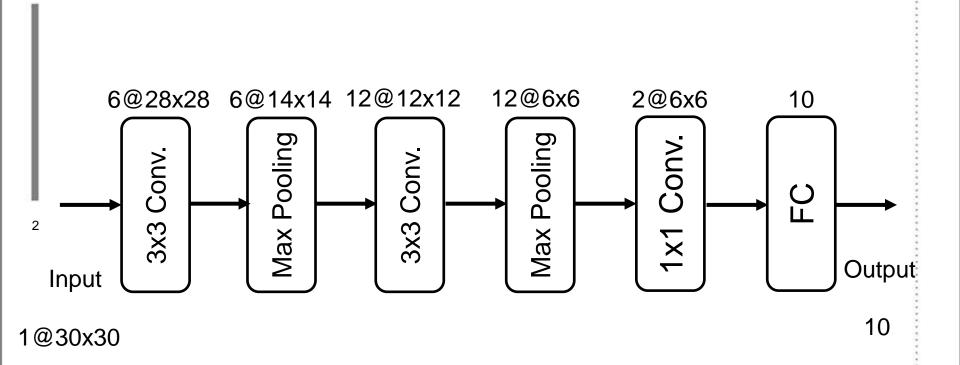
多頻率改良式LeNet-5

卷積神經網路之硬體電路設計





Introduction





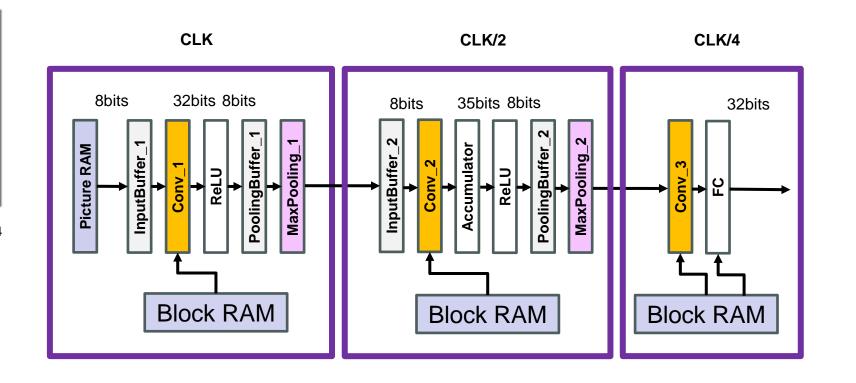


Introduction

Layer Type	Output Feature Map Size	Number of Parameters
Convolution 1	28×28×6	(3×3×6) + 6
Subsampling 1	14×14×6	-
Convolution 2	12×12×12	(6×3×3×12) + 12
Subsampling 2	6×6×12	-
Convolution 3	6×6×2	(12×1×1×2) + 2
Fully-Connected	10	(72×10) + 10







Pipeline

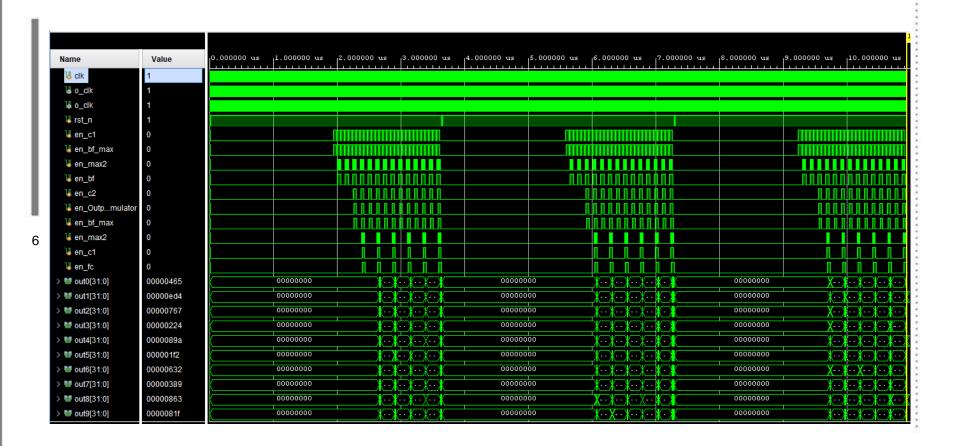
Layer1						Layer2				Layer3	
Rst_n Load_Weigh	Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	Accumulater	Pooling_Buffer_2	MaxPooling_2	Conv_3	FC
Rst_n Load_Weight		Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	Accumulater	Pooling_Buffer_2	MaxPooling_2	Conv_3
Rst_n Load_Weight			Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	Accumulater	Pooling_Buffer_2	MaxPooling_2
Rst_n Load_Weight				Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	Accumulater	Pooling_Buffer_2
Rst_n Load_Weight					Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	Accumulater
Rst_n Load_Weight						Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2
Rst_n Load_Weight							Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2
Rst_n Load_Weight								Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1
Rst_n Load_Weight									Input_Buffer_1	Conv_1	Pooling_Buffer_1

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												:
In	put_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	Accumulater	Pooling_Buffer_2	MaxPooling_2	Conv_3	FC	:
		Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	Accumulater	Pooling_Buffer_2	MaxPooling_2	Conv_3	:
			Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	Accumulater	Pooling_Buffer_2	MaxPooling_2	:
				Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	Accumulater	Pooling_Buffer_2	:
					Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	Accumulater	:
						Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	Conv_2	-
							Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	Input_Buffer_2	3
								Input_Buffer_1	Conv_1	Pooling_Buffer_1	MaxPooling_1	3
									Input_Buffer_1	Conv_1	Pooling_Buffer_1	:



Waveform





change after implementation.

Not Specified

Results

Process:

typical

Power Budget Margin: N/A Junction Temperature: 28.9°C

Thermal Margin: 56.1°C (4.7 W)

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or

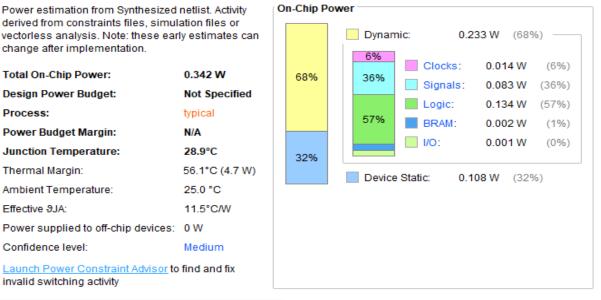
Ambient Temperature: 25.0 °C Effective 9JA: 11.5°C/W

Power supplied to off-chip devices: 0 W

Confidence level: Medium

Launch Power Constraint Advisor to find and fix invalid switching activity

Resource	Estimation	Available	Utilization %
LUT	69422	53200	130.49
LUTRAM	226	17400	1.30
FF	24102	106400	22.65
Ю	330	125	264.00
BUFG	3	32	9.38



create_clock -period 26.000 -name clk_26ns -waveform {0.000 13.000} [get_ports clk]

Setup	Hold		Pulse Width			
Worst Negative Slack (WNS):	0.380 ns	Worst Hold Slack (WHS):	NA	Worst Pulse Width Slack (WPWS):	12.020 ns	
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	NA	Total Pulse Width Negative Slack (TPWS):	0.000 ns	
Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA	Number of Failing Endpoints:	0	
Total Number of Endpoints:	39997	Total Number of Endpoints:	NA	Total Number of Endpoints:	20182	

Max _ Frequency: 39MHz



