ENGLISH

University of South-Eastern Norway

EXAMINATION INFORMATION PAGE

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Subject code: DDV3101	Subject name: DATAMASKINARKITEKTUR OG VHDL PROGRAMMERING	
Responsible subject teacher: HIEU NGUYEN	Campus: KONGSBERG	Faculty: TNM
Assignment given in WISEflow (date and time):	Submission time in WISEflow (date and time):	
No. of assignments: 8	No. of attachments: 0	No. of pages incl. front page and attachments: 5

Aids and collaboration:

Permitted aids: All aids are allowed.

	Yes	No
Is it an individual exam?	☒	☐
Is it allowed to collaborate with other persons?	☐	☒

If yes, explain the extend of permitted cooperation. In Comments to USN Regulations, illegal collaboration is defined as collaboration leading to text similarity in answers or giving one or both students unfair advantage in the exam situation.

Description of individual examination and illegal cooperation will be found at my.usn.no

Criteria for the answers:

Font type:	Font size:	Line spacing:
No. of words (min/max):	Maximum no. of pages excl. front page and attachments:	

Source reference:
Not required

Other important information:

THE CANDIDATE MUST CHECK THAT THE ASSIGNMENT SET IS COMPLETE

Question 01

The current trend in designing computer systems is to utilize multiple processors per chip rather than a faster uniprocessor.

a. Use the Dennard scaling law to explain this trend partly.

b. Is there any upper limit to performance improvement due to multiple processors per chip?

Question 02

"A few decades ago, the term architecture generally referred to only instruction set design" (Hennessy and Patterson, page 12). Explain why this is no longer correct by giving another design factor that influences today's computer systems' performance.

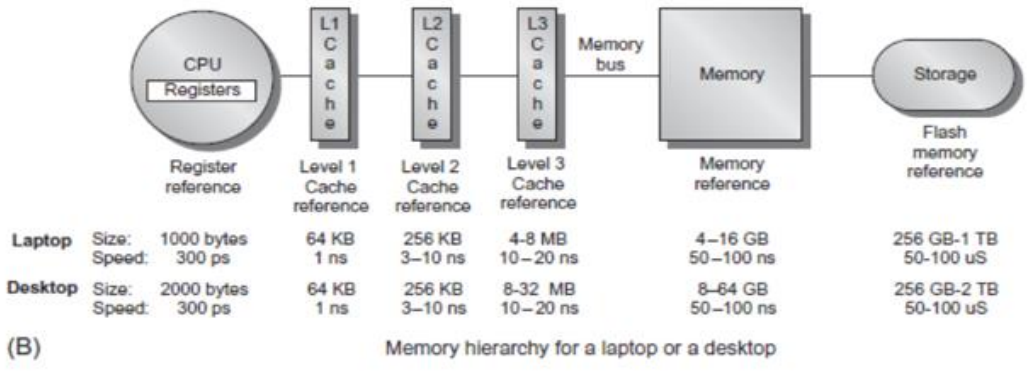
Question 03

a. What is the memory hierarchy?

b. The below figure is the memory hierarchy for a desktop/laptop. What are the benefits of this memory hierarchy in terms of speed and capacity?

c. Why should multiple cache layers be used?

d. How many total bits are required for a direct-mapped cache with 32 KiB of data and 4-word blocks, assuming a 32-bit address?



(B) Memory hierarchy for a laptop or a desktop

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Question 04

a. What is the instruction pipeline?

b. Is it correct that the executive time is shortened four times if the instruction pipeline has a depth of 4 stages?

c. Explain why a data hazard happens during the execution of the following two successive instructions

```
Sub $s1, $t0, $t1
Add $t2, $t3, $s1
```

d. How many stall cycles occur in this case?

e. Using graphical representation to show the forwarding technique can avoid data hazard.

f. Why is the fixed-length instruction preferred when it comes to the instruction pipeline?

Question 05

a. Where do the hazards happen with the following successive instructions?

b. Reorder to avoid the hazards and indicate how many cycles does it take to complete these instructions.

```
lw $t2, 4($t0)
add $t3, $t1, $t2
sw $t3, 12($t0)
lw $t4, 8($t0)
sub $t5, $t1, $t4
sw $t5, 16($t0)
```

Question 06

In this question, students use the flow design to design the one-bit full adder

a. Set up the truth table(s)

b. Find the simplified Boolean expression for the outputs

c. Develop VHDL code to implement the Boolean expressions in part b)

d. Develop a test bench to test the design in part c

Question 07

In this question, students use the "when-else" syntax to design the combinational circuit whose function is defined by the truth table below:

X (2 downto 0) (Input)	Y (1 downto 0) (Ouput)
000	11
001	11
010	01
011	01
100	00
101	00
110	10
111	11

Question 08

The below figure gives the state diagram of the finite state machine for the rising-edge detection.

a. What type of finite state machine is it?

b. Modify the diagram to detect the falling-edge of the input signal.

c. Write VHDL code to model the finite state machine to detect the falling-edge of the input signal.

d. Combine your falling edge detector with the mod-m counter and hex2seg circuit to build a test circuit. Students should include the source codes and schematic picture of the test circuit generated from the Vivado Xilinx IDE.