ELEC 334 - MICROPROCESSORS

PROJECT 1 – RANDOMIZED COUNTER

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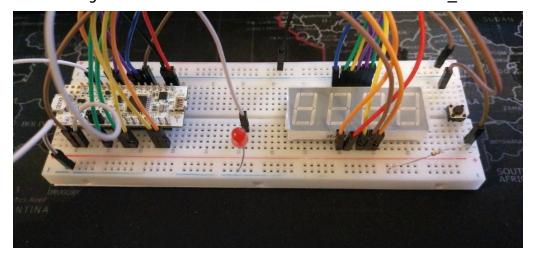
1 Intorduction

1.1 Briefing

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1.2 Objective

This project is developed on a STM32G031K8T NUCLEO BOARD. The Arm Cortex-M0+ architecture gained functionality with "asm.s" file developed with assembly language. The aim of the Project is to understand and gain a brief knowledge about ARM Cortex-M0+, how the pins work and put a general knowledge how instructions work.

2 Technical Aspects

2.1 Materials

Material	Price
Breadboard x1	8,84 TL
Jumper x40	3.72 TL
390R Resistor x1	0,03 TL
4x Seven Segment Display x1	7,45 TL
STM32G031K8 x1	137,59 TL
5mm LED Red x1	0,19 TL
Tactile Switch x1	0,28 TL

2.2 Method

The system supports 3 different button press type, which we will cover further into the section. Program will display 0000 on the 4 digit 7 segment display for a second. After that program will be on a loop. In this loop board will display 4005 on 4 digit 7 segment display and check for button interrupt. If the button is pressed. It will start the countdown from 9000 for the first countdown. In every step of countdown the program will generate a random number on the r7 register. After the countdown the random number will be displayed and will be saved into the responsible registers. Lastly if the pressed again in the countdown the program will paused until a further interrupt.

- Display 0000 on the segment display for a second.
- Display 4005 on the segment display until the button pressed.
- If the button pressed start the countdown from 9000 and display every number on the segment display.
- If the button pressed stop the countdown and display the number that stopped. After that wait for an another interrupt fort o contiune.
- After the countdown display the random number for 1 second.
- Display 0000 for a second and wait for an interrupt again and this the countdown starts from the random number generated by the board.

2.2.1 Random Number Algorithm

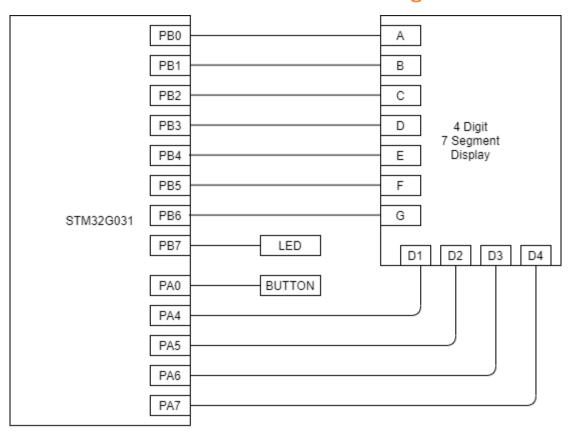
We used the Pseudo Code Random Number Generator algorithm which depends on several elements. The formula we will use:

$$next = (next * a + c) mod m$$

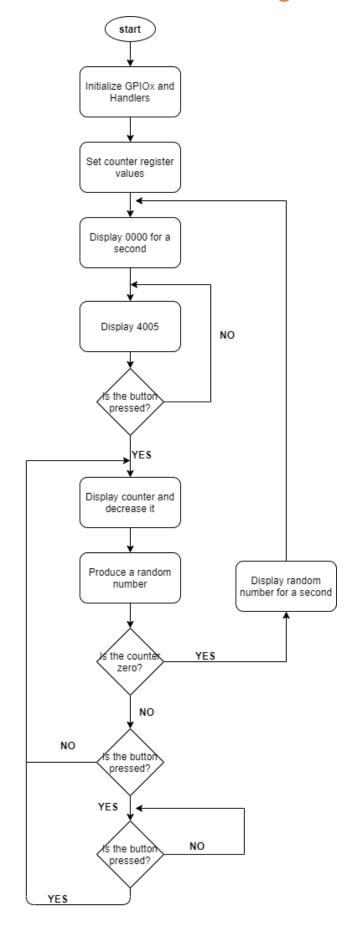
This formula will produce a number from 0 to 8999. After the countdown we add 1000 to number to maket this a number between 1000 and 9999.

2.3 Diagrams

2.3.1 Hardware Block Diagram



2.3.2 Software Block Diagram



3 Output

https://youtu.be/DPQuOiU-mz8

4 Conclusion

This project showed us a crucial points such as code length, data handling, register managment, bitwise module handling and problem solving.

Lets break it down and pieces shall we? First of all it was a great way to understand our C code that we programed on previous assignments. We had a chance to inspect how our code will work on machine wise and how it can be handled in different ways.

On the register handling part we learned how to preserve and manage our data for our usage. Since it is so easy to lose data that could be used in further instructions, it is important to store them in a good manner.

For code length we found clever methods fill the stack completely by shortening some parts but sacrificing readability. It can backfire for different readers but it efficient to shorten them.

Last setback that we faced is bitwise module activation. Putting right addresses and values into the registers played an important role on this process.

5 Appendix

```
6
     * project1.s
7
8
9
     * author: Aziz Can Akkaya
10
     * number: 171024005
11
12
13
     .syntax unified
14
     .cpu cortex-m0plus
15
     .fpu softvfp
16
     .thumb
17
18
19
    /* make linker see this */
    .global Reset_Handler
20
21
    /* get these from linker script */
22
    .word _sdata
23
24
     .word _edata
25
     .word _sbss
26
     .word _ebss
27
28
29
     /* define peripheral addresses from RM0444 page 57, Tables 3-4 */
                    (0x40021000) // RCC base address
     .equ RCC_BASE,
30
                           (RCC_BASE + (0x34)) // RCC IOPENR register offset
31
     .equ RCC_IOPENR,
32
33
     .equ GPIOC BASE,
                           (0x50000800)
                                                // GPIOC base address
     .equ GPIOC MODER,
                           (GPIOC_BASE + (0x00)) // GPIOC MODER register offset
34
                           (GPIOC_BASE + (0x14)) // GPIOC ODR register offset
35
     .equ GPIOC_ODR,
36
37
     .equ GPIOA_BASE,
                         (0x50000000)
                                                    //GPIOA base address
     .equ GPIOA_MODER,
                         (GPIOA BASE + (0x00)) //GPOIA MODER reigster offset
38
     .equ GPIOA_ODR,
39
                               (GPIOA\_BASE + (0x14))
                                                          //GPIOA ODR register
     offset
                               (GPIOA_BASE + (0X10))
40
     .equ GPIOA_IDR,
                                                        //GPIOA IDR register
     offset
41
                        (0x50000400)
42
     .equ GPIOB BASE,
                                                    //GPIOB base address
                         (GPIOB BASE + (0x00)) //GPIOB MODER register offset
43
     .equ GPIOB MODER,
                               (GPIOB BASE + (0x14)) //GPIOB ODR register
44
     .equ GPIOB ODR,
     offset
45
                                (1000) //delay value
46
     .equ leddelay,
47
48
                                             //a value for random code generator
                   (11035)
     .equ a,
49
     .equ c,
                   (12345)
                                            //c value for random code generator
50
                                      //m value for random come generator
     .equ m,
                   (9000)
51
                   (0x40)
52
     .equ ZERO,
                                      //4-digit SSD pin set for GPIOA, nummber 0
53
     .equ ONE,
                   (0x79)
                                      //4-digit SSD pin set for GPIOA, nummber 1
54
     .equ TWO,
                   (0x24)
                                      //4-digit SSD pin set for GPIOA, nummber 2
55
     .equ THREE,
                                     //4-digit SSD pin set for GPIOA, nummber 3
                   (0x30)
                                     //4-digit SSD pin set for GPIOA, nummber 4
56
     .equ FOUR,
                   (0x19)
                                     //4-digit SSD pin set for GPIOA, nummber 5
57
     .equ FIVE,
                   (0x12)
```

```
58
                                       //4-digit SSD pin set for GPIOA, nummber 6
     .equ SIX,
                    (0x02)
59
                                       //4-digit SSD pin set for GPIOA, nummber 7
     .equ SEVEN,
                    (0x78)
60
     .equ EIGHT,
                    (0x00)
                                       //4-digit SSD pin set for GPIOA, nummber 8
61
     .equ NINE,
                    (0x10)
                                       //4-digit SSD pin set for GPIOA, nummber 9
62
63
     /* vector table, +1 thumb mode */
64
65
     .section .vectors
     vector table:
66
                                /*
67
      .word estack
                                        Stack pointer */
                                /*
68
      .word Reset Handler +1
                                        Reset handler */
      .word Default Handler +1 /*
                                     NMI handler */
69
      .word Default_Handler +1 /* HardFault handler */
70
71
      /* add rest of them here if needed */
72
73
74
     /* reset handler */
75
     .section .text
76
     Reset_Handler:
77
     /* set stack pointer */
78
      ldr r0, =_estack
79
      mov sp, r0
80
81
      /* initialize data and bss
      * not necessary for rom only code
82
      * */
83
      bl init_data
84
85
      /* call main */
86
      bl main
87
      /* trap if returned */
88
      b.
89
90
91
     /* initialize data and bss sections */
92
     .section .text
93
     init_data:
94
95
      /* copy rom to ram */
      ldr r0, =_sdata
ldr r1, =_edata
96
97
98
      ldr r2, =_sidata
99
      movs r3, #0
100
      b LoopCopyDataInit
101
102
      CopyDataInit:
             ldr r4, [r2, r3]
103
             str r4, [r0, r3]
104
105
             adds r3, r3, #4
106
107
      LoopCopyDataInit:
108
             adds r4, r0, r3
             cmp r4, r1
109
110
             bcc CopyDataInit
111
      /* zero bss */
112
113
      ldr r2, =_sbss
      ldr r4, =_ebss
114
      movs r3, #0
115
116
      b LoopFillZerobss
```

```
117
118
      FillZerobss:
119
            str r3, [r2]
120
             adds r2, r2, #4
121
122
      LoopFillZerobss:
123
             cmp r2, r4
124
             bcc FillZerobss
125
126
    bx lr
127
128
129 /* default handler */
130 .section .text
131 Default Handler:
132
      b Default_Handler
133
134
135 /* main function */
136 .section .text
137 main:
138
      /* enable GPIOC clock, bit2 on IOPENR */
      ldr r6, =RCC_IOPENR
139
      ldr r5, [r6]
140
      /* movs expects imm8, so this should be fine */
141
142
      movs r4, 0x3
      orrs r5, r5, r4
143
144
      str r5, [r6]
145
      //GPIOA PIN SET FOUR OUTPUT
146
      ldr r6, =GPIOA_MODER
147
      ldr r5, [r6]
148
149
      movs r4, 0xFF
150
      lsls r4, r4, #8
151
      bics r5, r5, r4
152
153
      movs r4, 0x55
      lsls r4, r4, #8
154
155
      orrs r5, r5, r4
156
      ldr r4, =0xFFFFFFFC
157
      ands r5, r5, r4
158
      str r5,[r6]
159
      //GPIOB PIN SET FOR OUTPUT
160
      ldr r6, =GPIOB_MODER
161
      ldr r5, [r6]
      1dr r4, =0x5555
162
      ands r5, r5, r4
163
      str r5, [r6]
164
      //GPIOA PIN SET FOR INPUT
165
      ldr r6, =GPIOA_IDR
166
      ldr r5, [r6]
167
168
      1dr r4, =0x1
169
      ands r5, r5, r4
170
      str r5, [r6]
171
      //COUNTER REGISTER SET
172
      movs r0, #9
      movs r1, #0
173
174
      movs r2, #0
175
      movs r3, #0
```

```
176
177
    //Setting delay
178 set1:
179
      ldr r7, =1000000
180 //diplay 0000 on the ssd for 1 second
181 start_loop:
      ldr r6, = GPIOB_ODR
182
183
      ldr r5, [r6]
184
      movs r4, ZERO
185
      orrs r5, r5, r4
186
      str r5, [r6]
187
188
      subs r7, r7, #1
      ldr r6, = GPIOA\_ODR
189
      ldr r5, [r6]
190
191
      movs r4, 0xF0
192
      orrs r5, r5, r4
193
      str r5, [r6]
194
195
      ldr r4, =0
196
      cmp r7, r4
197
      bne start_loop
198 //clear output values
199 clear:
      ldr r6, = GPIOA_ODR
200
      ldr r5, [r6]
201
202
      movs r4, 0x00
203
      ands r5, r5, r4
204
      str r5, [r6]
205
206
      ldr r6, =GPIOB_ODR
207
      ldr r5, [r6]
208
      movs r4, 0x00
      ands r5, r5, r4
209
210
      str r5, [r6]
211
      //b countdown
212 //button check
213
     button:
214
      bl id mod
215
      ldr r6, =GPIOA_IDR
216
         ldr r5, [r6]
217
         1dr r4, =0x1
218
         ands r5, r5, r4
219
      cmp r5, #1
220
      beq countdown
221
222
     //id display (4005) if the button is not pressed
223
     id_mod:
      push {lr}
224
225
      //D1 OUTPUT
226
      ldr r6, = GPIOB_ODR
227
      ldr r5, [r6]
228
      movs r4, FOUR
229
      orrs r5, r5, r4
230
      str r5, [r6]
231
232
      ldr r6, = GPIOA_ODR
      ldr r5, [r6]
233
234
      movs r4, 0x10
```

```
235
      orrs r5, r5, r4
236
      str r5, [r6]
237
238
      ldr r4, =leddelay
239
240 delay5:
      subs r4, r4, #1
241
242
      bne delay5
243
      //CLEAR PINS
244
      ldr r6, = GPIOA_ODR
245
      ldr r5, [r6]
246
      movs r4, 0x00
247
      ands r5, r5, r4
248
      str r5, [r6]
249
      ldr r6, =GPIOB_ODR
250
251
      ldr r5, [r6]
252
      movs r4, 0x00
253
      ands r5, r5, r4
254
      str r5, [r6]
255
      //D2 and D3 OUTPUT
256
      ldr r6, = GPIOB_ODR
      ldr r5, [r6]
257
258
      movs r4, ZERO
      orrs r5, r5, r4
259
      str r5, [r6]
260
261
262
      ldr r6, = GPIOA\_ODR
263
      ldr r5, [r6]
264
      movs r4, 0x60
265
      orrs r5, r5, r4
266
      str r5, [r6]
267
268
      ldr r4, =leddelay
269
270 delay7:
271
      subs r4, r4, #1
      bne delay7
272
273
      //CLEAR PINS
274
      ldr r6, = GPIOA\_ODR
275
      ldr r5, [r6]
276
      movs r4, 0x00
277
      ands r5, r5, r4
278
      str r5, [r6]
279
      ldr r6, =GPIOB_ODR
280
      ldr r5, [r6]
281
282
      movs r4, 0x00
      ands r5, r5, r4
283
      str r5, [r6]
284
285
      //D4 OUTPUT
      ldr r6, = GPIOB_ODR
286
287
      ldr r5, [r6]
288
      movs r4, FIVE
289
      orrs r5, r5, r4
290
      str r5, [r6]
291
      ldr r6, = GPIOA\_ODR
292
293
      ldr r5, [r6]
```

```
294
      movs r4, 0x80
      orrs r5, r5, r4
295
296
      str r5, [r6]
297
298
      ldr r4, =leddelay
299
300 delay8:
301
    subs r4, r4, #1
302
      bne delay8
303
304
      ldr r6, = GPIOA_ODR
305
      ldr r5, [r6]
306
      movs r4, 0x00
      ands r5, r5, r4
307
308
      str r5, [r6]
309
310
      ldr r6, =GPIOB_ODR
311
      ldr r5, [r6]
312
      movs r4, 0x00
313
      ands r5, r5, r4
314
      str r5, [r6]
315
      pop {pc}
316
317 //if the button pressed in start it will lead to this point
318 countdown:
      bl button_check
319
320
      bl check
      bl led on
321
322
      bl display
323
     bl random
324
     //check and decrase control for units digit
325 cmp r3, #0
326 beq decrease_ten
327
      subs r3, r3, #1
328
     b countdown
329
330 decrease_ten:
     //check and decrase control for tens digit
331
332
      movs r3, #9
333
      cmp r2, #0
334
      beq decrease_hundred
335
      subs r2, r2, #1
336
      b countdown
337
338 decrease hundred:
      //check and decrase control for hundreds digit
339
340
      movs r2, #9
341
      cmp r1, #0
342
      beq decrease_thousand
343
      subs r1, r1, #1
344
      b countdown
345
346 decrease_thousand:
    //check and decrase control for thousands digit
347
348
      movs r1, #9
349
      cmp r0, #0
350
      beq show1
351
      subs r0, r0, #1
352
      b countdown
```

```
353
354
     //button check for pause
355
     button_check:
356
      push {lr}
357
      ldr r6, =GPIOA_IDR
         ldr r5, [r6]
358
359
         1dr r4, =0x1
360
         ands r5, r5, r4
361
      cmp r5, #1
362
      beg pause
363
      pop {pc}
364
365
    //pause loop, it will wait for an another press
366 pause:
      bl display
367
368
      bl led_on
369
      ldr r6, =GPIOA_IDR
         ldr r5, [r6]
370
371
         1dr r4, =0x1
372
         ands r5, r5, r4
373
      cmp r5, #1
374
      bne pause
375
      pop {pc}
376
377 show1:
      ldr r6, =0
378
      ldr r4, =1000
379
      adds r7, r7, r4
380
381
      movs r5, r7
382
      cmp r5, r4
383
      bgt mod1
384
385 show2:
386
      //setting up thousands value
387
      movs r0, r6
388
      ldr r6, =0
389
      ldr r4, =100
390
      cmp r5, r4
391
      bgt mod2
392
393 show3:
394
      //setting up hundreds value
395
      movs r1, r6
396
      ldr r6, =0
397
      ldr r4, =10
398
      cmp r5, r4
399
      bgt mod3
400
401 show4:
402
      //setting up tens value
403
      movs r2, r6
404
      ldr r6, =0
405
      ldr r4, =1
406
      cmp r5, r4
407
      bgt mod4
408
409 show5:
410
      //setting up units value
411
      movs r3, r6
```

```
412
      1dr r7, =1000
413
      b display_result
414
415 display_result:
416
      //displaying result for a second
417
      bl led_off
418
      bl display
419
      subs r7, r7, #1
420
      ldr r4, =0
421
      cmp r7, r4
422
      bne display_result
423
      b set1
424
425 //general modding function for every digits
426 mod1:
      subs r5, r5, r4
427
      adds r6, r6, #1
428
      cmp r5, r4
429
430
      bge mod1
431
      b show2
432
433 mod2:
434
      subs r5, r5, r4
435
      adds r6, r6, #1
436
      cmp r5, r4
437
      bge mod2
438
      b show3
439
440
441 mod3:
442 subs r5, r5, r4
443 adds r6, r6, #1
444
    cmp r5, r4
445
      bge mod3
446
      b show4
447
448 mod4:
449
      subs r5, r5, r4
450
      adds r6, r6, #1
451
      cmp r5, r4
452
      bge mod4
453
      b show5
454
455 //random generator
456 random:
457
      push {lr}
458
      ldr r4, =a
459
      //next*a
      muls r7, r7, r4
460
461
      1dr r4, =c
      //next*a + c
462
      adds r7, r7, r4
463
464
      //mod m
465
      1dr r4, = m
466
      cmp r7, r4
467
      bgt mod
468
      pop {pc}
469
470 mod:
```

```
471
      subs r7, r7, r4
472
      cmp r7, r4
473
      bge mod
474
      pop {pc}
475
476 //checking if all the digits is 0 or not for the counter
477
    check:
478
     push {lr}
479
      cmp r0, #0
480
      beg check1
481
      pop {pc}
482
483 check1:
      cmp r1, #0
484
485
      beq check2
486
      pop {pc}
487
488 check2:
489
     cmp r2, #0
490
      beq check3
491
      pop {pc}
492
493 check3:
      cmp r3, #0
494
495
      beg show1
496
      pop {pc}
497
498
    //led on function
499 led_on:
500
      push {lr}
501
      ldr r6, = GPIOB_ODR
502
      ldr r5, [r6]
503
      movs r4, 0x80
504
      orrs r5, r5, r4
505
      str r5, [r6]
506
      pop {pc}
507
508 //led off function
509 led off:
510
      push {lr}
511
      ldr r6, = GPIOB_ODR
512
      ldr r5, [r6]
513
      movs r4, 0x00
514
      orrs r5, r5, r4
515
      str r5, [r6]
516
      pop {pc}
517
518 //switch case for to set r0 value
519
    d1:
      push {lr}
520
521
         cmp r0, #0
522
         beq zero
523
524
         cmp r0, #1
525
         beq one
526
527
      cmp r0, #2
528
         beq two
529
```

```
530
      cmp r0, #3
531
         beq three
532
      cmp r0, #4
533
534
         beq four
535
536
      cmp r0, #5
537
         beq five
538
      cmp r0, #6
539
540
         beq six
541
542
      cmp r0, #7
543
         beq seven
544
545
         cmp r0, #8
546
         beq eight
547
548
         cmp r0, #9
549
         beq nine
550
551
    //switch case for to set r1 value
552 d2:
553
      push {lr}
554
         cmp r1, #0
555
         beq zero
556
557
         cmp r1, #1
558
         beq one
559
      cmp r1, #2
560
         beq two
561
562
563
      cmp r1, #3
564
         beq three
565
      cmp r1, #4
566
567
         beq four
568
      cmp r1, #5
569
570
         beq five
571
572
      cmp r1, #6
573
         beq six
574
575
      cmp r1, #7
576
         beq seven
577
         cmp r1, #8
578
579
         beq eight
580
581
         cmp r1, #9
582
         beq nine
583
584
    //switch case for to set r2 value
585 d3:
586
      push {lr}
587
         cmp r2, #0
588
         beq zero
```

```
589
590
         cmp r2, #1
591
         beq one
592
593
      cmp r2, #2
594
         beq two
595
      cmp r2, #3
596
597
         beq three
598
599
      cmp r2, #4
         beq four
600
601
      cmp r2, #5
602
603
         beq five
604
      cmp r2, #6
605
606
         beq six
607
608
      cmp r2, #7
609
         beq seven
610
         cmp r2, #8
611
         beq eight
612
613
         cmp r2, #9
614
615
         beq nine
616
    //switch case for to set r4 value
617
618 d4:
619
      push {lr}
620
         cmp r3, #0
621
         beq zero
622
623
         cmp r3, #1
624
         beq one
625
626
      cmp r3, #2
627
         beq two
628
629
      cmp r3, #3
630
         beq three
631
632
      cmp r3, #4
633
         beq four
634
      cmp r3, #5
635
         beq five
636
637
      cmp r3, #6
638
639
         beq six
640
      cmp r3, #7
641
642
         beq seven
643
         cmp r3, #8
644
645
         beq eight
646
647
         cmp r3, #9
```

```
648
        beq nine
649
650 //setting values for GPIOA pin output
651 zero:
652
    movs r4, ZERO
653
      pop {pc}
654
655 one:
656 movs r4, ONE
657
      pop {pc}
658
659 two:
    movs r4, TWO
660
661
      pop {pc}
662
663 three:
664 movs r4, THREE
665
    pop {pc}
666
667 four:
668 movs r4, FOUR
669 pop {pc}
670
671 five:
    movs r4, FIVE
672
673
     pop {pc}
674
675 six:
676 movs r4, SIX
        pop {pc}
677
678
679 seven:
680 movs r4, SEVEN
681
        pop {pc}
682
683 eight:
684 movs r4, EIGHT
        pop {pc}
685
686
687 nine:
688 movs r4, NINE
689
    pop {pc}
690
691 //digit display function
692 display:
693
     push {lr}
     ldr r6, = GPIOA_ODR
694
     ldr r5, [r6]
695
696
      movs r4, 0x10
      orrs r5, r5, r4
697
698
      str r5, [r6]
699
      ldr r6, = GPIOB\_ODR
700
701
      ldr r5, [r6]
702
      bl d1
      orrs r5, r5, r4
703
704
      str r5, [r6]
705
706
      ldr r4, =leddelay
```

```
707
708
    delay1:
709
      subs r4, r4, #1
710
      bne delay1
711
      ldr r6, = GPIOA_ODR
712
713
      ldr r5, [r6]
714
      movs r4, 0x00
      ands r5, r5, r4
715
716
      str r5, [r6]
717
      ldr r6, = GPIOB_ODR
718
719
      ldr r5, [r6]
720
      movs r4, 0x00
      ands r5, r5, r4
721
722
      str r5, [r6]
723
724
      ldr r6, = GPIOA\_ODR
725
      ldr r5, [r6]
726
      movs r4, 0x20
727
      orrs r5, r5, r4
728
      str r5, [r6]
729
730
      ldr r6, = GPIOB_ODR
      ldr r5, [r6]
731
732
      bl d2
      orrs r5, r5, r4
733
734
      str r5, [r6]
735
736
      ldr r4, =leddelay
737
738 delay2:
739
      subs r4, r4, #1
740
      bne delay2
741
742
      ldr r6, = GPIOA_ODR
743
      ldr r5, [r6]
744
      movs r4, 0x00
745
      ands r5, r5, r4
746
      str r5, [r6]
747
748
      ldr r6, = GPIOB_ODR
749
      ldr r5, [r6]
750
      movs r4, 0x00
751
      ands r5, r5, r4
      str r5, [r6]
752
753
      ldr r6, = GPIOA\_ODR
754
      ldr r5, [r6]
755
756
      movs r4, 0x40
757
      orrs r5, r5, r4
758
      str r5, [r6]
759
760
      ldr r6, = GPIOB_ODR
761
      ldr r5, [r6]
762
      bl d3 //movs r4, data
763
      orrs r5, r5, r4
764
      str r5, [r6]
765
```

```
766
      ldr r4, =leddelay
767
768
    delay3:
      subs r4, r4, #1
769
770
      bne delay3
771
      ldr r6, = GPIOA\_ODR
772
773
      ldr r5, [r6]
774
      movs r4, 0x00
775
      ands r5, r5, r4
776
      str r5, [r6]
777
778
      ldr r6, = GPIOB_ODR
779
      ldr r5, [r6]
      movs r4, 0x00
780
      ands r5, r5, r4
781
782
      str r5, [r6]
783
      ldr r6, = GPIOA\_ODR
784
785
      ldr r5, [r6]
786
      movs r4, 0x80
787
      orrs r5, r5, r4
788
      str r5, [r6]
789
790
      ldr r6, = GPIOB_ODR
791
      ldr r5, [r6]
792
      bl d4
793
      orrs r5, r5, r4
794
      str r5, [r6]
795
796
      ldr r4, =leddelay
797
798 delay4:
799
      subs r4, r4, #1
800
      bne delay4
801
      ldr r6, = GPIOA_ODR
802
803
      ldr r5, [r6]
      movs r4, 0x00
804
805
      ands r5, r5, r4
806
      str r5, [r6]
807
      ldr r6, = GPIOB_ODR
808
809
      ldr r5, [r6]
810
      movs r4, 0x00
811
      ands r5, r5, r4
      str r5, [r6]
812
             pop {pc}
813
814
815
```

6 References

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