```
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       //3/29/23
//EE469 Lab1
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       //This module tests the ALU module against a given set of test vectors.
 8
      module alu_testbench();
           logic [103:0] testvectors [1000:0]; logic [31:0] a, b, Result; logic [3:0] ALUFlags; logic [1:0] ALUControl; logic clk;
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15
           alu dut (.a(a), .b(b), .ALUControl(ALUControl), .Result(Result), .ALUFlags(ALUFlags));
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           parameter CLOCK_PERIOD = 100;
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           //clock setup
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           initial clk = 1;
           always begin
               #(CLOCK_PERIOD /2);
               c1k = \sim c1k;
           end
           initial begin
               $readmemh("alu.tv", testvectors);
28
29
30
               for(int i = 0; i < 20; i = i + 1) begin
    {ALUControl, a, b, Result, ALUFlags} = testvectors[i]; @(posedge clk);
end //end simulation</pre>
31
           end //initial
34
35
       endmodule
36
```