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EE 469
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Lab 3 Report

Procedure

In this lab, the single cycle processor was upgraded to a pipelined processor. Stalling, flushing, and forwarding logic were added to handle data and control hazards.

Results

```
11100000010011110000000000001111    // 0  MAIN  SUB  R0 R15 R15    R0 = 0
11100010100000000001000000000001    // 4        ADD  R1 R0 #1     R1 = 1
11100001100000000010000000000001    // 8        ORR  R2 R0 R1     R2 = 1
11100010100000000010000000000010    // 12       ADD  R2 R0 #2     R2 = 2
11100010010100100000000000000000    // 16       SUBS R0 R2 #0     R0 = 2
00001010000000000000000000000001    // 20       BEQ  TAG1
11100000000000100010000000000000    // 24       AND  R2 R2 R0     R2 = 2
11100000000000100001000000000000    // 28       AND  R1 R2 R0     R1 = 2
11100000100000011001000000000000    // 32 TAG1  ADD  R9 R1 R0     R9 = 4
11100101100000000100100000001001    // 36       STR  R9 [R0, #9]
11100101100100000011000000001001    // 40       LDR  R3 [R0, #9]  R3 = 4
11100000000000011001000000000010    // 44       AND  R2 R3 R2     R2 = 0
```

Figure 1: Test assembly instructions with expected register outputs

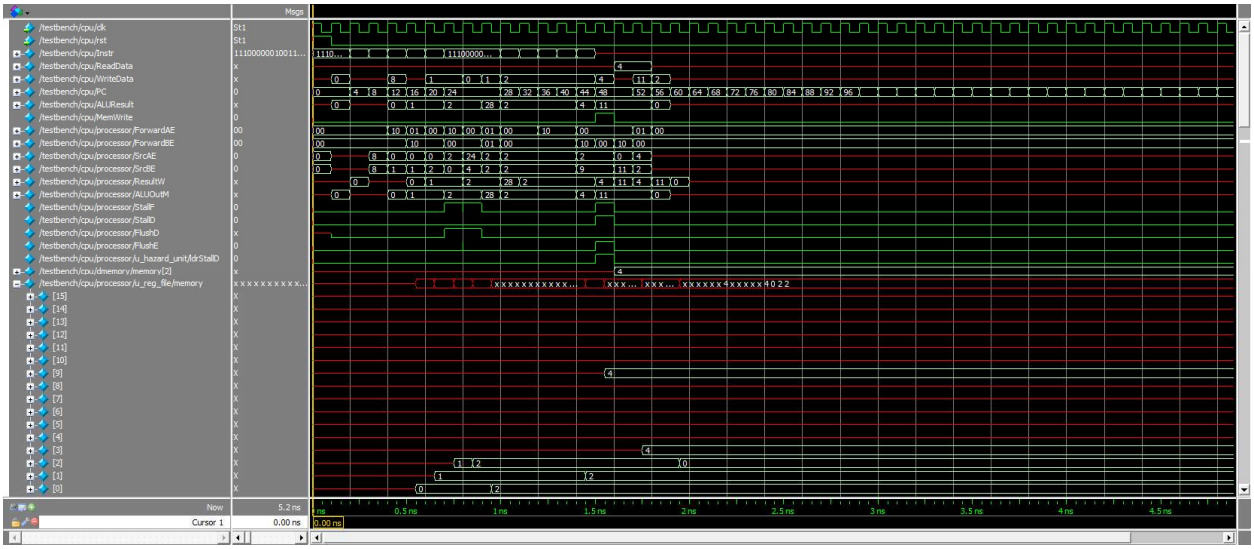

Figure 2: Simulation waveform

As shown in Figure 1 and 2, the pipelined processor is executing the instructions correctly. Stalling, flushing, and forwarding processes are also demonstrated. Figure 2 will be investigated more thoroughly in the following sections. Figures 3, 4, and 5 are magnified portions of Figure 2.

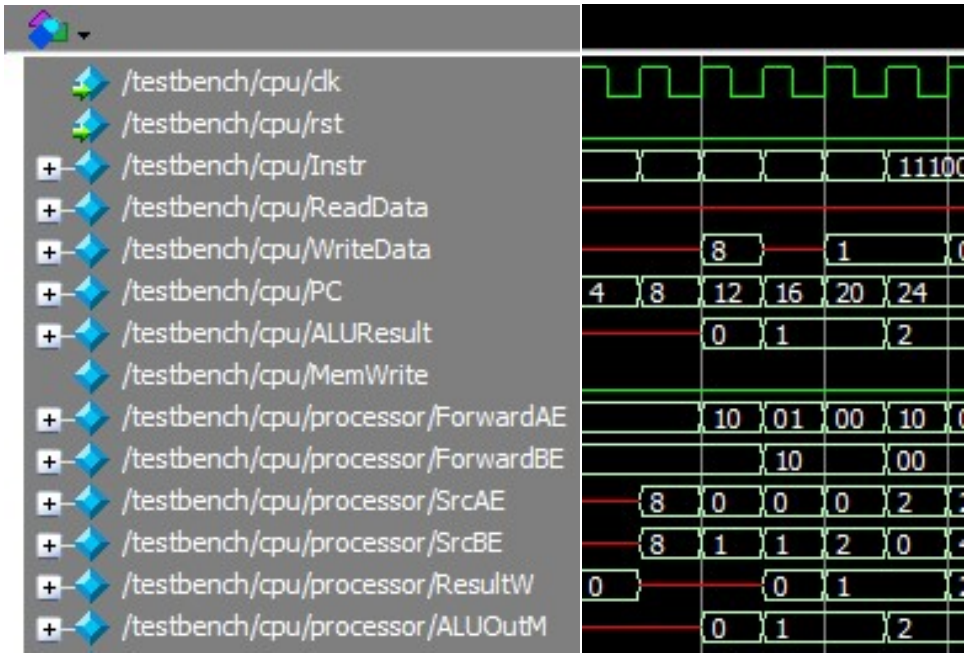

Figure 3: Forwarding signals

When PC=12, instruction 4 is in the execution stage and instruction 0 is in the memory stage. Since source register A of instruction 4 is the same as the destination register of instruction 0, there is a match between execute and memory stages and ForwardAE is set to 10. Hence, the data from the memory stage is forwarded to the execution stage: SrcAE = ALUOutM.

When PC=16, instruction 8 is in the execution stage and instruction 0 is in the writeback stage. Since source register A of instruction 8 is the same as the destination register of instruction 0, there is a match between execute and writeback stages and ForwardAE is set to 01. Hence, the data from the writeback stage is forwarded to the execution stage: SrcAE = ResultW.

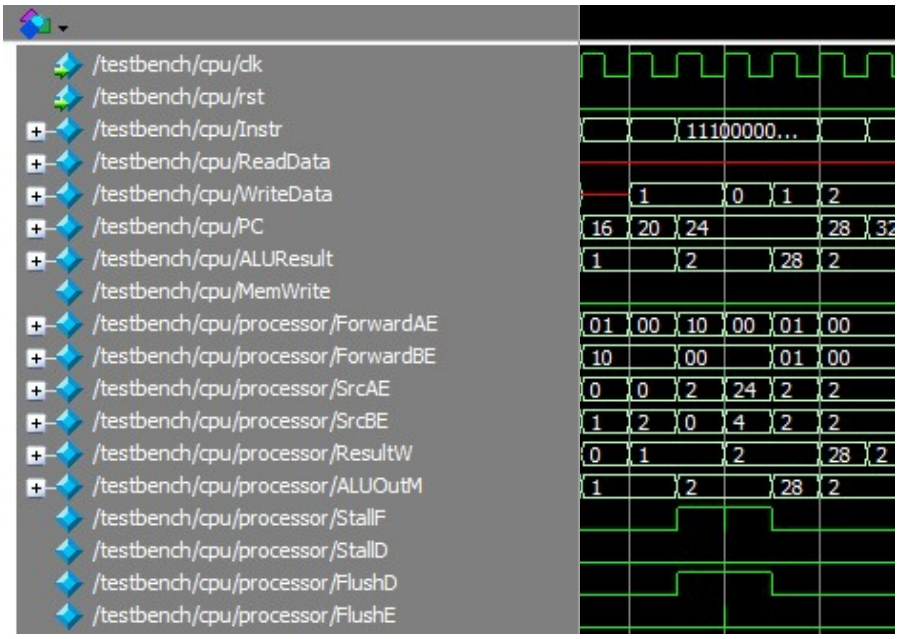

Figure 4: Branch flushing

Figure 4 shows that the two cycles of instruction are being flushed when the branch instruction (instruction 20) enters the decode stage.

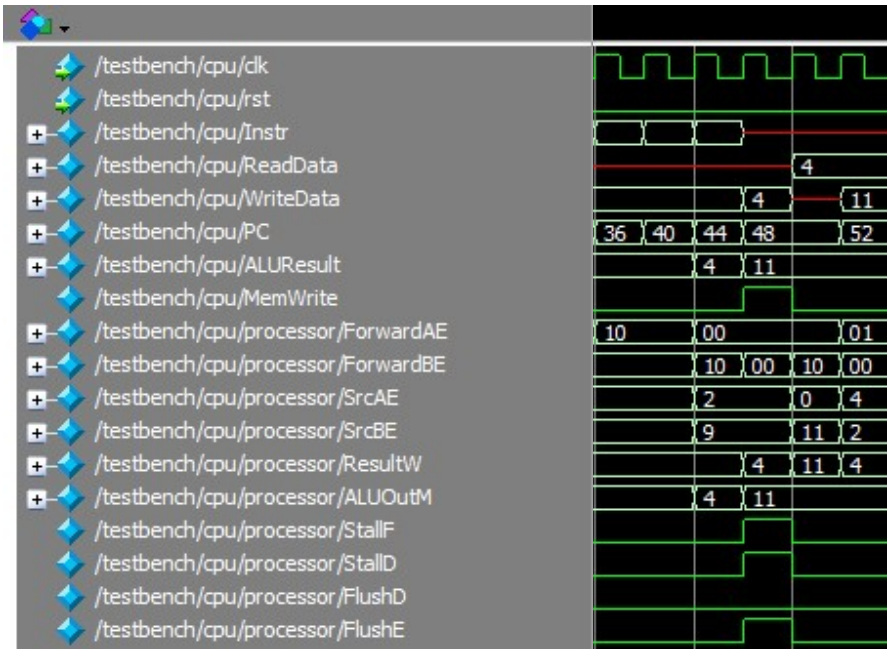

Figure 5: Memory stalling

Figure 5 shows that the processor stalled for the LDR instruction (instruction 40) to finish before executing instruction 44, which accessed the destination register of instruction 40.

Appendix