Advanced Computer Architecture The Smooth Challenge

Lukasz Koprowski
Department of Computing
Imperial College London
Email: lukasz.koprowski10@imperial.ac.uk

Abstract—The abstract goes here.

I. Introduction

This demo file is intended to serve as a "starter file" for IEEE conference papers produced under LATEX using IEEE-tran.cls version 1.7 and later. I wish you the best of success.

mds

January 11, 2007

A. Subsection Heading Here

Subsection text here.

1) Subsubsection Heading Here: Subsubsection text here.

II. HARDWARE AND SOFTWARE ANALYSIS

CPU Intel(R) Core(TM)2 Duo CPU T5800 @ 2.00GHz cache: 2048 KB cores: 2

RAM

OS Ubuntu 12.10

Compiler GCC 4.7.2

Language C++11

We started work on speeding up the application by looking at available hardware, and possible techniques which could be applied to achieve better performance.

We chose a 5 years old Toshiba laptop as our target device. It has a Intel Core 2 Due CPU with 2MB of cache and 2 cores, one tacked at 800 MHz, and another at 2.00 GHZ. There was 3GB of RAM memory. We were hoping to find a graphics card with CUDA support, but we were unlucky here.

The first improvement that came to or mind was to optimize compiler's flags to target our platform. We expected it provide a huge gain considering that this micro architecture supports floating point vector operations and knowing that the code generation can significantly affect applications performance.

With two separate cores the second obvious move was to fully utilize power of both of them. That required detecting areas of the applications that were independent and could be run in parallel. Robert Kruszewski Twentieth Century Fox Springfield, USA Email: homer@thesimpsons.com

III. APPLICATION ANALYSIS

IV. PERFORMANCE IMPROVEMENTS

Chosen mesh size

V. CONCLUSION

The conclusion goes here.

ACKNOWLEDGMENT

The authors would like to thank...

REFERENCES

 H. Kopka and P. W. Daly, A Guide to ETEX, 3rd ed. Harlow, England: Addison-Wesley, 1999.