**同济大学**

**计算机科学与技术系**

**计算机组成原理课程实验报告**

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日 期 2018/5/28

# 实验目标

使用 Verilog HDL 语言实现 54 条 MIPS 指令的 CPU 的设计和仿真。

# 总体设计

## 作品功能设计及原理说明

MIPS的所有指令的格式

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Opcode | Name | Action | Opcode bitfields | | | | | |
| **Arithmetic Logic Unit** | | | | | | | | |
| ADD rd,rs,rt | Add | rd=rs+rt | 000000 | rs | rt | rd | 00000 | 100000 |
| ADDI rt,rs,imm | Add Immediate | rt=rs+imm | 001000 | rs | rt | imm | | |
| ADDIU rt,rs,imm | Add Immediate Unsigned | rt=rs+imm | 001001 | rs | rt | imm | | |
| ADDU rd,rs,rt | Add Unsigned | rd=rs+rt | 000000 | rs | rt | rd | 00000 | 100001 |
| AND rd,rs,rt | And | rd=rs&rt | 000000 | rs | rt | rd | 00000 | 100100 |
| ANDI rt,rs,imm | And Immediate | rt=rs&imm | 001100 | rs | rt | imm | | |
| LUI rt,imm | Load Upper Immediate | rt=imm<<16 | 001111 | rs | rt | imm | | |
| NOR rd,rs,rt | Nor | rd=~(rs|rt) | 000000 | rs | rt | rd | 00000 | 100111 |
| OR rd,rs,rt | Or | rd=rs|rt | 000000 | rs | rt | rd | 00000 | 100101 |
| ORI rt,rs,imm | Or Immediate | rt=rs|imm | 001101 | rs | rt | imm | | |
| SLT rd,rs,rt | Set On Less Than | rd=rs<rt | 000000 | rs | rt | rd | 00000 | 101010 |
| SLTI rt,rs,imm | Set On Less Than Immediate | rt=rs<imm | 001010 | rs | rt | imm | | |
| SLTIU rt,rs,imm | Set On | rt=rs<imm | 001011 | rs | rt | imm | | |
| SLTU rd,rs,rt | Set On Less Than Unsigned | rd=rs<rt | 000000 | rs | rt | rd | 00000 | 101011 |
| SUB rd,rs,rt | Subtract | rd=rs-rt | 000000 | rs | rt | rd | 00000 | 100010 |
| SUBU rd,rs,rt | Subtract Unsigned | rd=rs-rt | 000000 | rs | rt | rd | 00000 | 100011 |
| XOR rd,rs,rt | Exclusive Or | rd=rs^rt | 000000 | rs | rt | rd | 00000 | 100110 |
| XORI rt,rs,imm | Exclusive Or Immediate | rt=rs^imm | 001110 | rs | rt | imm | | |
| **Shifter** | | | | | | | | |
| SLL rd,rt,sa | Shift Left Logical | rd=rt<<sa | 000000 | rs | rt | rd | sa | 000000 |
| SLLV rd,rt,rs | Shift Left Logical Variable | rd=rt<<rs | 000000 | rs | rt | rd | 00000 | 000100 |
| SRA rd,rt,sa | Shift Right Arithmetic | rd=rt>>sa | 000000 | 00000 | rt | rd | sa | 000011 |
| SRAV rd,rt,rs | Shift Right Arithmetic Variable | rd=rt>>rs | 000000 | rs | rt | rd | 00000 | 000111 |
| SRL rd,rt,sa | Shift Right Logical | rd=rt>>sa | 000000 | rs | rt | rd | sa | 000010 |
| SRLV rd,rt,rs | Shift Right Logical Variable | rd=rt>>rs | 000000 | rs | rt | rd | 00000 | 000110 |
| **Multiply** | | | | | | | | |
| DIV rs,rt | Divide | HI=rs%rt; LO=rs/rt | 000000 | rs | rt | 0000000000 | | 011010 |
| DIVU rs,rt | Divide Unsigned | HI=rs%rt; LO=rs/rt | 000000 | rs | rt | 0000000000 | | 011011 |
| MFHI rd | Move From HI | rd=HI | 000000 | 0000000000 | | rd | 00000 | 010000 |
| MFLO rd | Move From LO | rd=LO | 000000 | 0000000000 | | rd | 00000 | 010010 |
| MTHI rs | Move To HI | HI=rs | 000000 | rs | 000000000000000 | | | 010001 |
| MTLO rs | Move To LO | LO=rs | 000000 | rs | 000000000000000 | | | 010011 |
| MULT rs,rt | Multiply | HI,LO=rs\*rt | 000000 | rs | rt | 0000000000 | | 011000 |
| MULTU rs,rt | Multiply Unsigned | HI,LO=rs\*rt | 000000 | rs | rt | 0000000000 | | 011001 |
| **Branch** | | | | | | | | |
| BEQ rs,rt,offset | Branch On Equal | if(rs==rt) pc+=offset\*4 | 000100 | rs | rt | offset | | |
| BGEZ rs,offset | Branch On >= 0 | if(rs>=0) pc+=offset\*4 | 000001 | rs | 00001 | offset | | |
| BGEZAL rs,offset | Branch On >= 0 And Link | r31=pc; if(rs>=0) pc+=offset\*4 | 000001 | rs | 10001 | offset | | |
| BGTZ rs,offset | Branch On > 0 | if(rs>0) pc+=offset\*4 | 000111 | rs | 00000 | offset | | |
| BLEZ rs,offset | Branch On | if(rs<=0) pc+=offset\*4 | 000110 | rs | 00000 | offset | | |
| BLTZ rs,offset | Branch On | if(rs<0) pc+=offset\*4 | 000001 | rs | 00000 | offset | | |
| BLTZAL rs,offset | Branch On | r31=pc; if(rs<0) pc+=offset\*4 | 000001 | rs | 10000 | offset | | |
| BNE rs,rt,offset | Branch On Not Equal | if(rs!=rt) pc+=offset\*4 | 000101 | rs | rt | offset | | |
| BREAK | Breakpoint | epc=pc; pc=0x3c | 000000 | code | | | | 001101 |
| J target | Jump | pc=pc\_upper|(target<<2) | 000010 | target | | | | |
| JAL target | Jump And Link | r31=pc; pc=target<<2 | 000011 | target | | | | |
| JALR rs | Jump And Link Register | rd=pc; pc=rs | 000000 | rs | 00000 | rd | 00000 | 001001 |
| JR rs | Jump Register | pc=rs | 000000 | rs | 000000000000000 | | | 001000 |
| MFC0 rt,rd | Move From Coprocessor | rt=CPR[0,rd] | 010000 | 00000 | rt | rd | 00000000000 | |
| MTC0 rt,rd | Move To Coprocessor | CPR[0,rd]=rt | 010000 | 00100 | rt | rd | 00000000000 | |
| SYSCALL | System Call | epc=pc; pc=0x3c | 000000 | 00000000000000000000 | | | | 001100 |
| **Memory Access** | | | | | | | | |
| LB rt,offset(rs) | Load Byte | rt=\*(char\*)(offset+rs) | 100000 | rs | rt | offset | | |
| LBU rt,offset(rs) | Load Byte Unsigned | rt=\*(Uchar\*)(offset+rs) | 100100 | rs | rt | offset | | |
| LH rt,offset(rs) | Load Halfword | rt=\*(short\*)(offset+rs) | 100001 | rs | rt | offset | | |
| LBU rt,offset(rs) | Load Halfword Unsigned | rt=\*(Ushort\*)(offset+rs) | 100101 | rs | rt | offset | | |
| LW rt,offset(rs) | Load Word | rt=\*(int\*)(offset+rs) | 100011 | rs | rt | offset | | |
| SB rt,offset(rs) | Store Byte | \*(char\*)(offset+rs)=rt | 101000 | rs | rt | offset | | |
| SH rt,offset(rs) | Store Halfword | \*(short\*)(offset+rs)=rt | 101001 | rs | rt | offset | | |
| SW rt,offset(rs) | Store Word | \*(int\*)(offset+rs)=rt | 101011 | rs | rt | offset | | |

# 主要模块（指令）设计

## ADD

### 操作流程（不用流程图表示，用列表表示）

* 取指令
* temp←GPR[rs]+GPR[rt]（判断上下溢出）
* 若溢出
  + 异常信号
* 否则
  + GPR[rd]←temp
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GRP[rt] | ALUOVF? |

### 数据通路图



## ADDU

### 操作

* 取指令
* temp←GPR[rs]+GPR[rt]（判断上下溢出）
* GPR[rd]←temp
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GRP[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GRP[rt] | 0 |

### 数据通路图



## SUB

### 操作

* 取指令
* temp←GPR[rs]-GPR[rt]（判断上下溢出）
* 若溢出
  + 异常信号
* 否则
  + GPR[rd]←temp
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |

### 数据通路图



## SUBU

### 操作

* 取指令
* temp←GPR[rs]-GPR[rt]（不判断上下溢出）
* GPR[rd]←temp
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |

### 数据通路图



## AND

### 操作

* 取指令
* GPR[rd]←GPR[rs]|GPR[rt]
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |

### 数据通路图



## OR

### 操作

* 取指令
* GPR[rd]←GPR[rs]&GPR[rt]
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |

### 数据通路图



## XOR

### 操作

* 取指令
* GPR[rd]←GPR[rs]^GPR[rt]
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |

### 数据通路图



## NOR

### 操作

* 取指令
* GPR[rd]←GPR[rs]**↓**GPR[rt]
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |

### 数据通路图



## SLT

### 操作

* 取指令
* GPR[rd]←((signed)GPR[rs]<(signed)GPR[rt])?32'b1:32'b0
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |

### 数据通路图



## SLTU

### 操作

* 取指令
* GPR[rd]←((unsigned)GPR[rs]<(unsigned)GPR[rt])?32'b1:32'b0
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |

### 数据通路图



## SLL

### 操作

* 取指令
* s←sa
* GPR[rd]←{GPR[rt][31-s:0], (s){1'b0}}
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |

### 数据通路图



## SRL

### 操作

* 取指令
* s←sa
* GPR[rd]←{(s){1'b0}, GPR[rt][31:s]}
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |

### 数据通路图



## SRA

### 操作

* 取指令
* s←sa
* GPR[rd]←{(s){GPR[rt][31]}, GPR[rt][31:s]}
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |

### 数据通路图



## SLLV

### 操作

* 取指令
* s←GPR[rs][4:0]
* GPR[rd]←{GPR[rt][31-s:0], (s){1'b0}}
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |

### 数据通路图



## SRLV

### 操作

* 取指令
* s←GPR[rs][4:0]
* GPR[rd]←{(s){1'b0}, GPR[rt][31:s]}
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |

### 数据通路图



## SRAV

### 操作

* 取指令
* s←GPR[rs][4:0]
* GPR[rd]←{(s){GPR[rt][31]}, GPR[rt][31:s]}
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |

### 数据通路图



## JR

### 操作

* 取指令
* PC←GPR[rs]

### 列表

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT |
| WData(rd) | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |

### 数据通路图



## ADDI

### 操作

* 取指令
* signed\_imm←{{(16){immediate[15]}},immediate}
* temp←GPR[rs]+ signed\_imm（带符号，判断上下溢出）
* 若溢出
  + 异常信号
* 否则
  + GPR[rt]←temp
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |

### 数据通路图



## ADDIU

### 操作

* 取指令
* signed\_imm←{{(16){immediate[15]}},immediate}
* temp←GPR[rs]+ signed\_imm（无符号，不判断上下溢出）
* GPR[rt]←temp
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |

### 数据通路图



## ANDI

### 操作

* 取指令
* GPR[rt]←GPR[rs]&{16'b0, immediate}
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |

### 数据通路图



## ORI

### 操作

* 取指令
* GPR[rt]←GPR[rs]|{16'b0, immediate}
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |

### 数据通路图



## XORI

### 操作

* 取指令
* GPR[rt]←GPR[rs]^{16'b0, immediate}
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |

### 数据通路图



## LW

### 操作

* 取指令
* vAddr←{(16){offset[15]}, offset}+GPR[base] //虚拟地址
* pAddr←AddressTranslation(vAddr) //物理地址
* memword←LoadMemoryWord(pAddr)
* GPR[rt]←memword
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND | DMEM | ADDRMAP |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP | ALU |

### 数据通路图



## SW

### 操作

* 取指令
* vAddr←{(16){offset[15]}, offset}+GPR[base] //虚拟地址
* pAddr←AddressTranslation(vAddr) //物理地址
* dataword←GPR[rt]
* StoreMemory(pAddr, dataword)
* PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND | DMEM | ADDRMAP |
| WData | A | OP | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |

### 数据通路图



## BEQ

### 操作

* 取指令
* target\_offset←{(14){offset[15],offset,2'b0}
* if(GPR[rs]==GPR[rt])
  + PC←PC+target\_offset
* else
  + PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND | DMEM | ADDRMAP | MUX | UADD | |
| WData | A | OP | B | A | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |

### 数据通路图



## BNE

### 操作

* 取指令
* target\_offset←{(14){offset[15],offset,2'b0}
* if(!(GPR[rs]==GPR[rt]))
  + PC←PC+target\_offset
* else
  + PC←PC+4

### 列表

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND | DMEM | ADDRMAP | MUX | UADD | |
| WData | A | OP | B | A | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |

### 数据通路图



## SLTI

### 操作

* 取指令
* GPR[rt]←((signed)GPR[rs]<(signed)({(16{immediate[15]}, immediate}))?32'b1:32'b0
* PC←PC+4

### 列表

| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND | DMEM | ADDRMAP | MUX | UADD | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| WData | A | OP | B | A | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |

### 数据通路图



## SLTIU

### 操作

* 取指令
* GPR[rt]←((unsigned)GPR[rs]<(unsigned)({(16{immediate[15]}, immediate}))?32'b1:32'b0
* PC←PC+4

### 列表

| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND | DMEM | ADDRMAP | MUX | UADD | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| WData | A | OP | B | A | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |

### 数据通路图



## LUI

### 操作

* 取指令
* GPR[rt]←{immediate,16'b0}
* PC←PC+4

### 列表

| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND | DMEM | ADDRMAP | MUX | UADD | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| WData(默认rd) | A | OP | B | A | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |

### 数据通路图



## J

### 操作

* 取指令
* PC←{PC[31:28], instr\_index, 2'b0}

### 列表

| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND | DMEM | ADDRMAP | MUX | UADD | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| WData(默认rd) | A | OP | B | A | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |

### 数据通路图



## JAL

### 操作

* 取指令
* GPR[31]←PC+4（没有延迟槽√）或PC+8（有延迟槽）
* PC←{PC[31:28], instr\_index, 2'b0}

### 列表

| 指令 | PC | IM | RF | ALU | | | EXPT | EXTEND | DMEM | ADDRMAP | MUX | UADD | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| WData(默认rd) | A | OP | B | A | B |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |

### 数据通路图



## DIV

### 操作

* 取指令
* quotient←GPR[rs] / GPR[rt]（32位带符号）
* LO←quotient
* remainder←GPR[rs] % GPR[rt]（32位带符号）
* HI←remainder
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |

### 数据通路图



## DIVU

### 操作

* 取指令
* quotient←GPR[rs] / GPR[rt]（32位无符号）
* LO←quotient
* remainder←GPR[rs] % GPR[rt]（32位无符号）
* HI←remainder
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |

### 数据通路图



## MULT

### 操作

* 取指令
* product←GPR[rs] \* GPR[rt]（32位有符号）
* LO←product[31:0]
* HI←product[63:32]
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |

### 数据通路图



## MULTU

### 操作

* 取指令
* product←GPR[rs] \* GPR[rt]（32位无符号）
* LO←product[31:0]
* HI←product[63:32]
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |

### 数据通路图



## BGEZ

### 操作

* 取指令
* 如果 GPR[rs]>=0
  + PC←PC+{16{offset[15]}, offset}
* 否则
  + PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |

### 数据通路图



## JALR

### 操作

* 取指令
* temp←GPR[rs]
* GPR[rd]←PC+4（不考虑延迟槽）
* PC←temp

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  |  |  |  |  |  |  |  |

### 数据通路图



## LBU

### 操作

* 取指令
* ext\_offset←{16{offset[15]}, offset}
* vAddr←ext\_offset+GPR[base]
* pAddr←AddressTranslation(vAddr)
* //pAddr←{pAddr[31:2], pAddr[1:0]^2{ReverseEndian}}
* memword←LoadMemoryWord(pAddr)
* byte←vAddr[1:0]^{2{BigEndianCPU}}
* membyte←memword[8\*byte+:8]
* GPR[rt]←{24'b0,membyte}
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |

### 数据通路图



## LHU

### 操作

* 取指令
* ext\_offset←{16{offset[15]}, offset}
* vAddr←ext\_offset+GPR[base] //(必须是2字节对齐的，即vAddr末位为0)
* pAddr←AddressTranslation(vAddr)
* //pAddr←{pAddr[31:2], pAddr[1:0]^{ReverseEndian,0}}
* memword←LoadMemoryWord(pAddr)
* byte←vAddr[1:0]^{BigEndianCPU,0}
* membyte←memword[8\*byte+:16]
* GPR[rt]←{24'b0,membyte}
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |

### 数据通路图



## LB

### 操作

* 取指令
* ext\_offset←{16{offset[15]}, offset}
* vAddr←ext\_offset+GPR[base]
* pAddr←AddressTranslation(vAddr)
* //pAddr←{pAddr[31:2], pAddr[1:0]^2{ReverseEndian}}
* memword←LoadMemoryWord(pAddr)
* byte←vAddr[1:0]^{2{BigEndianCPU}}
* membyte←memword[8\*byte+:8]
* GPR[rt]←{24{membyte[8]},membyte}
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |

### 数据通路图



## LH

### 操作

* 取指令
* ext\_offset←{16{offset[15]}, offset}
* vAddr←ext\_offset+GPR[base] //(必须是2字节对齐的，即vAddr末位为0)
* pAddr←AddressTranslation(vAddr)
* //pAddr←{pAddr[31:2], pAddr[1:0]^{ReverseEndian,0}}
* memword←LoadMemoryWord(pAddr)
* byte←vAddr[1:0]^{BigEndianCPU,0}
* membyte←memword[8\*byte+:16]
* GPR[rt]←{16{membyte[15]},membyte}
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |

### 数据通路图



## SB

### 操作

* 取指令
* ext\_offset←{16{offset[15]}, offset}
* vAddr←ext\_offset+GPR[base]
* pAddr←AddressTranslation(vAddr)
* //pAddr←{pAddr[31:2], pAddr[1:0]^{ReverseEndian,0}}
* StoreMemoryByte(pAddr, GPR[rt][7:0]) //可能需要将GPR[rt]的低字节根据写入位置调整位置，补充0形成一个字再送内存
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |

### 数据通路图



## SH

### 操作

* 取指令
* ext\_offset←{16{offset[15]}, offset}
* vAddr←ext\_offset+GPR[base] //(必须是2字节对齐的，即vAddr末位为0)
* pAddr←AddressTranslation(vAddr)
* //pAddr←{pAddr[31:2], pAddr[1:0]^{ReverseEndian,0}}
* StoreMemoryHalfWord(pAddr, GPR[rt][15:0]) //可能需要将GPR[rt]的低半字根据写入位置调整位置，补充0形成一个字再送内存
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |

### 数据通路图



## BREAK

### 操作

* 取指令
* 触发BREAK异常

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |

### 数据通路图



## SYSCALL

### 操作

* 取指令
* 触发SYSCALL异常

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |
| SYSCALL | SYSCALL←1，cause[6:2]←4'b1000  exec\_addr←PC | | | | | | | | | | | | | |

### 数据通路图



## ERET

### 操作

* 取指令
* 调用返回

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |
| SYSCALL | SYSCALL←1，cause[6:2]←4'b1000  exec\_addr←PC | | | | | | | | | | | | | |
| ERET | ERET←1, status←status>>5  PC←EPC\_out | | | | | | | | | | | | | |

### 数据通路图



## MFHI

### 操作

* 取指令
* GPR[rd]←HI
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |
| SYSCALL | SYSCALL←1，cause[6:2]←4'b1000  exec\_addr←PC | | | | | | | | | | | | | |
| ERET | ERET←1, status←status>>5  PC←EPC\_out | | | | | | | | | | | | | |
| MFHI | PC+4 | PC | HI→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |

### 数据通路图



## MFLO

### 操作

* 取指令
* GPR[rd]←LO
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |
| SYSCALL | SYSCALL←1，cause[6:2]←4'b1000  exec\_addr←PC | | | | | | | | | | | | | |
| ERET | ERET←1, status←status>>5  PC←EPC\_out | | | | | | | | | | | | | |
| MFHI | PC+4 | PC | HI→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MFLO | PC+4 | PC | LO→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |

### 数据通路图



## MTHI

### 操作

* 取指令
* HI←GPR[rs]
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |
| SYSCALL | SYSCALL←1，cause[6:2]←4'b1000  exec\_addr←PC | | | | | | | | | | | | | |
| ERET | ERET←1, status←status>>5  PC←EPC\_out | | | | | | | | | | | | | |
| MFHI | PC+4 | PC | HI→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MFLO | PC+4 | PC | LO→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MTHI | PC+4 | PC | HI←GPR[rs] | | | | | | | | | | | |

### 数据通路图



## MTLO

### 操作

* 取指令
* LO←GPR[rs]
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |
| SYSCALL | SYSCALL←1，cause[6:2]←4'b1000  exec\_addr←PC | | | | | | | | | | | | | |
| ERET | ERET←1, status←status>>5  PC←EPC\_out | | | | | | | | | | | | | |
| MFHI | PC+4 | PC | HI→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MFLO | PC+4 | PC | LO→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MTHI | PC+4 | PC | HI←GPR[rs] | | | | | | | | | | | |
| MTLO | PC+4 | PC | LO←GPR[rs] | | | | | | | | | | | |

### 数据通路图



## MFC0

### 操作

* 取指令
* GPR[rt]←CPR[0,rd]
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |
| SYSCALL | SYSCALL←1，cause[6:2]←4'b1000  exec\_addr←PC | | | | | | | | | | | | | |
| ERET | ERET←1, status←status>>5  PC←EPC\_out | | | | | | | | | | | | | |
| MFHI | PC+4 | PC | HI→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MFLO | PC+4 | PC | LO→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MTHI | PC+4 | PC | HI←GPR[rs] | | | | | | | | | | | |
| MTLO | PC+4 | PC | LO←GPR[rs] | | | | | | | | | | | |
| MFC0 | PC+4 | PC | cp0addr←rd  mfc0←1  GPR[rt]←cp0rdata | | | | | | | | | | | |

### 数据通路图



## MTC0

### 操作

* 取指令
* CPR[0,rd]←GPR[rt]
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |
| SYSCALL | SYSCALL←1，cause[6:2]←4'b1000  exec\_addr←PC | | | | | | | | | | | | | |
| ERET | ERET←1, status←status>>5  PC←EPC\_out | | | | | | | | | | | | | |
| MFHI | PC+4 | PC | HI→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MFLO | PC+4 | PC | LO→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MTHI | PC+4 | PC | HI←GPR[rs] | | | | | | | | | | | |
| MTLO | PC+4 | PC | LO←GPR[rs] | | | | | | | | | | | |
| MFC0 | PC+4 | PC | cp0addr←rd  mfc0←1  GPR[rt]←cp0rdata | | | | | | | | | | | |
| MTC0 | PC+4 | PC | cp0addr←rd  mtc0←1  cp0data←GPR[rt] | | | | | | | | | | | |

### 数据通路图



## CLZ

### 操作

* 取指令
* GPR[rd]←count\_leading\_zeros GPR[rs]
* PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |
| SYSCALL | SYSCALL←1，cause[6:2]←4'b1000  exec\_addr←PC | | | | | | | | | | | | | |
| ERET | ERET←1, status←status>>5  PC←EPC\_out | | | | | | | | | | | | | |
| MFHI | PC+4 | PC | HI→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MFLO | PC+4 | PC | LO→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MTHI | PC+4 | PC | HI←GPR[rs] | | | | | | | | | | | |
| MTLO | PC+4 | PC | LO←GPR[rs] | | | | | | | | | | | |
| MFC0 | PC+4 | PC | cp0addr←rd  mfc0←1  GPR[rt]←cp0rdata | | | | | | | | | | | |
| MTC0 | PC+4 | PC | cp0addr←rd  mtc0←1  cp0data←GPR[rt] | | | | | | | | | | | |
| CLZ | PC+4 | PC | ALU→GRP[rd] | GPR[rs] | CLZ |  | 0 |  |  |  |  |  |  |  |

### 数据通路图



## TEQ

### 操作

* 取指令
* 如果 GPR[rt]==GPR[rs]
  + 触发TRAP异常
* 否则
  + PC←PC+4

### 列表

| **指令** | **PC** | **IM** | **RF和HI/LO** | **ALU** | | | **EXPT** | **EXTEND** | **EXTEND2** | **DMEM** | **ADDRMAP** | **MUX** | **UADD** | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **WData(默认rd)** | **A** | **OP** | **B** | **A** | **B** |
| ADD | PC+4 | PC | ALU | GPR[rs] | S+ | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| ADDU | PC+4 | PC | ALU | GPR[rs] | U+ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SUB | PC+4 | PC | ALU | GPR[rs] | S- | GPR[rt] | ALUOVF? |  |  |  |  |  |  |  |
| SUBU | PC+4 | PC | ALU | GPR[rs] | U- | GPR[rt] | 0 |  |  |  |  |  |  |  |
| AND | PC+4 | PC | ALU | GPR[rs] | & | GPR[rt] | 0 |  |  |  |  |  |  |  |
| OR | PC+4 | PC | ALU | GPR[rs] | | | GPR[rt] | 0 |  |  |  |  |  |  |  |
| XOR | PC+4 | PC | ALU | GPR[rs] | ^ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| NOR | PC+4 | PC | ALU | GPR[rs] | **↓** | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLT | PC+4 | PC | ALU | GPR[rs] | S< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLTU | PC+4 | PC | ALU | GPR[rs] | U< | GPR[rt] | 0 |  |  |  |  |  |  |  |
| SLL | PC+4 | PC | ALU | GPR[rt] | << | sa | 0 |  |  |  |  |  |  |  |
| SRL | PC+4 | PC | ALU | GPR[rt] | >> | sa | 0 |  |  |  |  |  |  |  |
| SRA | PC+4 | PC | ALU | GPR[rt] | >>> | sa | 0 |  |  |  |  |  |  |  |
| SLLV | PC+4 | PC | ALU | GPR[rt] | << | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRLV | PC+4 | PC | ALU | GPR[rt] | >> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| SRAV | PC+4 | PC | ALU | GPR[rt] | >>> | GPR[rs] | 0 |  |  |  |  |  |  |  |
| JR | GPR[rs] | PC | - | - | - | - | GPR[rs] [1:0]==2'b0 |  |  |  |  |  |  |  |
| ADDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | S+ | EXTEND | ALUOVF? | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ADDIU | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | U+ | EXTEND | 0 | IM[15:0] (SIGN) |  |  |  |  |  |  |
| ANDI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | & | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| ORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | | | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| XORI | PC+4 | PC | ALU (→GPR[rt]) | GPR[rs] | ^ | EXTEND | 0 | IM[15:0] (ZERO) |  |  |  |  |  |  |
| LW | PC+4 | PC | DMEM (→GPR[rt]) | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, R | ALU |  |  |  |
| SW | PC+4 | PC |  | GPR[base] | U+ | EXTEND | 0 | IM[15:0]  (SIGN) |  | ADDRMAP, GPR[rt], W | ALU |  |  |  |
| BEQ | MUX[ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| BNE | MUX[~ALU[0]] | PC |  | GPR[rs] | == | GPR[rt] | 0 | IM[15:0]  (SIGN) |  |  |  | PC+4,  UADD | PC | {EXTEND [29:0],2'b0} |
| SLTI | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| SLTIU | PC+4 | PC | ALU  (→GPR[rt]) | GPR[rs] | S< | EXTEND | 0 | IM[15:0]  (SIGN) |  |  |  |  |  |  |
| LUI | PC+4 | PC | {immediate, 16'b0}  (→GPR[rt]) |  |  |  | 0 |  |  |  |  |  |  |  |
| J | {PC[31:28], instr\_index, 2'b0} | PC |  |  |  |  | 0 |  |  |  |  |  |  |  |
| JAL | {PC[31:28], instr\_index, 2'b0} | PC | PC+4  →GPR[31] |  |  |  | 0 |  |  |  |  |  |  |  |
| DIV | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | S/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| DIVU | PC+4 | PC | ALU(除法)  LO←quotient  HI← remainder | GPR[rs] | U/ | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULT | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | S\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| MULTU | PC+4 | PC | ALU(乘法)  {HI, LO}←remainder | GPR[rs] | U\* | GPR[rt] | 0 |  |  |  |  |  |  |  |
| BGEZ | MUX[GPR[rs][31]] | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  |  |  | UADD,PC+4 | PC | EXTEND[29:0],2'b0 |
| JALR | GPR[rs] | PC | PC+8 |  |  |  | 0 |  |  |  |  |  |  |  |
| LBU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LHU | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (ZERO) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LB | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:8]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| LH | PC+4 | PC | EXTEND2→GRP[rt] |  |  |  | 0 | IM[15:0](offset)  (SIGN) | DMEM[byte\*8+:16]  (SIGN) | ADDRMAP,R | UADD |  | EXTEND | GPR[base] |
| SB | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][7:0],W | UADD |  | EXTEND | GPR[base] |
| SH | PC+4 | PC |  |  |  |  | 0 | IM[15:0](offset)  (SIGN) |  | ADDRMAP,GPR[rt][15:0],W | UADD |  | EXTEND | GPR[base] |
| BREAK | BREAK←1，cause[6:2]←4'b1001  exec\_addr←PC | | | | | | | | | | | | | |
| SYSCALL | SYSCALL←1，cause[6:2]←4'b1000  exec\_addr←PC | | | | | | | | | | | | | |
| ERET | ERET←1, status←status>>5  PC←EPC\_out | | | | | | | | | | | | | |
| MFHI | PC+4 | PC | HI→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MFLO | PC+4 | PC | LO→GRP[rd] |  |  |  | 0 |  |  |  |  |  |  |  |
| MTHI | PC+4 | PC | HI←GPR[rs] | | | | | | | | | | | |
| MTLO | PC+4 | PC | LO←GPR[rs] | | | | | | | | | | | |
| MFC0 | PC+4 | PC | cp0addr←rd  mfc0←1  GPR[rt]←cp0rdata | | | | | | | | | | | |
| MTC0 | PC+4 | PC | cp0addr←rd  mtc0←1  cp0data←GPR[rt] | | | | | | | | | | | |
| CLZ | PC+4 | PC | ALU→GRP[rd] | GPR[rs] | CLZ |  | 0 |  |  |  |  |  |  |  |
| TEQ | PC+4 | PC |  | GPR[rs] | == | GPR[rt] | TRAP←ALU[0]，cause[6:2]←ALU[0]?cause[6:2]  exec\_addr←ALU[0]?PC:exec\_addr | | | | | | | |

### 数据通路图



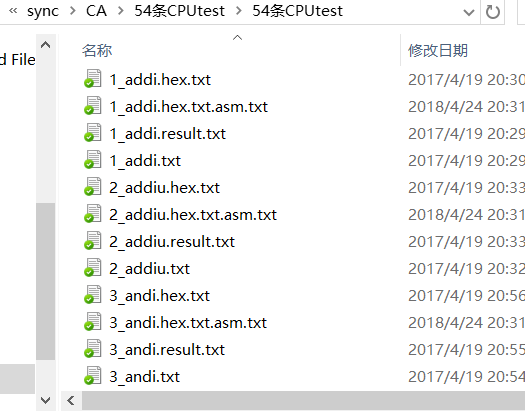
## 总体数据通路



# 测试/调试过程

* 使用MIPS246网站提供的“54指令CPU测试文件”进行测试，Testbench代码如下：

|  |
| --- |
| module sccomp\_dataflow\_oj\_tb(  );  reg clk\_in;  wire clk\_div;  reg rst;  wire [31:0] inst;  wire [31:0] pc;  wire [31:0] addr;    reg [31:0] instPrev;  reg [31:0] pcPrev;  wire cpuRunning;  integer file\_output;  reg cpuEna\_n = 1'b0;  sccomp\_dataflow uut(  .clk\_in(clk\_in),  .clk\_afterDiv(clk\_div),  .cpuEna\_n(cpuEna\_n),  .reset(rst),  .inst(inst),  .pc(pc),  .addr(addr),  .cpuRunning(cpuRunning)  );    initial begin  clk\_in = 0;  rst = 1;  file\_output = $fopen("results.txt");  #0  $readmemh("../../../Test/54\_div.hex.txt", uut.imem.array\_reg);  #5  rst = 0;  end        always #5 clk\_in = ~clk\_in;    reg cpuDonotRecordFirst = 0;    always @(negedge clk\_div) begin  instPrev <= inst;  pcPrev <= pc;  if (cpuRunning) begin  if(inst[0] === 1'bx)  cpuEna\_n <= 1'b1;  if(cpuDonotRecordFirst) begin  $fdisplay(file\_output,"pc: %h", pcPrev - 32'h00400000);  $fdisplay(file\_output,"instr: %h", instPrev);      $fdisplay(file\_output,"regfile0: %h",uut.sccpu.cpu\_ref.array\_reg[0]);  $fdisplay(file\_output,"regfile1: %h",uut.sccpu.cpu\_ref.array\_reg[1]);  $fdisplay(file\_output,"regfile2: %h",uut.sccpu.cpu\_ref.array\_reg[2]);  $fdisplay(file\_output,"regfile3: %h",uut.sccpu.cpu\_ref.array\_reg[3]);  $fdisplay(file\_output,"regfile4: %h",uut.sccpu.cpu\_ref.array\_reg[4]);  $fdisplay(file\_output,"regfile5: %h",uut.sccpu.cpu\_ref.array\_reg[5]);  $fdisplay(file\_output,"regfile6: %h",uut.sccpu.cpu\_ref.array\_reg[6]);  $fdisplay(file\_output,"regfile7: %h",uut.sccpu.cpu\_ref.array\_reg[7]);  $fdisplay(file\_output,"regfile8: %h",uut.sccpu.cpu\_ref.array\_reg[8]);  $fdisplay(file\_output,"regfile9: %h",uut.sccpu.cpu\_ref.array\_reg[9]);    $fdisplay(file\_output,"regfile10: %h",uut.sccpu.cpu\_ref.array\_reg[10]);  $fdisplay(file\_output,"regfile11: %h",uut.sccpu.cpu\_ref.array\_reg[11]);  $fdisplay(file\_output,"regfile12: %h",uut.sccpu.cpu\_ref.array\_reg[12]);  $fdisplay(file\_output,"regfile13: %h",uut.sccpu.cpu\_ref.array\_reg[13]);  $fdisplay(file\_output,"regfile14: %h",uut.sccpu.cpu\_ref.array\_reg[14]);  $fdisplay(file\_output,"regfile15: %h",uut.sccpu.cpu\_ref.array\_reg[15]);  $fdisplay(file\_output,"regfile16: %h",uut.sccpu.cpu\_ref.array\_reg[16]);  $fdisplay(file\_output,"regfile17: %h",uut.sccpu.cpu\_ref.array\_reg[17]);  $fdisplay(file\_output,"regfile18: %h",uut.sccpu.cpu\_ref.array\_reg[18]);  $fdisplay(file\_output,"regfile19: %h",uut.sccpu.cpu\_ref.array\_reg[19]);    $fdisplay(file\_output,"regfile20: %h",uut.sccpu.cpu\_ref.array\_reg[20]);  $fdisplay(file\_output,"regfile21: %h",uut.sccpu.cpu\_ref.array\_reg[21]);  $fdisplay(file\_output,"regfile22: %h",uut.sccpu.cpu\_ref.array\_reg[22]);  $fdisplay(file\_output,"regfile23: %h",uut.sccpu.cpu\_ref.array\_reg[23]);  $fdisplay(file\_output,"regfile24: %h",uut.sccpu.cpu\_ref.array\_reg[24]);  $fdisplay(file\_output,"regfile25: %h",uut.sccpu.cpu\_ref.array\_reg[25]);  $fdisplay(file\_output,"regfile26: %h",uut.sccpu.cpu\_ref.array\_reg[26]);  $fdisplay(file\_output,"regfile27: %h",uut.sccpu.cpu\_ref.array\_reg[27]);  $fdisplay(file\_output,"regfile28: %h",uut.sccpu.cpu\_ref.array\_reg[28]);  $fdisplay(file\_output,"regfile29: %h",uut.sccpu.cpu\_ref.array\_reg[29]);    $fdisplay(file\_output,"regfile30: %h",uut.sccpu.cpu\_ref.array\_reg[30]);  $fdisplay(file\_output,"regfile31: %h",uut.sccpu.cpu\_ref.array\_reg[31]);  end else  cpuDonotRecordFirst <= 1;  end else  cpuDonotRecordFirst <= 0;  end  endmodule |

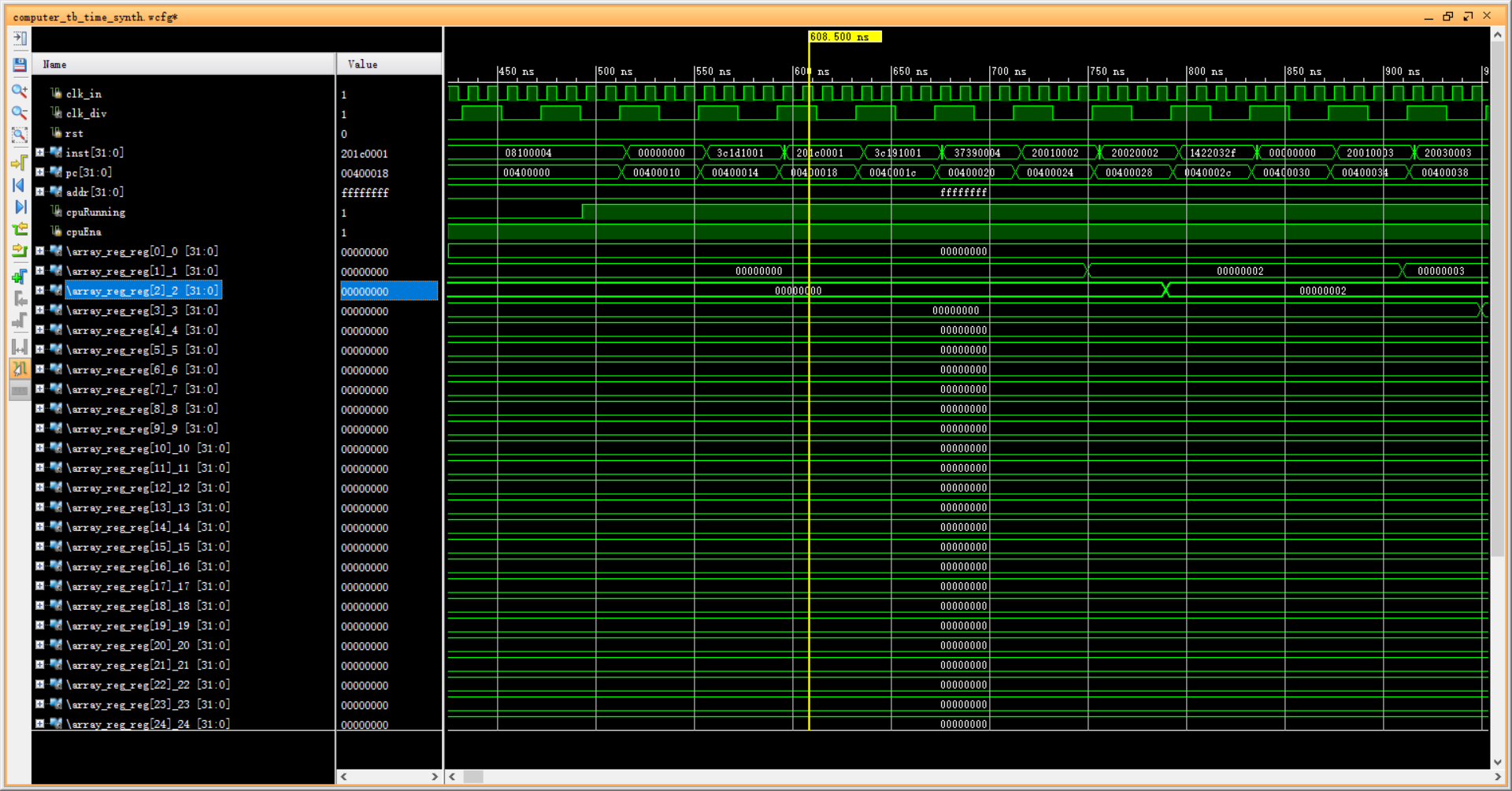


采用上述文件中的\*.hex.txt加载入IMEM进行测试；

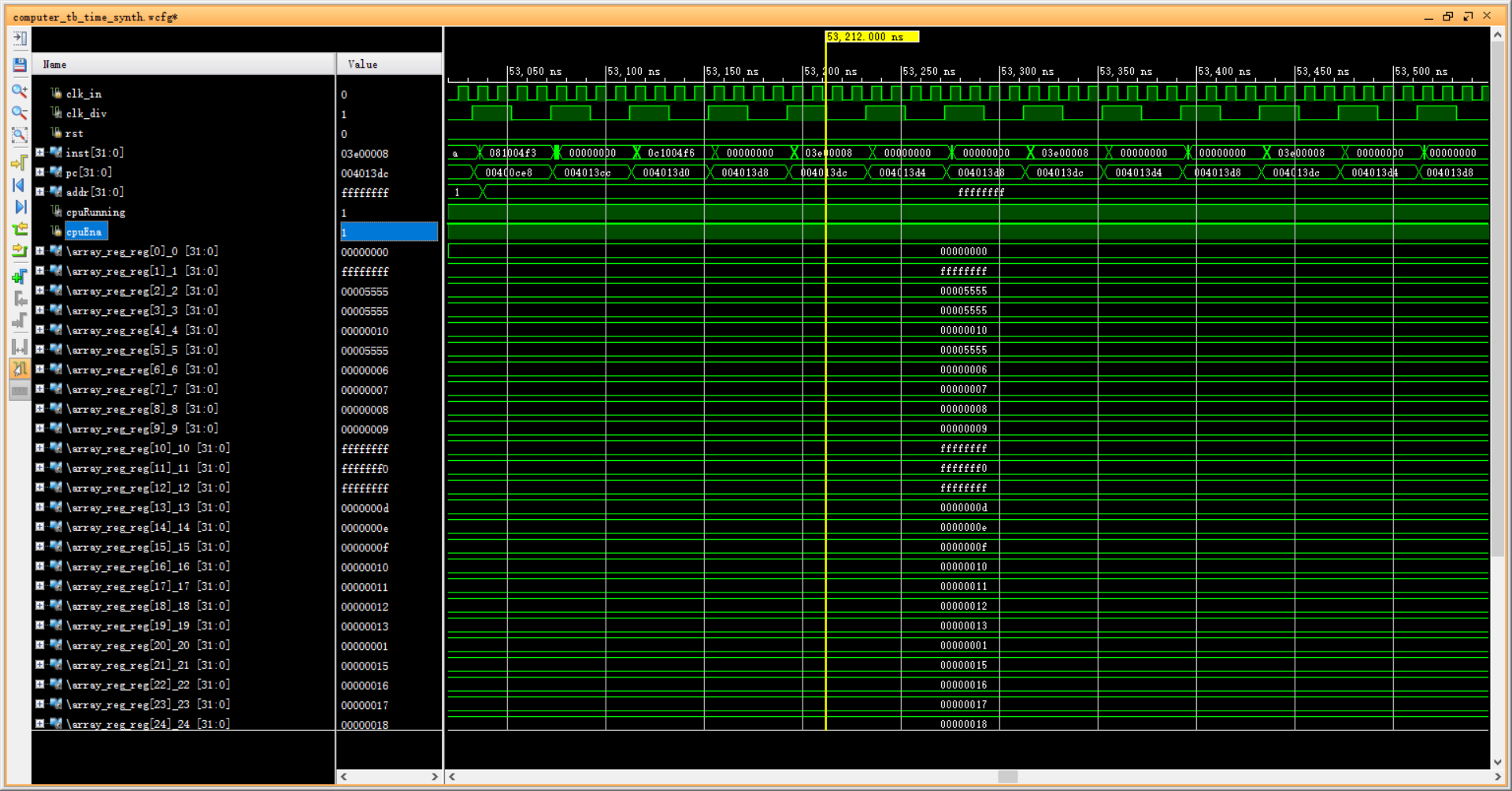
* 加载mips\_54\_mars\_simulate\_student\_ForWeb.coe，使用其中的汇编指，用综合后仿真的方法运行设计好的CPU；同时将它反汇编为mips\_54\_mars\_simulate\_student\_ForWeb.asm，加载入MARS（MIPS模拟器）。同时运行两者，观察两个CPU的状态，看是否相同。若相同，则这个CPU的设计达到了目标。

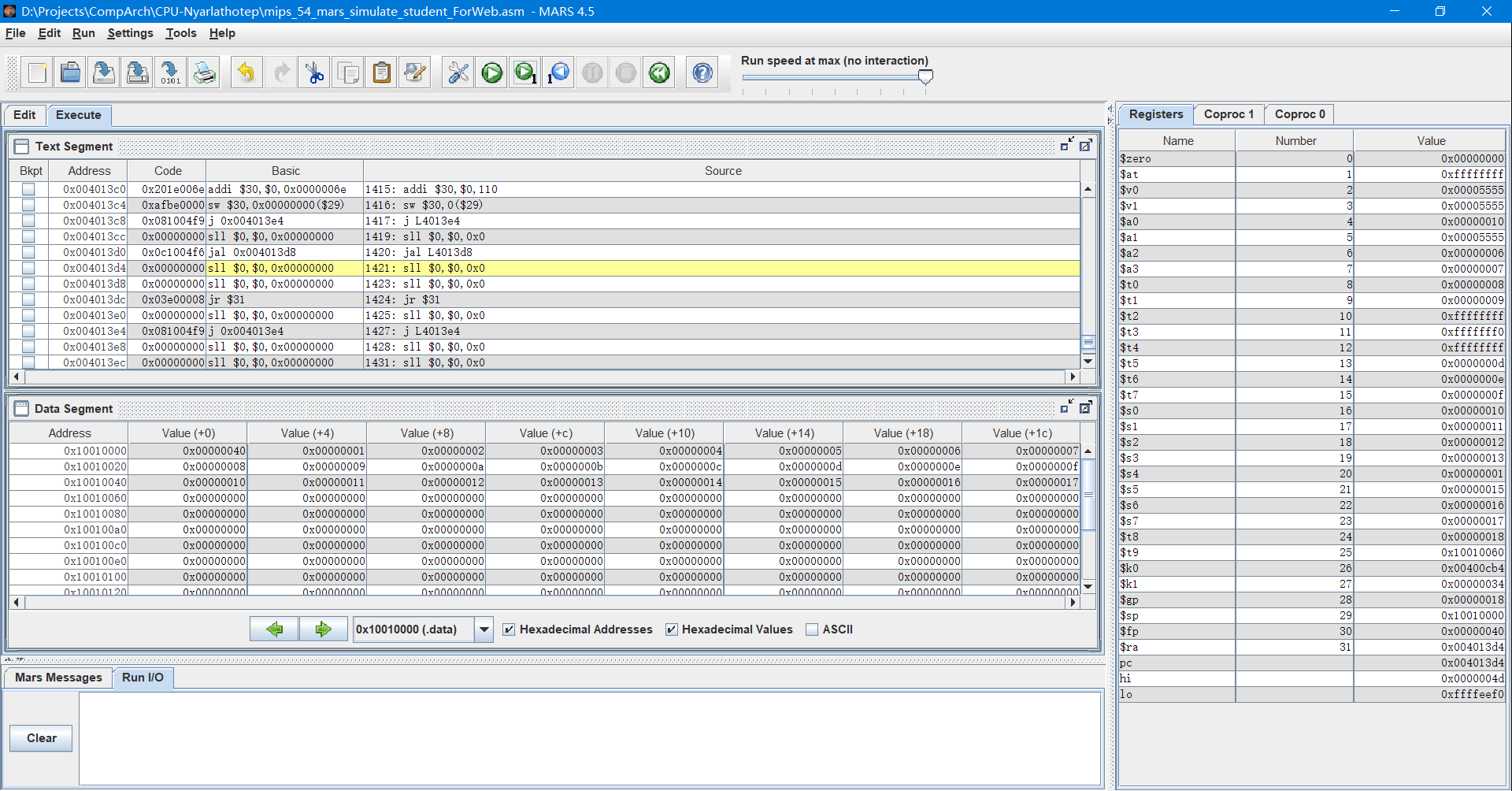
# 实验结果分析

* 本地测试，测试输出结果均与\*.result.txt符合。
* 综合后仿真测试：CPU在25MHz的仿真时钟信号下正常运行。



* MARS在运行反汇编后的代码时，运行完成后代码在0x004013d4和0x004013dc之间进入循环；而综合后仿真的结果也达到了这个状态。据观察，该汇编程序可以很好地检测CPU各条指令的运行情况，若有不正常的结果产生，会将程序流程导向一个表示错误的死循环。而本CPU没有进入任何一个错误死循环，说明CPU很好的完成了任务。





# 结论

可以使用Verilog HDL和IP核完成一个单周期54条指令MIPS CPU的设计。

# 心得体会及建议

本次CPU的制作过程耗时极长，过程复杂，锻炼了我的硬件思维和硬件设计能力，也让我充分了解到了CPU的运行机制。

建议：希望在布置CPU设计任务和公布验收过程时，提供的文档要尽可能详细精确，避免出现指令存储使用了Block Memory而非Distributed Memory导致在线检测无法通过的问题。