DDS Lab (Code: CS203)

Mini Project Evaluation

Course Faculty

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Basic Objectives

1. Basic objective of this mini project is to understand design, implementation, and synthesizing the different logic circuits or hardware modules using Xilinx ISE Design Suite or similar HDL simulator.
2. The mini project is primarily based on the various aspects such as reliability, quality of services via a fault detection and location in logic circuits.
3. Each assignment is dedicated to the testing of Stuck-at (SA0 and SA1) fault at different location on the I/O wires/lines of the logic gates of a logic circuit.

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Project Submission

- Only the group leader needs to submit their project for the group.
- Each project must be submitted in a compressed file.
- Submit the compress file in ZIP or RAR file (preferable).
- Submitted project in a compressed file must be renamed as Group#_Group-Leader-Roll#.zip or Group#_Group-Leader-Roll#.rar. **For example, Group-0_201CS000.zip** is the compressed project file submitted by Group-0 in which group leader's roll number is 201CS000.
- **The compressed file must be submitted at the IRIS module only and by the deadline.**
- **Deadline: 19th December 2021.**

Project Submission Contd...

- The compressed file must contain **TWO** folders.
  - **Folder-I:** This folder represents the Verilog/VHDL Source Code folder that contains the source code files, timing diagrams, logic diagrams, experimental results files, etc. generated on synthetization or simulation of the mini-project assignment using the Xilinx or similar HDL simulator.
  - **Folder-II:** This folder contains the Project report which must be prepared in the HTML environment.

Folder-I: HDL Source Code

- Each group must implement their mini-project assignment using the Xilinx or similar HDL simulator.
- Synthetization / simulation of your project must be done by considering stuck-at fault at multiple variations or locations of the I/O wires/lines of the logic circuit in your assignment.
- Consequently, the Folder-I must contain the source code files, timing diagrams, logic diagrams, results files, etc. generated on synthetization or simulation of the fault at different locations.

Folder-II: Report Preparation

- **Project report must be prepared in HTML environment.**
- The HTML code of your report should run on the stand-alone machine and looks like (on execution of your html code) the Virtual Lab environment where you are doing your CS203 Lab experiments.
- You may use CSS, JavaScript, etc. tools to make your report more interactive and near to Virtual Lab contents.
- Making your report more interactive and giving a feeling of Virtual Lab is more advisable and chance to earn higher score on the report.
- There is no page limit for your project report. However, writing unnecessary contents must be avoided.
- **A TEXT FILE must be included in the folder.** This file includes the system and software requirements to run your HTML code in a standalone machine.

Report Organization

Your project report can be organized as follows.

1. Group Information- group number, member's name and roll number.
2. Project Information- Project number and project title (or problem statement), aim/objective of this project, etc.
3. Theory related to your project assignment, Advantages and Disadvantages of your project, etc.
4. Simulation Procedure- Step by step description of the procedure how one can perform your experiment, Input selection, corresponding output, change in logic diagram, etc.
5. Demonstration of simulation procedure.

Report Organization Contd...

6. **Demonstration of your simulation procedure.** The demonstration must include necessary logic diagrams, truth-table, etc. This part should be as you execute/simulate your practice lab assignments at the Virtual Lab environment .
7. This simulation demonstration page should be designed in such a way that possible fault locations on the I/O wires of logic gates for SA0, SA1 or both faults and corresponding output via the truth table representation and the logic circuit diagrams can be observed.

Deadline

- You must submit the mini-project assignment on/before the deadline.
- No request will be entertained over the deadline if you will be unable to submit the assignment in due time.
- **Deadline: 19th December 2021.**

Project Evaluation

- Your project must be evaluated in two steps.
  - Step-I: Evaluation of Submitted Project.
  - Step-II: Presentation of the project followed by Q&A session.

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The End