Designing of Frequency divider circuit using 3-bit / Mod-8 / divide-by-8 asynchronous counter

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***Abstract*- Analog and digital applications require the use of frequency division to tailor the signal according to the circuit requirements. For this, we can use various toggling flipflops. In this paper, 'Divide by 8' frequency divider circuit is proposed using D-flipflop. With ADC, to feed the digital sequence to frequency divider circuitry, and DAC, to get final output in the same analog signal, the circuit is mixed signal design.**

Keywords– frequency divider, D flipflop, asynchronous counter

I. Reference Circuit Details

As shown in the figure we have three chain D-flipflops which acts as a negative-edge-triggered up-asynchronous counter (Ripple Counter).

The first D flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the complemented output of the preceding flip-flop. First flipflop toggles at the negative edge of external clock pulse. Second and third flipflops toggles at every negative clock edge of preceding output of the flipflop.

One flip-flop will divide the clock, $f$clk by 2, second flip-flops will divide $f$clk by 4 and thus after third flipflop, we will get frequency $f$clk divide by 8.

As shown in the block diagram, Analog-to-Digital Converter will convert input analog signal to the digital sequence. This sequence will act as the external clock. Frequency divider circuit will divide the input clock frequency by 8 as explained above. The output of this circuit will be converted into analog form using Digital-to-analog converter.

Example: Suppose input signal frequency is 1KHz the output signal frequency will be 125Hz.

II. Reference circuit diagram

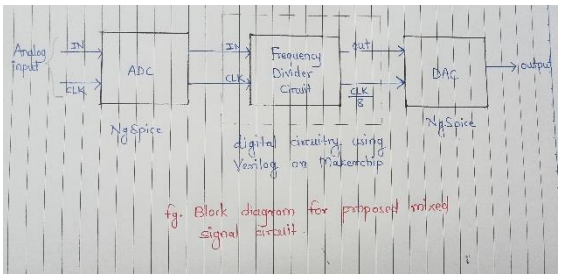

fig. Block diagram for proposed mixed signal circuit

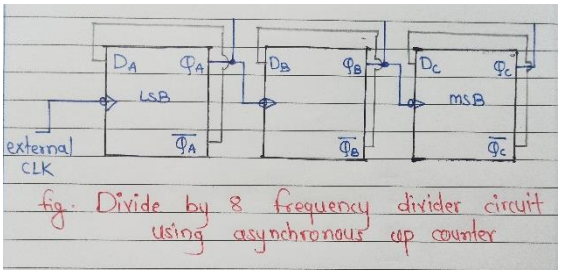

fig. Divide by 8 frequency divider circuit using asynchronous up counter

III. Reference waveform

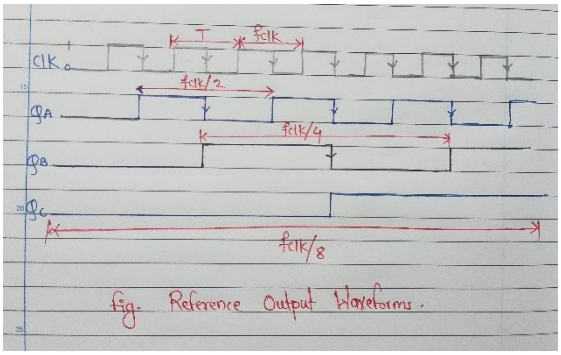

fig. Reference Output Waveforms.

References

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