JLR's Chiplet Challenge

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Team 15

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Abstract

This report presents a strategic analysis and innovative solutions to address the dual challenges articulated in JLR's problem statement. Part 1.1 of the problem statement requires us to focus on the imperative of adopting chiplet technology and offering a precise roadmap to maximize its value within the automotive context. At least two key applications have been identified, and our rationale underscores the transformational potential of chiplets. Part 2.1 of the problem statement requires us to delve into semiconductor communication technologies, emphasizing the intricacies of chiplet communication and the requisite intellectual properties (IPs). Our insights and solutions aim to empower JLR with a forward-thinking approach to leverage chiplets for automotive excellence.

1. Introduction

Between 2023 and 2037, automobiles will be transformed in almost every way to further improve efficiency, safety, driver experience and sustainability, as we drive toward a world in which vehicles are perfectly safe with zero emissions.
Vehicles will become more autonomous, sustainable, networked, and connected, driving special requirements for semiconductor devices and packaging.

To achieve this level of autonomy and connectedness, the vehicles of the near future must become a portable data center on wheels, requiring performance similar to modern high-performance computing systems with battery-operated energy consumption requirements.

While continued monolithic integration will partially enable these capabilities, advanced multi-die packaging will enable cost-effective interoperability and reuse. It is critical that these multi-die solutions scale to meet criteria like power and cost requirements for automotive systems.

Figure 1 illustrates the unique requirements of the automotive industry in this period of rapid evolution. [10]

2. Strategic Rationale for Chiplet Adoption

2.1. Why Chiplets?

Advantages of Chiplets over SoCs:

- Chiplets can be designed in the **optimum process node** (performance, power, cost) for the particular function and/or feature.
- Size and Yield – As monolithic silicon reaches it's reticle limitations, chiplets are much easier and cheaper to manufacture.
- Upgradability – Systems built with chiplets are easily upgradable. New chiplets can be introduced to replace existing components thereby **extending** the **lifespan** and capabilities of the system without requiring a complete redesign.
- The ability to **integrate** diverse and **potentially incompatible** semiconductor materials, such as GaN, SiC, Ga2O3, etc on a single package.[8]
- Chiplets provide **modularity** in the design due to which they can be reused in multiple products and projects.
- Enables choice: allows chipmakers/OEMs to select the right combination of chiplets for their needs, rather than be forced to choose a potentially less-optimum monolithic chip.
- Reduced NRE (non-recurring engineering) expenses in chiplet designs may be particularly advantageous for niche applications that require lower volumes of chips.
- **Lowers** the **entry** barrier to designing and selling silicon and **shortens** system development **cycle time**.
- Chiplets can incorporate **redundancy** in **safety critical** components in cars ensuring lower chances of total system failure.

	Autonomous	Networked	Sustainable	Connected
Purpose	ADAS and safety	Intra-vehicular networking and software-define vehicles	Carbon-neural transport: electrification and hydrogen	Infotainment and Vehicle-to-Everything (V2X)
Requirements and bottlenecks	Synthesize from multiple sensor sources: • Real-time environmental modeling • Path planning • Low-latency, high-bandwidth sensor-compute connectivity	More sophisticated zonal or domain controllers for more sophisticated sensor and response networks	Manage battery lifecycle: More complex local or cloud-connected battery management systems, aimed at increasing battery lifecycles	Increased connectivity to enable V2X features in communication with other vehicles, infrastructure, pedestrians, and external networks.

Figure 1: Requirements Unique to Automotive Trends [10]

2.2. *Where Chiplets?*

Based on the above-mentioned advantages that chiplets present over standard SoC architectures and designs, domains of interest with high scope of chiplet implementation have been identified, taking into account factors like: the extent of functional divisions and process node size optimization possible, computational or processing requirements, feature growth rate, and improvement demands.

Identified Automotive Domains:

- Advanced Driver Assistance System **(ADAS)**
- Infotainment
- Battery Management System **(BMS)**
- Motor and Motor Controller

The following presents a comprehensive analysis of each of the identified domains, containing a list of functions, a functional block diagram, and a discussion on the potential of chiplet adoption taking into consideration current and future automotive trends and requirements.

2.2.1. *Advanced Driver Assistance Systems (ADAS)*

An advanced driver-assistance system (ADAS) includes technologies that assist drivers with the safe operation of a vehicle. ADAS uses computer networks to enable **data-driven approaches** using sensors and cameras, to detect nearby obstacles or driver errors, and respond accordingly. ADAS can enable various levels of autonomous driving.

Some of the most common applications are

- **Adaptive Cruise Control (ACC):** ACC maintains a **safe following distance** from the vehicle in front by automatically adjusting the vehicle's speed. This is crucial for preventing rear-end collisions in highway traffic.
- **Blind Spot Monitoring (BSM):** BSM uses sensors to monitor the blind spots around the vehicle and provides warnings to the driver when another vehicle is detected in these areas. This helps prevent dangerous lane-changing maneuvers.
- **Adaptive headlights:** Adjusts the direction and **intensity** of the headlights according to the road conditions and traffic.
- **Intersection Collision Avoidance:** ADAS can assist in preventing collisions at intersections by **detecting cross-traffic** and providing warnings or taking evasive actions if necessary.
- **Emergency Call (eCall) Systems:** In the event of a serious accident, eCall systems can **automatically notify emergency** services and provide them with the vehicle's location, helping to reduce response times and potentially saving lives.
- **Automatic parking:** Steers the vehicle into a parking spot with minimal input from the driver.
- **Automatic Emergency Braking (AEB):** AEB systems detect impending collisions and **automatically apply the brakes** to prevent or mitigate the impact. This is especially critical in situations where the driver's reaction time is insufficient to prevent a collision.

Evolution of the ADAS: [10]

In the near future, as we target increased levels of autonomy, we will require better integration of high-capacity, emerging (e.g., reduced latency) memory, as well as other RF communication and ranging technologies.

The ADAS community aims to enable an **energy efficient**, fully connected, **cost-effective**, software defined, Level 5 autonomous vehicle with cost

Technology attribute	2023	2027	2032	2037
ADAS level (widely available)	Level 1-2	Level 2-3	Level 3-4	Level 5
Compute performance	250 TOPS	>2-5 TFLOPS	>10 TFLOPS	>100 TFLOPS
Network speed			10 Gbit/sec	100 Gbit /sec
Architecture and semiconductor requirements	Up to four-core, 28/40nm, embedded microcontrollers (MCUs)	Up to eight-core, sub-20nm MPUs	10nm, domain-specific architectures	Sub-5nm, domain-specific architectures
Advanced packaging and heterogenous integration	Monolithic designs or board-level integration; system-in-package (SiP) solutions too expensive	Reduced-cost, chiplet-enabled, SiP designs with better analog, HV, and RF integration	Better integration with high-performance, high-capacity memory below cost of monolithic designs	Reduced power and cost and higher-performance communication through more aggressive in-package integration
Higher voltage IO	Some logic platforms limited to 1.8V	Better chiplet integration for 2.5-3.3V capability with advanced logic nodes	Better chiplet integration for 2.5-3.3V capability with more advanced logic nodes	
High voltage analog	5V analog capability; specialized analog at ~80V; early adoption of 400V in EVs	Specialized analog at 120V; initial support for kV range for EVs	Increased support for high kV capability for EVs	

Figure 2: Automotive Requirements deployed in the median automobile over the next 15 years [10]

characteristics appropriate for a mass-market vehicle by 2035.

Attaining Level-5 of ADAS Autonomy would require:

Immense Processing Power: Processing power of the order of **100s** of **TFLOPS** will be required for sensor fusion across the hundreds of sensors being used and for specialized, domain-specific processing of sensor data to model the surrounding environment and to direct all aspects of low-latency vehicle control.

High Throughput: Given the large number of sensors required, new, domain-based and zonal architectures will require ∼**100Gb/s** intra-vehicle networks. Coupled with high-bandwidth wireless internet and infrastructure connections, these capabilities will also enable software-defined vehicles, and immersive infotainment.

Low Latency: Real-time functions require low-latency operations, requiring close proximity, high data-transfer bandwidth, and reduced power consumption and dissipation. As the number of sensors increases, fully networked vehicles will drive the need for high-speed PHYs (physical layers) and related hardware.

Figure 2 illustrates the requirement of shifting from monolithic designs to more advanced chiplet-based designs with rapid evolution in the ADAS and its levels of autonomy.

Use of chiplets in ADAS:

The use of chiplets in various subsystems of ADAS can have potentially beneficial applications such as the following:

1)Adaptive Cruise Control (ACC): Implementing chiplet technology in ACC systems can be highly efficient and beneficial in enhancing the performance, responsiveness, and intelligence of these ADAS systems.

Here's how chiplets can contribute to the efficiency and effectiveness of Adaptive Cruise Control systems

Advanced Sensor Integration: Chiplets can facilitate the integration of advanced sensor functionalities within ACC systems. By incorporating **specialized chiplets** to handle **sensor inputs**, it becomes possible to process data from various sensors such as radar, LiDAR, and cameras more efficiently. This enhanced sensor integration can improve the **accuracy** of **object detection**, enabling the ACC system to respond more effectively to changes in the surrounding environment, including the detection of vehicles, pedestrians, and obstacles. Thus they can handle data better than conventional SoC's

Real-time Data Processing: Chiplet technology enables the development of high-performance processing units that can handle complex algorithms and real-time data processing tasks. This

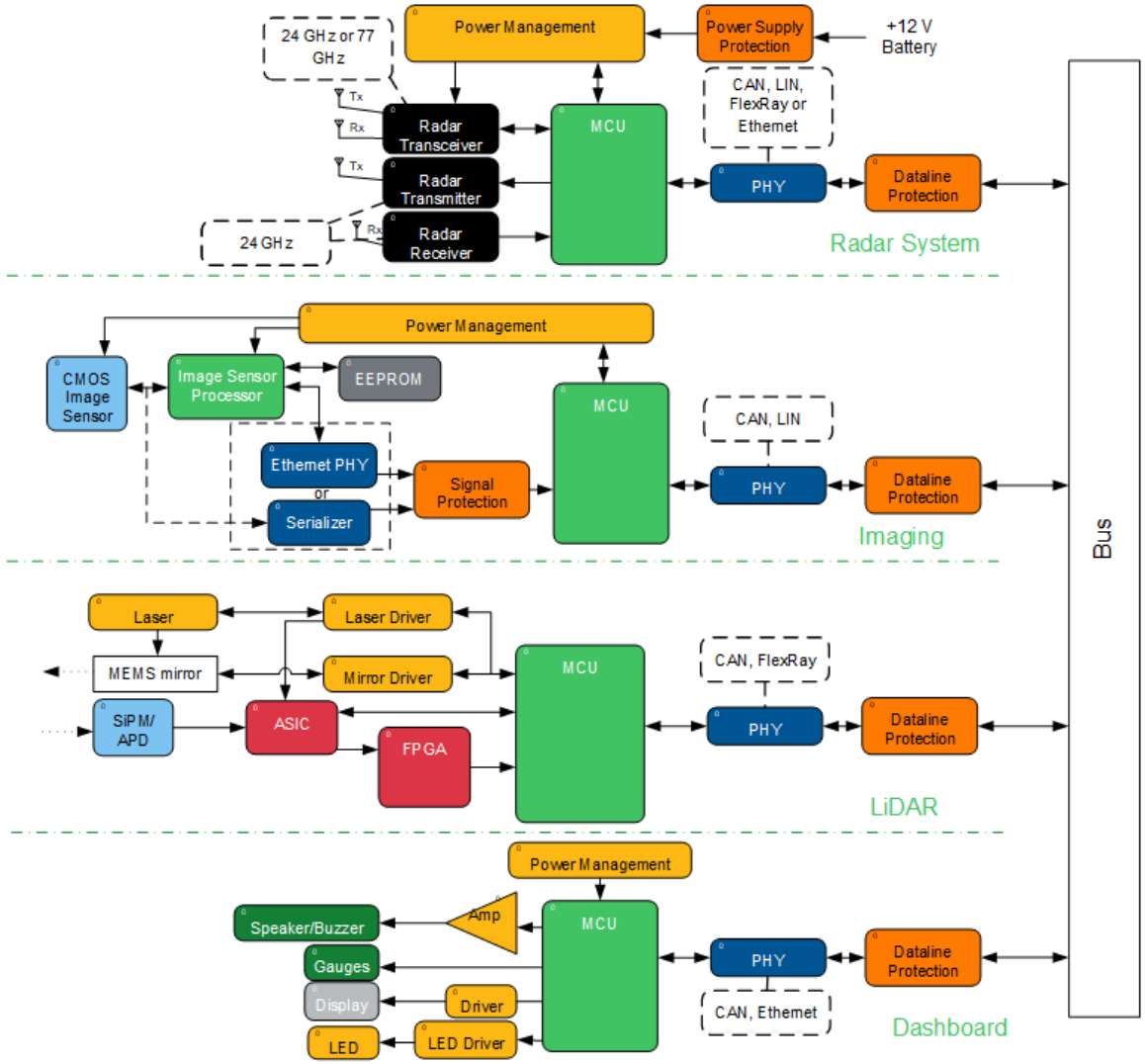

Figure 3: ADAS Block diagram.

capability is crucial for ACC systems, as it allows for **swift decision-making** and **precise control** of vehicle speed and distance from other vehicles. By leveraging chiplet technology, ACC systems can adapt to varying driving scenarios, traffic densities, and road conditions, thereby improving the overall efficiency and reliability of the cruise control function.

2) Blind Spot Detection System: Implementing chiplet technology in Blind Spot Detection (BSD) systems can be highly effective in enhancing the accuracy, reliability, and responsiveness of safety-critical automotive systems. This comes in handy, especially for safety-critical applications.
Chiplet based systems can incorporate redundancy for critical components. If a chiplet fails, a **backup chiplet** can take over its functions, **enhancing** the **fault tolerance** and safety of the ADAS system.

Intelligent Warning Systems: Chiplets can enable the implementation of intelligent warning systems within BSD systems, allowing for adaptive and **customizable warning strategies** based on the analysis of sensor data and vehicle dynamics. These intelligent warning features can optimise the BSD system's response to different driving scenarios, traffic conditions, and environmental factors, providing drivers with timely and context-sensitive alerts to **prevent potential collisions** or hazardous situations

2.2.2. Infotainment Systems

An automobile's infotainment system is a comprehensive system that seamlessly delivers a blend of information and entertainment content or services. Essentially, these in-built car computers integrate a diverse range of functionalities, from digital radios to in-built reversing cameras.

In-Vehicle Infotainment (IVI) refers to a fusion of vehicle systems that cater to providing entertainment and information to both the driver and passengers. This is achieved through various audio/video interfaces and control elements such as touch-screen displays, button panels, voice commands, and more.

According to market analysts, the global automotive infotainment market is projected to yield **$20,720 million** by **2030**, with an expected growth rate of **8.32% CAGR** [1]. Let's delve into these advanced technological systems a bit further.

The key components of an in-vehicle infotainment system are as follows:

Integrated Head Unit: This touch-screen-based, tablet-like device mounted on the vehicle's dashboard acts as a user-friendly control center for the infotainment system.

Heads-Up Display: A fundamental part of high-end infotainment systems, the automotive heads-up display projects real-time vehicle information onto a transparent screen integrated with the windshield. It serves to minimize driver distraction and provide vital details such as speed, navigation maps, electronic digital cluster data, climate control, and multimedia options.

High-end DSPs and GPUs to support multiple displays: Modern infotainment systems rely on robust automotive processors designed for advanced IVI systems. These processors can facilitate the display of content on multiple screens, providing an enriched in-vehicle experience for both drivers and passengers.

Operating Systems: Vehicle infotainment systems depend on operating systems capable of supporting connectivity, convenient functions, and the integration of downloadable software applications to expand the system's capabilities. Leading operating systems such as Android, Linux, QNX, and Windows dominate the infotainment segment.

CAN, LVDS, and other network protocol support: Infotainment system electronic hardware components rely on standardized communication protocols like Controller Area Network (CAN) to enable microcontrollers and devices to communicate without the need for a host computer.

Connectivity Modules: Infotainment systems incorporate GPS, Wi-Fi, and Bluetooth modules to establish connections with external networks and devices. These modules enable services such as navigation, internet connectivity, and seamless smartphone integration with the infotainment system.

Automotive Sensor Integration: Proximity sensors, gesture recognition sensors for ambient light detection, camera sensors, and various other in-vehicle sensors seamlessly integrate with infotainment systems to provide safety-related information to both the driver and passengers.

Digital Instrument Cluster: Advanced infotainment systems have revolutionized automotive cockpit designs, transforming traditional static displays into dynamic digital instrument clusters. These digital clusters display the vehicle's essential analog gauges, including the speedometer, RPM gauge, and odometer. They acquire data from the vehicle's ECU unit via OBD port-II and display it on the infotainment system's screen. As an integral part of the digital cockpit system, the instrument cluster is interlinked with other digital interfaces within the vehicle, such as the head-up display (HUD), HVAC, and infotainment systems.

Requirements of the Infotainment System and the potential of chiplet adoption

High Speed DSP: Almost all embedded system applications and features of the infotainment system in the coming years will demand digital signal processing (DSP) with higher capabilities in terms of speed, finer resolution, and greater accuracy. This correlation underscores the crucial role of high-performance computing in achieving high-speed digital signal processing. An example of this can be seen in the implementation of a Driver Drowsiness Monitoring System, which makes use of automotive-grade image sensors for capturing infrared images of the driver's eyes. This system incorporates patented pupil identification technology and a high-speed digital signal processor to analyse and identify instances of driver drowsiness or distraction. [5].

Chiplets for high performance computing: The performance requirements necessitate the integration of a substantial amount of compute and memory into a single package. Rather than opting for a monolithic System on Chip (SoC), AMD proposes a different approach, leveraging advanced die-stacking technologies to break down the EHP into smaller components, which include active interposers and chiplets. These chiplets can house multiple GPU compute units or CPU cores. Notably, the chiplet approach differs from traditional multi-chip module (MCM) designs in that each individual chiplet is not a complete chip.

For instance, the CPU chiplet contains CPU cores and caches but lacks memory interfaces and external I/O. A monolithic SOC imposes a single process technology choice on all system components. With chiplets and interposers, each discrete

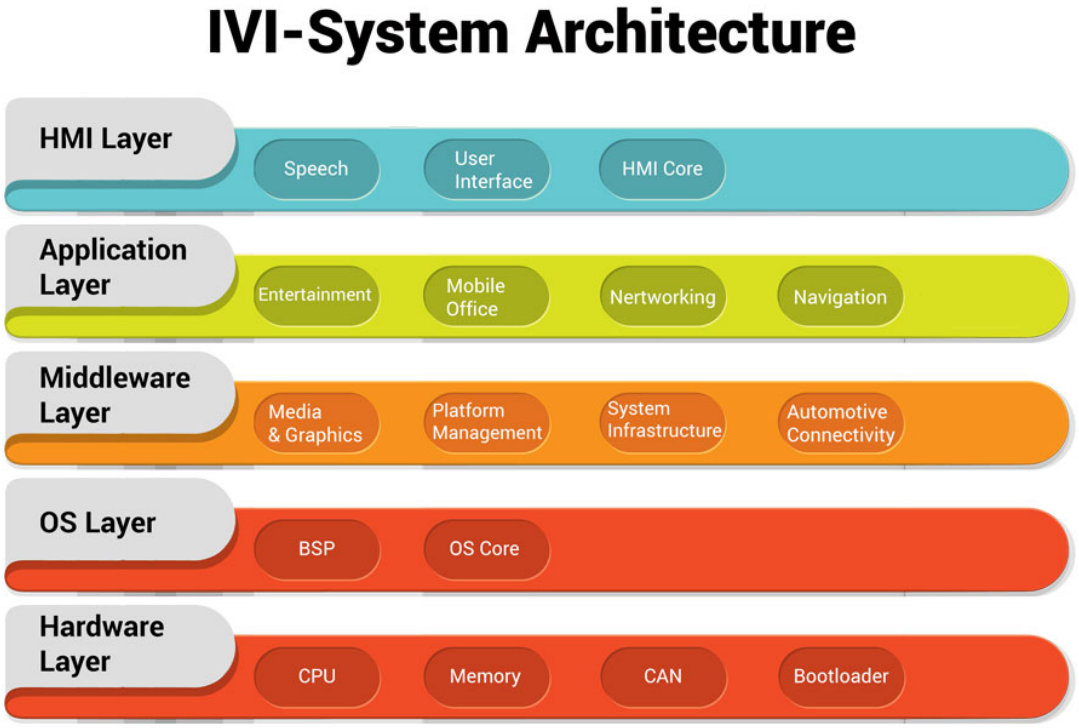

Figure 4: IVI Functional Blocks

piece of silicon can be tailored and optimized for its specific functions. This approach is expected to result in higher yields for smaller chiplets due to their size. When combined with Known Good Die (KGD) testing, these chiplets can be assembled into larger systems at a reasonable cost.

This decomposition of the EHP into smaller pieces is expected to facilitate silicon-level reuse of intellectual property (IP) [6].

High resolution touch screen: It is true that chiplets, which are small integrated circuits, can be used in a variety of applications, including in the context of electric vehicles and their touch-screen displays. By incorporating chiplets with a crystalline substrate, manufacturers can achieve higher performance active components compared to devices utilizing thin-film amorphous or polycrystalline silicon. This results in smaller active elements, such as transistors, leading to a reduction in circuitry size. In the context of electric vehicles, these chiplets could potentially be utilized in touch-screen displays to enhance the efficiency and performance of the real-time information systems that monitor battery status, charging points, and energy consumption. Similarly, in autonomous vehicles, chiplets can contribute to the development of touch-screen interfaces that facilitate seamless communication between passengers and the vehicle's autonomous systems. The use of chiplets with a crystalline substrate can offer several advantages, including improved overall performance and compact design, which can be particularly beneficial in the development of advanced technological systems such as those found in electric and autonomous vehicles.

Analog and digital tuners for multi-standard radio reception: Some of the challenges faced while using 3D monolithic integration for RF/mm-wave applications are poor heterogeneous integration flexibility in materials and devices, high design complexity and poor thermal management. This method of integration is widely studied to overcome problems such as increased interconnect delays for digital applications and other scaling limitations. When compared polylithic integration is better in addressing these challenges than monolithic integration while maintaining the same performance. Chiplets when used in radio applications can be designed to perform specific tasks within the system and can serve various purposes such as filtering, modulation/demodulation, amplification, signal processing and other RF functions. [11]

Benefits of using chiplets in Android Auto and Apple CarPlay instead of SoC's: Chiplets are connected by ultra-fast and coherent chiplet interconnect technology aiding in the implementation of fast and efficient compute systems. Vehicles

are becoming more software-defined, multimedia-rich and have incredible graphics and audio. AI technologies will define a major part of the user experience requiring a tremendous amount of processing with each added feature. The GPU chiplet brings several key advantages and benefits to the vehicle's entertainment system like improved graphics processing, optimized performance and efficiency, enhanced AI and machine learning capabilities. Most cutting-edge user-interface platforms include features that will ensure drivers remain wirelessly connected with high-speed telematics and Wi-Fi networking. [9]

Technologies used in parking assistance:

1. Neural networks that drive these automated systems often require significant processing power and digital signal processing. Chiplets offer a modular approach to AI hardware design, allowing for specialization and customization of components [7]

2.Chiplets can be used in Global Po- sitioning System (GPS) technology to enhance its performance, flexibility, and efficiency, GPS is critically reliant on RF (radio frequency) technology. Chiplets can be used to enhance this feature .[11]

2.2.3. Motor and Motor Controller

An electric vehicle's motor controller is a combination of power electronics and embedded microcomputers that effectively converts the energy stored in the batteries into motion. The Motor controller is a crucial component in electric vehicles. Following are some of its functions:

- **Command Processing:** The Motor controller receives input commands from various vehicle interfaces, such as the Throttle, Brake, and Forward/Reverse control switches. These commands are essential for controlling the vehicle's movement and ensuring a smooth driving experience.
- **Motor Control:** One of the fundamental functions of the Motor controller is to manage the electric motor's speed, torque, and direction. By precisely controlling these parameters, it enables the vehicle to accelerate, decelerate, and change direction as per the driver's inputs.
- **Inverter:** In an electric vehicle, the power source is typically a high-voltage DC battery. However, electric motors operate on AC power. The inverter within the Motor controller converts the DC power from the battery into the AC power required by the electric motor. This conversion process involves changing the frequency and voltage to suit the motor's needs.
- **Energy Management:** Effective energy management is critical for electric vehicles. The Motor controller plays a significant role in optimizing energy consumption and ensuring that the motor operates within **safe** and **parameters.** It can adjust the motor's performance based on various driving scenarios, helping to maximize the vehicle's range and efficiency.

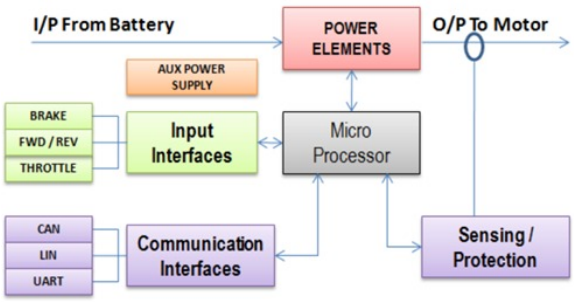

Figure 5: Motor Controller Functional Blocks.

Potential Of Chiplet Adoption

The motor system usually consists of discrete controller units whose efficiency and control parameters **do not change** much on **transitioning to chiplets**. Following are some other challenges

- **Interconnect Complexity:** Managing the interconnects between chiplets, especially in **high-performance** applications, can lead to **increased complexity** and potential signal integrity issues. Careful design and layout are required to avoid problems with signal integrity and electromagnetic interference (EMI).
- The use of chiplets necessitates the requirement for a specific type of packaging which may **not be suited** for **high power applications** and this causes the chiplet to exhibit abnormal behaviour in the high voltage and temperature range. As the motor control system of a car deals with the extremes in terms of power, so implementing chiplets in the motor controller doesn't give us any substantial gain.
- **Higher Development Costs:** Developing a chiplet based motor control system can be **more costly** in terms of initial development and validation. Designing, testing, and qualifying multiple chiplets may require a **larger investment** of time and resources.
- **Thermal Management:** Managing heat dissipation in a chiplet-based motor control systems can be extremely challenging due to

the compact and densely integrated nature of chiplets. Effective thermal management is essential to prevent overheating.

*2.2.4. **Battery Management System (BMS)***

A Battery Management System (BMS) is a specialized technology designed to monitor and control a battery pack, which is an assembly of multiple cells in a grid-like configuration (i.e., series and parallel) to provide a specific range of voltage and current for a predetermined duration against expected load scenarios.
Typical functions carried out by a BMS are:

- Battery monitoring and protection (temperature, overcurrent, etc.)
- State Estimations i.e. State of Charge (SoC), State of Health (SoH), etc.
- Cell balancing: equalizing the SoC and voltage of each cell.
- Efficient charging & discharging.

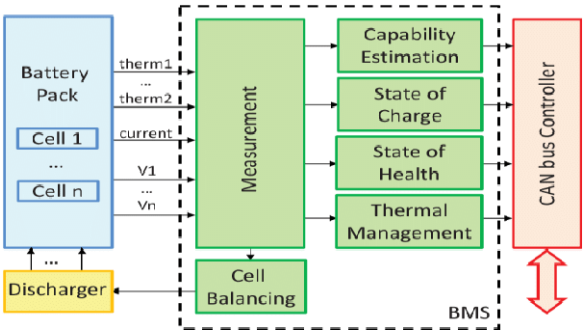

Figure 6: BMS Functional Blocks.

Where can we implement chiplets:
Implementing chiplets in a Battery Management System (BMS) involves integrating semiconductor devices, typically small chips or microcontrollers, into the BMS design to perform specific functions or tasks. It is possible to disassemble the various functional components of a BMS and individually execute each of them using specialized chiplets. For instance, employing distinct chiplets for tasks like cell balancing, state of charge calculation, and so on.

Differences over the current approach:
Incorporating chiplets for state estimations, especially when considering a data-driven approach like **neural networks** can prove to be a powerful method, however, the accuracy is severely impacted by the availability of sufficient data to cover a wide operating range and how powerful the platform of implementation is [12].

It is also important to note that conventional methods for state estimations, such as **Sigma Point Kalman Filtering** for State of Charge (SoC) measurements and weighted least squares for State of Health (SoH) calculation, already provide a high level of accuracy. Kalman filters are capable of operating with much less data and under unpredictable scenarios [12].

Transitioning to a data-driven approach can introduce unnecessary constraints and complexities for an on-chip implementation.
Integrating multiple chiplets into a **coherent BMS** can be challenging and may require advanced packaging and interconnect technologies. Ensuring that all chiplets work seamlessly together can be complex and costly.
As a BMS often operates in a real-time environment, additional interconnects used in chiplet-based BMS can introduce latency in data communication which may impact real-time monitoring and control.

*2.3. **Final Conclusion and Comments***

From the above discussions and comparisons, the BMS and Motor Controller are components that either do not provide significant improvement with the adoption of chiplet technologies or are too complex to implement leading to a larger list of drawbacks in terms of manufacturing costs, interconnect complexities and packaging difficulties if not implemented well.

The ADAS and Infotainment domains fit well into the narrowed scope, both being fast-growing areas with ever-increasing feature adoption rates. With increased levels of autonomy, cloud-based vehicle data logging and service & update implementations, intra and inter-vehicle communication, these domains will require immense improvements in terms of processing power, information throughput, latency and power efficiency in the near future. These are areas that are best able to utilize the wide array of advantages that chiplets provide: improved optimization of die process node sizes and the high upgradability of chiplet-based systems, further accelerating growth in the automotive industry.

3. Communication Technologies and Intellectual Properties for Chiplet Integration

As in a chiplet-based approach, various chiplets of different operating domains like analog, digital, RF, etc are integrated. Hence, communication technologies are used for reliable and power efficient communication between various chiplets of different types and speeds.

In chiplet-based designs, inter chiplet communication is done using D2D interface. A D2D (die-to-die) interface is a functional block that provides the data interface between two silicon dies (chiplets) within a package. The D2D creates a reliable link and is generally described as the **PHY (physical layer)** and the **controller**. Point to remember before choosing a D2D IP is that for D2D communications, there are a variety of channels or substrates that can be used to communicate depending on the packaging technology, like an organic substrate for 2D packaging or an interposer for 2.5D. This will impact the particular D2D interface IP since the channel will be different and will likely require modifications to the interface, for example, the bump pitch or the signal loss.

*3.1. **Summary of Leading Communication Technologies***

*3.1.1. **Leading Communication Technologies***

Organisation	Intel	AMD	TSMC
Packaging	EMIB	MCM	CoWoS
Interconnect	AIB 1.0	IF	LIPINCON
Throughput	2 Gb/s	10.6 Gb/s	2.8 Gb/s
Latency	5 ns	9 ns	14 ns
Power	1.2 pJ/bit	2 pJ/bit	0.56 pJ/bit

Table 1: Comparison of Various In-Use D2D Communication Technologies [4]

- TSMC communicate between L3 cache and CPU using **LIPINCON (Low-voltage-In-Package-INterCONnect) interfaces.** One interface serves as a master for CPU communication to L3 while the second is a slave for the opposite direction.
- NVIDIA announced **NVIDIA NVLink C2C**, an ultra-fast chip-to-chip and die-to-die interconnect that allows custom dies to coherently interconnect to the company's GPUs, CPUs, DPUs, NICs and SOCs.
- **AMD's Infinity Fabric** on package SerDes provides a means for communication on short package routes (10-20mm) between the IOD (input/output die) and CCD(core chiplet die).
- **Intel's AIB standard** is an open-source, roya- lty-free PHY-level standard for connecting multiple semiconductor die within the same package.

These are the proprietary D2D interface that will mostly focus in homogeneous chiplet design (Intel's AIB may be integrated heterogeneously). A comparison of the proprietary communication technologies has been provided in Table 1. For heterogeneous integration, an open standard communication technology is required. Hence, there are **other standard open communication technology** IPs for PHY viz. OpenHBI, BoW, AIB, are available that can be used with customised controller IPs according to our chiplet communication requirements. Other than all this, **UCIe (Universal Chiplet Interconnect Express)** is an open specification for a D2D interface between chiplets co-developed by AMD, Arm, Google Cloud, etc. It defines standard UCIe PHY (physical layer) and UCIe Controller (includes die-to-die adapter and protocol layer) as well as IPs and procedures for compliance testing. UCIe is the currently the most prominent standard for die-to-die communication with 2 existing specifications, UCIe 1.0 and 1.1. .With the UCIe 1.1 specification optimized for automotive applications.

*3.1.2. **Standard Open Communication Tech***

Various open standard generic parallel interfaces are available that provide the PHY layer specifications for the interconnection. An adapter layer is then used to interface with the upper layers (protocol layers). As a result, the system implementation becomes independent of the protocol used for each application. A brief description along with specification comparision of these protocols is given below.

Organisation	UCIe Advanced	UCIe Standard	OCP	OCP	Chips Alliance
Packaging	2D, 2.5D, Bridge	2D	2D, 2.5D, 3D	2D, 2.5D	2D, 2.5D, Bridge, 3D
Interconnect	UCIe	UCIe	OpenHBI 1.0/2.0	BoW	AIB
Edge Density (Tbps/mm)	5.2	0.9	4	0.44	1.64
Latency (ns)	2	2	4	5	5
Power (pJ/bit)	0.6-0.5	1.0-0.5	0.4	1.0-0.5	0.5

Table 2: Comparison of Various Open D2D Communication Technologies [3]

- **Bunch Of Wires (BoW):** BoW is an energy-efficient, easy-to-use PHY interface specification for die-to-die (D2D) parallel interfaces that can be implemented in organic laminate or advanced packaging technologies.
- **OpenHBI:** OpenHBI is a symmetric, multichannel chip to chip interconnect supporting wafer level integrated fanout or Si-interposer layer for a high density of the interconnects. The basic building block of the interconnect is a DWORD which consists of outputs/inputs 48 signals of which upto 42 are data signals, the other signals are used

for parity check, databus inversion, Lane repair support. It supports a protocol layer of PCIe, CXL and CCIX. The memory chiplets with JEDEC HBM3 interoconnects are also supported by this interconnect technology. It has a data transfer rate of 8GT/s for a reach within 3mm length and consumes 0.4pJ per transmitted bit.

- **XSR SerDes:** It is a high performance, low Latency PHY to connect between chiplets as well as chiplets to optical engine. Developed by Optical Internetworking Forum (OIF)
- **Advanced Interface Bus (AIB):** AIB is a physical-layer (PHY) specification.

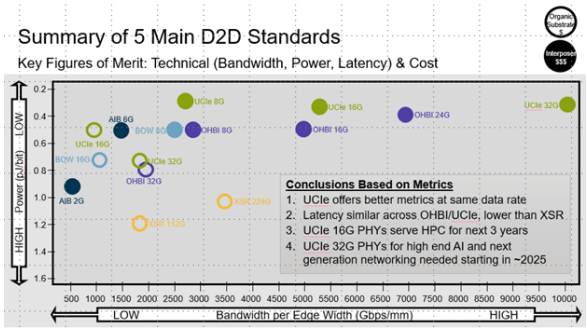

Figure 7: Power-Bandwidth Comparison of D2D IPs [13]

3.1.3. ***UCIe***

UCIe[2] is a multi-layer multi-protocol communication technology with well defined die-to-die interfaces. The three major layers defined in the UCIe stack are **physical layer, die to die adaptor** and **protocol layer**.

- **Protocol Layer:** The protocol layer mostly focuses on communicating between various internal sub-systems of the given die. It uses IPs like PCIe, CXL, CCIX along with IPs for streaming like AMBA CHI. It uses FLIT Aware Die to Die Interface(FDI) for signaling interface.
- **Die-to-Die Adapter Layer:** The D2D interface has a signaling interface between various protocols like FLIT aware die-to-die interface (FDI) and Raw data die-to-die interface (RDI).
- **Physical Layer:** Physical interconnect signaling interface with usage models for single module and multi-module. It has 16 standard links and upto 64 links in advanced packages. It has a main band interface for the

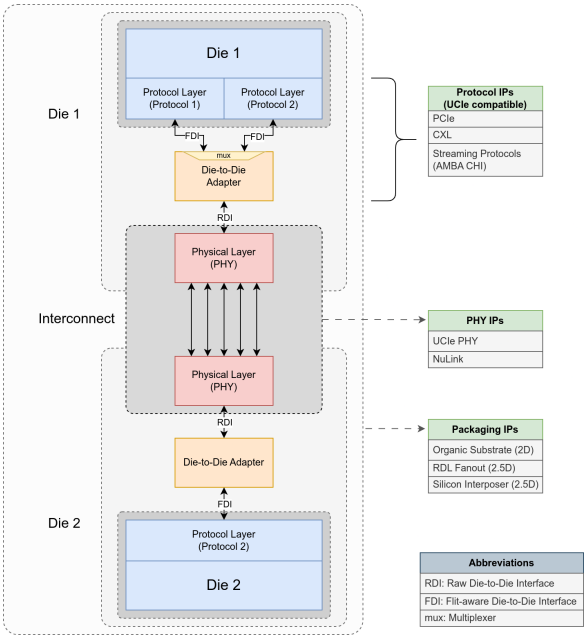

Figure 8: UCIe 1.1 Flow Diagram.

datapath and a sideband interface for the control. It has lane-repair and lane reversal capabilities in case the interconnecting lane gets corrupted.

3.2. ***Chiplet communication IPs***

Intellectual properties or IPs mean a design or verification unit that is pre-packed and available for licensing. Semiconductor IP (SIP) and Design IP (DIP) are generally the same thing and often just referred to as IP, IP blocks, or IP cores. It is a piece of the design, such as a processor, that has been pre-verified and can be included in someone else's design. We have explained what available can be used based on the type of communication chiplets (CPU, GPU, memory, etc.).

IPs for standard open communication technologies other than UCIe are listed below:

- **BoW Base:** BoW-Base is designed for the transmission distances below 10 mm and uses unterminated unidirectional interfaces.
- **OpenHBI 1.0 and 2.0:** Can be used in high bandwidth memory applications (using HBM).
- **AIB-O, AIB-1.0 and 2.0:** AIB is ideal for designing SoCs, FPGAs, SerDes chiplets, high-performance ADC/DAC chiplets, optical networking chiplets and more. AIB 2.0 has more than six times the edge bandwidth density of AIB 1.0 through increases in the per-wire line rate and the number of IOs per channel.

UCIe compatable IPs are listed below:

- **PCIe:** For general I/O and communication.
- **CXL:** We have **CXL.io** for I/O and peripherals, **CXL.cache** for applications like efficient and coherent caching and **CXL.memory** to access device attached memory.
- **CCIX:** Enables multiple devices to share data in a cache coherence manner for acceleration.
- **AMBA CHI:** Unified interface for device attach (compute, accelerators, memory)
- **Nulink:** NuLink PHY is more scalable and cost-efficient than interposers

Automotive applications in ADAS and Infotainment critically require high memory bandwidth, high performance and high power efficiency. It is also essential that the IPs we choose are widely accepted in the market to foster modularity and enable choice.

*3.3. **Required IPs for Key Applications***

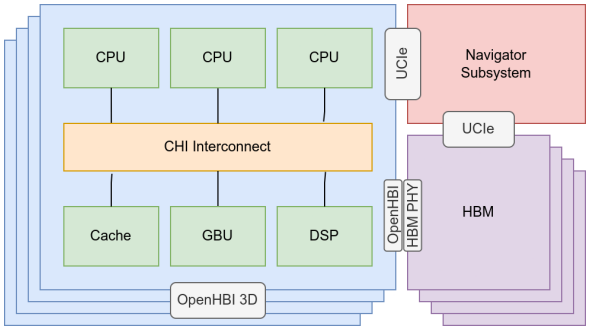

Figure 9: Example use of interconnects and chiplets in automotive chips

- Different communications IPs each have different advantages and disadvantages over each other.
- UCIe has a good latency, and bandwidth and has well-defined and self-sufficing IPs, however, it does not support 3D IC packaging technology and requires an expensive interposer for gaining a good FoM.
- The later versions of OpenHBI support 3D IC packaging technology and have a good FoM for its power consumption, bandwidth and length of interconnect. However, it only has its physical protocol layer and doesn't have its own protocol layer.
- Hence our solution will focus on optimizing our package by leveraging the 3D packaging capabilities of OpenHBI for communication between the compute and accelerate units which will be stacked in 3D.
- The UCIe technology will be used for communicating between the various different subsystems of different domains like analog, computing, memory, RF ,etc(As shown in Figure 9).
- As OpenHBI supports the protocols of the UCIe technology, the unit which is on the interface of the two technologies will use two separate physical layers.
- Similarly we can use HBM memory chiplets, which have high bandwidth and low latency. Such chiplets can be stacked in 3D for efficiency in space and since the OpenHBI physical layer supports communication from HBM physical layer, we will use OpenHBI physical layer in the compute chiplets for communicating with the memory having HBM physical layer.

Different communications IPs each have different advantages and disadvantages over each other.

3.4. Conclusion

In the realm of chiplet integration, effective communication technologies are crucial for reliable and power-efficient interactions between diverse chiplets of varying functionalities such as analog, digital, and RF domains. This is achieved through die-to-die (D2D) interfaces, where the physical layer (PHY) and controller play key roles. Proprietary D2D interfaces from major players like Intel, AMD, and TSMC exhibit differences in packaging, interconnect, throughput, latency, and power. For heterogeneous integration of chiplets, an open standard is necessary for interoperability . Various standard open communication technologies, such as BoW, OpenHBI, OCP, and AIB, are compared. UCIe stands out as a multi-layer, multi-protocol communication technology with distinct layers for the physical interface, die-to-die adapter, and protocol. These standards can be used in a hybrid fashion according to our requirements for PHY and controller for D2D interface between 2 particular chiplets in the topology of a chiplet based SoC.

References

[1] *Automotive Infotainment Market Report*, 2022.

[2] *Building an open ecosystem of chiplets for on-package innovations*, 2022.

[3] *Design and technology spaces for heterogeneous chiplet integration*, https://www.gsaglobal.org/wp-content/uploads/2022/09/System-3-Yujeong-Shim-WISH-Design-Spaces-for-Chiplets.pdf, 2022.

[4] *DRA75x, DRA74x Infotainment Applications Processor Silicon Revision 2.0*, https://fuse.wikichip.org/news/2446/tsmc-demonstrates-a-7nm-arm-based-chiplet-design-for-hpc/, 2019.

[5] *Driver Drowsiness Monitoring*, https://www.faststreamtech.com/industries/smart-automotive-solution/driver-monitoring-system/.

[6] D. P. GARROU, *HPC, chiplets and interposers*, https://sst.semiconductor-digest.com/2017/06/hpc-chiplets-and-interposers/, 2022.

[7] *IET Intelligent Transport Systems, Vol. 12, Issue 8*, 2018.

[8] *Is GaN Replacing Silicon? The Applications and Limitations of Gallium Nitride in 2019*, https://www.allaboutcircuits.com/news/GaN-replace-silicon-applications-limitations-gallium-nitride/, 2019.

[9] *MediaTek Partners With NVIDIA to Transform Automobiles With AI and Accelerated Computing*, https://blogs.nvidia.com/blog/2023/05/28/mediatek-intelligent-cabin-solutions/, 2023.

[10] *Microelectronics and advanced packaging technologies roadmap* (Semiconductor Research Corporation, 2023).

[11] *Polylithic Integration for RF/MM-Wave Chiplets using Stitch-Chips: Modeling, Fabrication, and Characterization*, 2020.

[12] H. B. Sassi, F. Errahimi, N. Es-Sbai, and C. Alaoui, *A comparative study of ANN and Kalman Filtering-based observer for SOC estimation*, IOP Publishing, 2018.

[13] *Synopsys Protocol Verification Solution for UCIe 1.0*, https://blogs.synopsys.com/vip-central/2022/07/07/synopsys-protocol-verification-solution-for-ucie-1-0/, 2022.

ABBREVIATIONS	
AC	Alternating Current
ACC	Adaptive Cruise Control
ADAS	Advanced Driver Assistance System
AEB	Automatic Emergency Braking
AI	Artificial Intelligence
AIB	Advanced Interface Bus
AMBA CHI	Advanced Microcontroller Bus Architecture Bus Protocol Coherent Hub Interface
ANN	Artificial Neural Networks
ASIC	Application-Specific Integrated Circuit
BMS	Battery Management System
BSM	Blind Spot Monitoring
BoW	Bunch of Wires
CAGR	Compound annual growth rate
CAN	Control Area Network
CCD	Core Chiplet Die
CMOS	Complementary Metal Oxide Semiconductor
CoWoS	Chip on Wafer on Substrate
CXL	Compute Express Link
D2D	Die to Die
DC	Direct Current
DIP	Design IP
DSPs	Digital Signal Processors
eCall	Emergency Call
ECU	Electronic Control Unit
EEPROM	Electrically Erasable Programmable Read-only Memory
EHP	Enormous Heterogenous Processors
EMI	Electro-Magnetic Interference
EMIB	Embedded Multi-die Interconnect Bridge
FDI	FLIT aware D2D Interface
FLIT	Flow control Unit
FPGA	Field-programmable gate array
FoM	Figure of Merit
Ga2O3	Gallium Oxide
GaN	Gallium Nitride
GPUs	Graphics Processing Units
HUD	Head Up Display
HV	High Voltage
HVAC	Heating, Ventilation and Air Conditioning
IF	Infinity Fabric
IOD	Input Output Die
IPs	Intellectual Properties
IVI	In Vehicle Infotainment
KGD	Known Good Die
LiDAR	Light Detection And Ranging
LIN	Local Interconnect Network
LIPINCON	Low-voltage-In-Package-INterCONnect
LVDS	Low Voltage Differential Signaling
MCM	Multi Chip Module