

Electronics and Communication Systems

Electronics Systems

Master Degree in **Computer Engineering**

<https://computer.ing.unipi.it/ce-lm>

Luca Fanucci

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Massimiliano Donati

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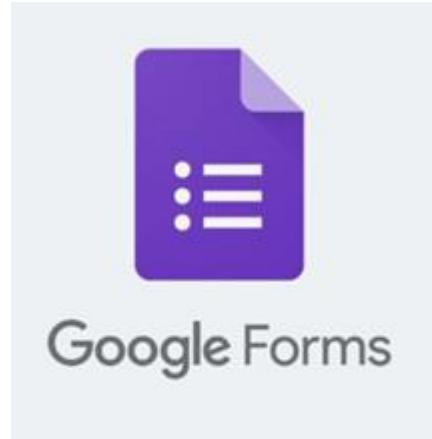
Luca Zulberti

Phone: +39 050 2217 625

Email: luca.zulberti@phd.unipi.it

Students' background and Contacts

Name Surname	Telephone	E-mail	Home Town/Country	Bachelor Degree/ University
Luca Fanucci	347 5013837	luca.fanucci@unipi.it	Montecatini Terme (PT) Italy	Electronic Engineering University of Pisa



https://docs.google.com/forms/d/e/1FAIpQLSePQn8x_IZAg0kAVMi8kk9QQ426UcoT__xCWydjwvuYqFEFKg/viewform?usp=sf_link

Course Schedule

	1M Computer Eng					
	Lu	Ma	Me	Gi	Ve	Sa
8:30/9:30	Performance evaluation of Computer Systems and networks F2					
9:30/10:30	Performance evaluation of Computer Systems and networks F2					
10:30/11:30	Communication Systems F2					
11:30/12:30	Communication Systems F2		Large scale and multist. databases F3		Large scale and multist. databases SI5	
12:30/13:30			Large scale and multist. databases F3		Large scale and multist. databases SI5	
14:00/15:00						
15:00/16:00	Electronics and Communications Systems F2	Large scale and multist. databases SI5	Performance evaluation of Computer Systems and networks SI5	Communication Systems A13	Electronics and Communications Systems SI5	
16:00/17:00	Electronics and Communications Systems F2	Large scale and multist. databases SI5	Performance evaluation of Computer Systems and networks SI5	Communication Systems A13	Electronics and Communications Systems SI5	
17:00/18:00	Electronics and Communications Systems F2	Performance evaluation of Computer Systems and networks SI5	Large scale and multist. databases SI5	Performance evaluation of Computer Systems and networks SI5	Electronics and Communications Systems SI5	
18:00/19:00		Performance evaluation of Computer Systems and networks SI5	Large scale and multist. databases SI5	Performance evaluation of Computer Systems and networks SI5		

Question Time

by appointment:

Tel. 347 5013837

Email: luca.fanucci@unipi.it

Course Goals and Prerequisites

- Goals
 - Provide you with an introduction to the **techniques** and **methodologies** used to produce embedded systems based on Very Large Scale Integration (VLSI) technology
 - **Circuits** and **Architectures** for **basic digital signal processing blocks** to be used for complex system synthesis according to given **performance criteria**: area, speed, power consumption and reliability.
 - Give you some **hands-on experience** with software tools used for Computer Aided Design (CAD)
 - Create a foundation for further exploration of VLSI
 - Basic of **sensor conditioning** electronics and **smart sensors**
- Prerequisites
 - Basic understanding of circuits and electronics
 - Basic understanding of logic design

Course Goals and Prerequisites

- Prerequisites
 - Basic understanding of circuits and electronics
 - Basic understanding of logic design

Prerequisiti-Reti Logiche - Prof. Stea (1/2)

ORGANIZZAZIONE FUNZIONALE DI UN CALCOLATORE: Schema a blocchi.

Tecniche di indirizzamento degli operandi e principali istruzioni dei processori della famiglia INTEL 80x86. Il linguaggio assembler MASM, il Debug ed il Code View per processori della famiglia 80x86

RETI COMBINATORIE: Le porte AND, OR, NOT, NAND e NOR; il decodificatore/demultiplatore; il multiplatore. Le porte a tre strati e le loro applicazioni. Modalità di descrizione, trattazione algebrica e sintesi ottima delle reti combinatorie. I transitori e le alee.

RETI SEQUENZIALI ASINCRONE: Modelli funzionali, modalità di descrizione e modelli implementativi. I flip-flop SR, D latch e D edge-triggered. Le memorie RAM.

Prerequisiti-Reti Logiche - Prof. Stea(2/2)

RETI SEQUENZIALI SINCRONIZZATE: L'elemento di registro; i registri in traslazione e i contatori. Reti sequenziali sincronizzate di Moore, di Mealy e di Mealy Ritardato: modelli funzionali, modalità di descrizione, modelli implementativi. Il flip-flop J-K. Reti sequenziali complesse: descrizione in un linguaggio di trasferimento tra registri, sintesi in accordo al modello strutturale con parte operativa e parte controllo (con particolare riferimento ai modelli microprogrammati).

STRUTTURA FISICA DI UN CALCOLATORE: Moduli di base e loro collegamento. Struttura interna del processore; della memoria e di alcune interfacce (parallele, seriali, di conteggio e per la conversione A/D e D/A). L'ingresso/uscita dati a controllo di programma. Il meccanismo di interruzione ed il controllore di interruzione. Tecniche di interruzione nell'ingresso/uscita dati.

ALGORITMI E RETI DI TIPO ARITMETICO: Richiami sulla rappresentazione dei numeri naturali, interi e reali; gli algoritmi e le reti fondamentali per una aritmetica dei numeri naturali e dei numeri interi.

Prerequisiti-Elettronica Digitale-Prof. Piotto

PORTE LOGICHE IN TECNOLOGIA CMOS: Inverter CMOS, parametri caratteristici dei circuiti digitali, calcolo dell'energia dissipata durante la commutazione, fan-in, fan-out, sintesi delle porte logiche tramite il metodo della pull-up/pull-down network, protezione ingressi da scariche elettrostatiche, logica a pass transistor, body effect.

LOGICA SEQUENZIALE: Latch realizzato con inverter, flip-flop S/R in tecnologia CMOS, flip-flop D e D edge triggered, il circuito integrato NE555 e le sue applicazioni.

MEMORIE A SEMICONDUTTORE: Struttura a matrice delle memorie, ROM a diodi, ROM e PROM a MOS, memoria SRAM e DRAM, principio di funzionamento del decoder degli indirizzi (wired NOR), memorie EPROM e EEPROM.

GENERATORI DI CLOCK: Generatore di onda quadra, oscillatore quarzato di Pierce.

Course Main Topics

Course Main Topics

Course Main Topics (1/2)

- **Fundamental Design metrics** in digital integrated circuits design. Design space exploration, in terms of area, speed, power consumption, reliability and flexibility addressing the exponential growth in complexity and performance (Moore's law).
- **Design methodologies for full-custom and semi-custom digital integrated circuits** including Field Programmable Gate Arrays (FPGA), Gate Arrays and Standard-Cells. High-level electronic design automation (EDA) tools for hardware-software co-design. Hardware description languages (SystemC, VHDL and Verilog) modeling, simulation and logic synthesis.

Course Main Topics (2/2)

- **CMOS device and interconnect modeling**, static and dynamic logic families, latch and flop design, ALU and MAC design, power supply and clock distribution, signal integrity, and I/O design.
- **Power Consumption in CMOS digital integrated circuits**. Design techniques for the reduction of power consumption at different level of abstractions: logic design, clock gating, multi-VDD, multi-VT, dynamic frequency scaling, dynamic voltage scaling, dynamic thermal management.
- **Sensors** definition, classification and characterization, with focus on **inertial MEMS sensors**, **vital parameter sensors**, etc.. Sensor compensation and calibration techniques. Sensor readout electronics and sensor data fusion.

Course Material (1/2)

< Tutti i team

EA

598II 22/23 - ELECTRONICS AND... ...

Pagina iniziale

Blocco appunti per la classe

Attività

Voti

Reflect

Insights

Canali

Generale

Communications systems

Electronics systems

 Electronics systems Post File Note +

+ Nuovo Carica Modifica nella visualizzazione a griglia Condividi

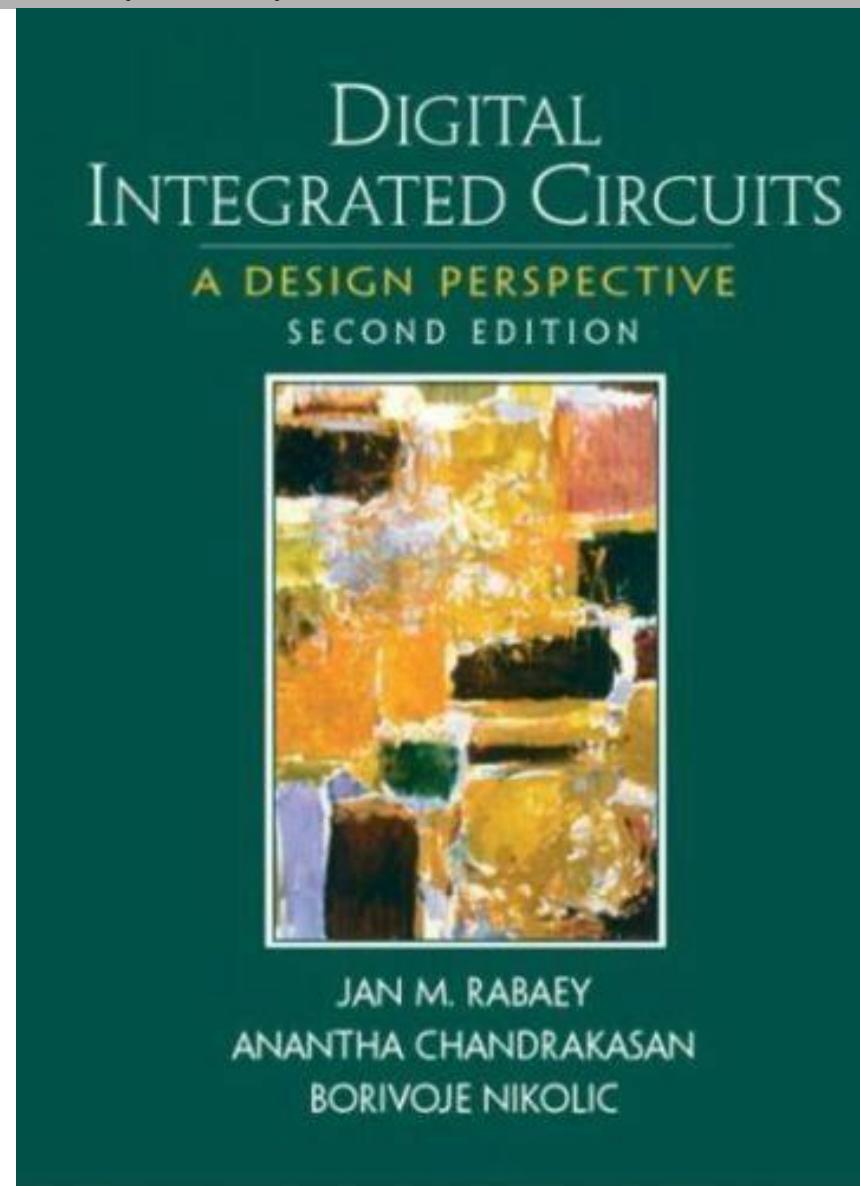
Electronics systems

Nome	Data/ora modifica	Modificato da
Lecture Slides	Circa un'ora fa	Luca Fanucci
VHDL and Hands-on Exercises	Circa un'ora fa	Luca Zulberti

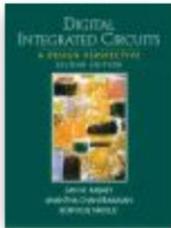
Course Material (1/2)

- CMOS Design Bibliographic References:
 - Weste and Eshraghian, "Principles of VLSI Design - A Systems Perspective (2nd ed)", Addison Wesley
 - M. Smith, "Application Specific Integrated Circuits", Addison-Wesley, 1997
 - J. M. Rabaey, "Digital Integrated Circuits - A Design Perspective", Prentice Hall

<http://icbook.eecs.berkeley.edu/overview>



Course Material (1/2)



LIBRO

Digital integrated circuits : a design perspective / Jan M. **Rabaey**, Anantha Chandrakasan, Borivoje Nikolic

Nikolic, Borivoje ; Chandrakasan, Anantha P ; **Rabaey**, Jan M

Upper Saddle River, NJ Pearson education international : Prentice Hall ; 2003

Disponibile. Controlla "Dove lo trovo?" >

DOVE LO TROVO

DETTAGLI

INVIA A

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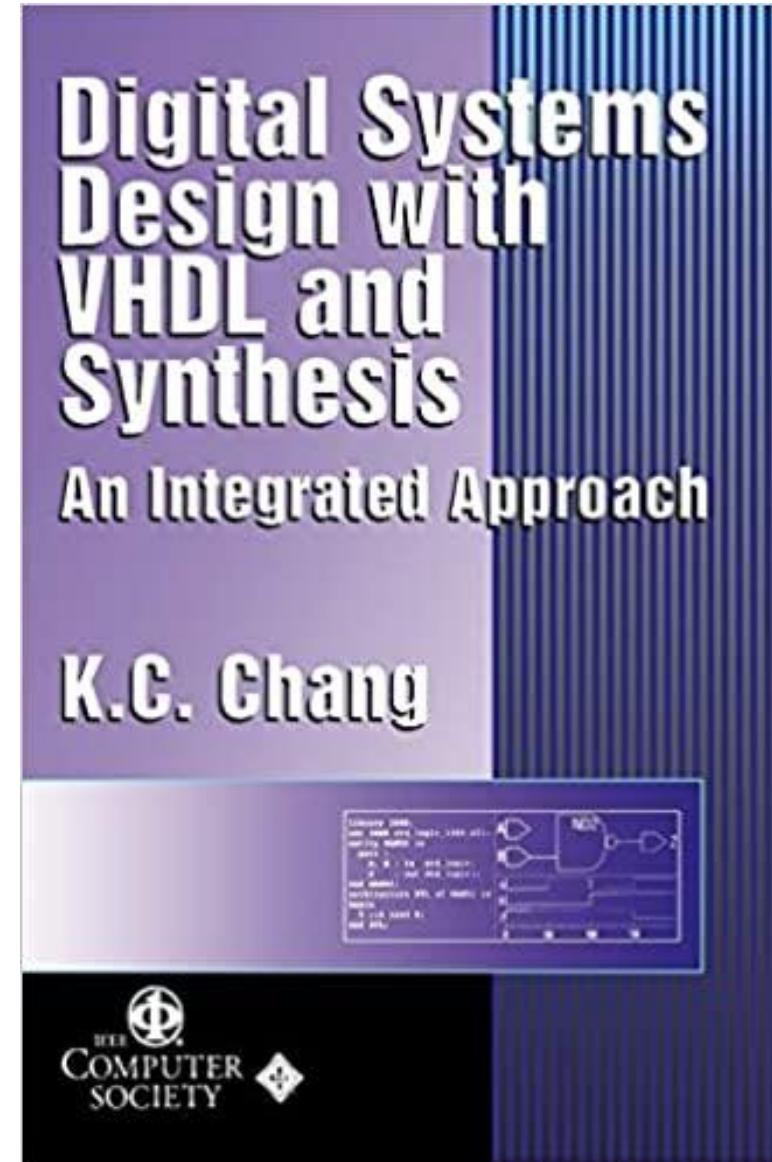
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(1 copia, 1 disponibile, 0 richieste)

Course Material (2/2)

■ VHDL Bibliographic References:

- IEEE Standard VHDL Language Reference Manual : IEEE Std 1076-1993
- S. Mazor, P. Langstraat, "A guide to VHDL", Kluwer Academic Publishers
- Douglas L. Perry, "VHDL" (2nd edition), McGraw Hill
- B. Cohen, "VHDL Coding Styles and Methodologies", Kluwer Academic Publishers
- K.C. Chang, "*Digital Systems Design with VHDL and Synthesis*", IEEE Computer Society
- W.F. Lee, "VHDL: Coding and Logic Synthesis with SynopsysTM", Academic Press

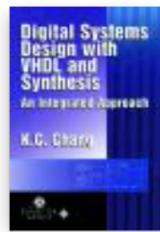


Course Material (2/2)

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Digital systems design with **VHDL** and synthesis : an integrated approach / K.C. Chang

Chang, Kou Chuan 1957-

Los Alamitos Ca : IEEE computer society ; 1999

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OPZIONI: Bisogno di aiuto? / Orari delle Biblioteche

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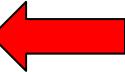
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Course Material (2/2)

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 - IEEE Standard VHDL Language Reference Manual : IEEE Std 1076-1993
 - S. Mazor, P. Langstraat, "A guide to VHDL", Kluwer Academic Publishers
 - Douglas L. Perry, "VHDL" (2nd edition), McGraw Hill
 - B. Cohen, "VHDL Coding Styles and Methodologies", Kluwer Academic Publishers
 - K.C. Chang, "*Digital Systems Design with VHDL and Synthesis*", IEEE Computer Society
 - W.F. Lee, "VHDL: Coding and Logic Synthesis with Synopsys™", Academic Press
- PC-based VHDL simulation tools:
 - Aldec (<http://www.aldec.com>): Active HDL
 - https://www.aldec.com/en/products/fpga_simulation/active_hdl_student
 - ~~Mentor Siemens (<https://eda.sw.siemens.com/en-US/ic/modelsim/>)~~: ModelSim
 - ~~Intel-Altera (<https://www.intel.it/content/www/it/it/software/programmable/quartus-prime/model-sim.html>)~~ ModelSim 
 - <http://ghdl.free.fr/> (+ <http://gtkwave.sourceforge.net/>)
- Xilinx Development tool:
 - <http://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html> 

OVERVIEW

ModelSim

ModelSim simulates behavioral, RTL, and gate-level code - delivering increased design quality and debug productivity with platform-independent compile. Single Kernel Simulator technology enables transparent mixing of VHDL and Verilog in one design.

[Watch webinar](#)

[View fact sheet](#)

 Get in touch with our sales team 1-800-547-3000



<https://eda.sw.siemens.com/en-US/ic/modelsim/>

Student edition Currently **not available**

VHDL Simulation (2/3)

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ModelSim*-Intel® FPGA Edition Software

[Benefits](#)[FAQ](#)[Support](#)

What's New

Starting with Intel® Quartus® Prime version 21.3, the ModelSim*-Intel® FPGA edition software has been discontinued and replaced by the [Questa*-Intel® FPGA Edition software](#). Refer to this [customer advisory](#) for details.

Watch this [video](#) to find out how easy it is to migrate to Questa*-Intel FPGA Edition.

Also, review the [Quick Start Guide](#) for instructions on how to get started.

The ModelSim*-Intel® FPGA edition software is a version of the ModelSim* software targeted for Intel® FPGAs devices. The software supports Intel gate-level libraries and includes behavioral simulation, HDL testbenches, and Tcl scripting.

[Download ModelSim*-Intel® FPGA edition software →](#)

<https://www.intel.it/content/www/it/it/software/programmable/quartus-prime/model-sim.html>

Free Edition Available

VHDL Simulation (3/3)

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Active-HDL™ | Student Edition

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Free Active-HDL Student Edition

Active-HDL Student Edition is a mixed language design entry and simulation tool offered at no cost by Aldec for students to use during their course work.

Licensing

Active-HDL Student Edition includes a "load and go" license. This means students can begin using it immediately after installing.

Key Features of Active-HDL Student Edition

- Mixed language simulator
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- Graphical Design entry & editing
- Code2Graphics and Graphics2Code
- Pre-compiled FPGA vendor libraries
- IEEE Language Support: VHDL, Verilog, SystemVerilog(Design), SystemC
- Waveform Viewer and List Viewer
- Interface with MATLAB®/Simulink®
- HTML and PDF Design Documentation

- https://www.aldec.com/en/products/fpga_simulation/active_hdl_student
- Low Cost Alternative Solution

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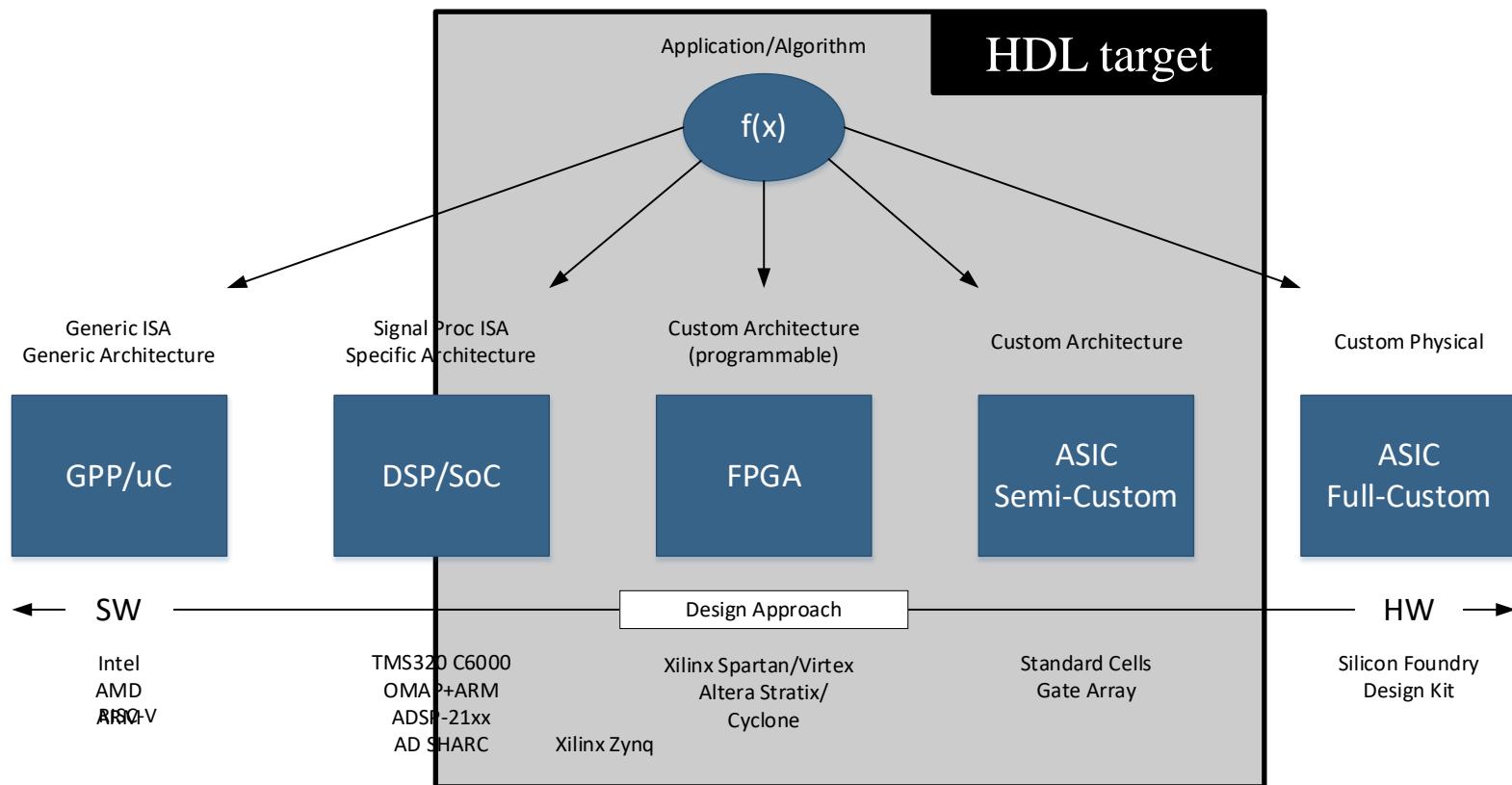
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VHDL Logic synthesis and FPGA Programming

<http://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html>

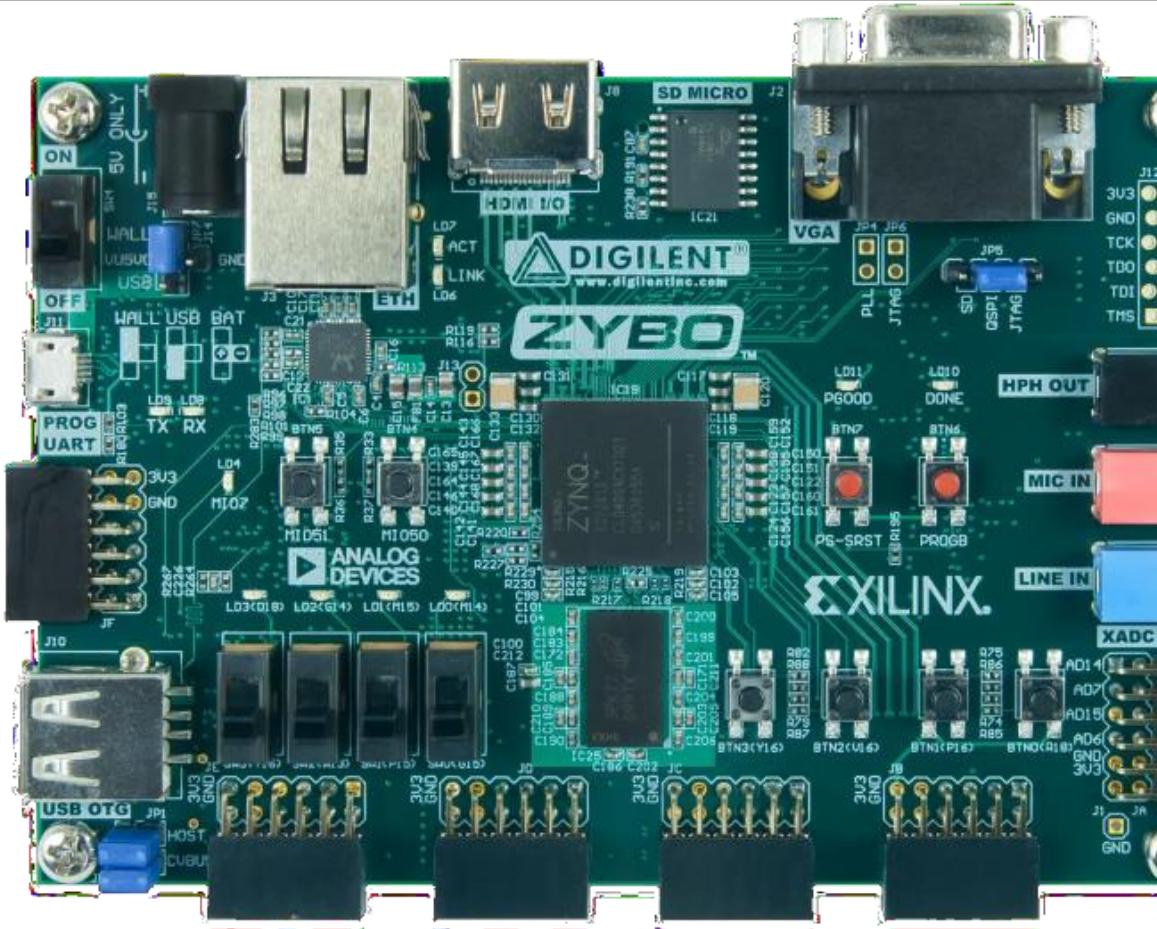
Digital Design Technology Map:

From a $f(x)$ to *Hardware Acceleration*



Hands-on:

VHDL modelling, logic synthesis and FPGA Programming



During the Lab we will design from scratch a complete digital system, from requirements to the implementation on a FPGA Board and its test.

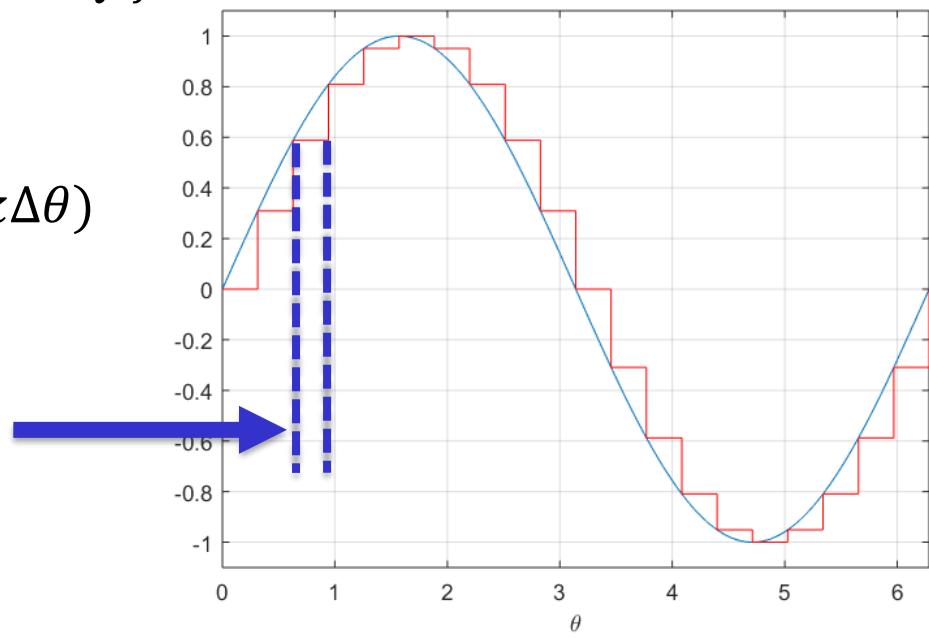
Hands-on: DDFS System Description

The DDFS (Direct Digital Frequency Synthesizer) is a digital system able to generate a quantized *sin* waveform, with frequency control.

Building block of many Telecommunication systems

Suppose we want to generate a single tone at frequency f :

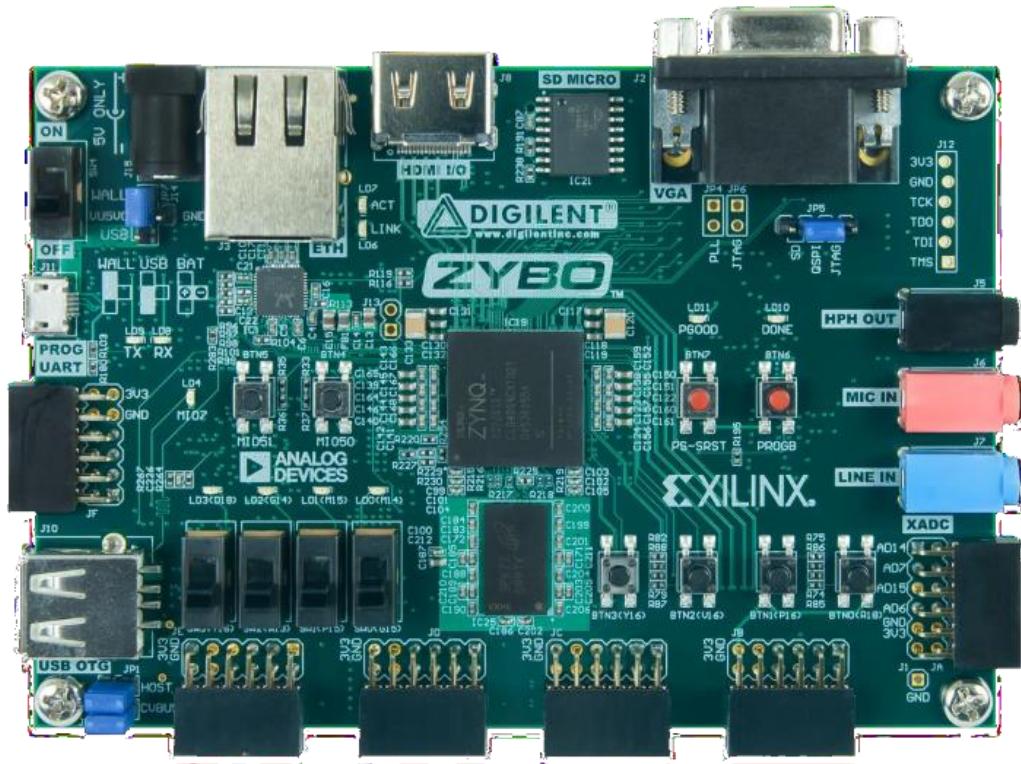
- Ideal output: $\sin(2\pi ft) = \sin(\theta)$
- Discrete time: $\sin(2\pi fkT_{ck}) = \sin(k\Delta\theta)$
- Phase resolution: $\Delta\theta = 2\pi \frac{f}{f_{ck}}$
 - Depends on f
 - Depends on f_{ck}



ZyBo Development Board (1/3)

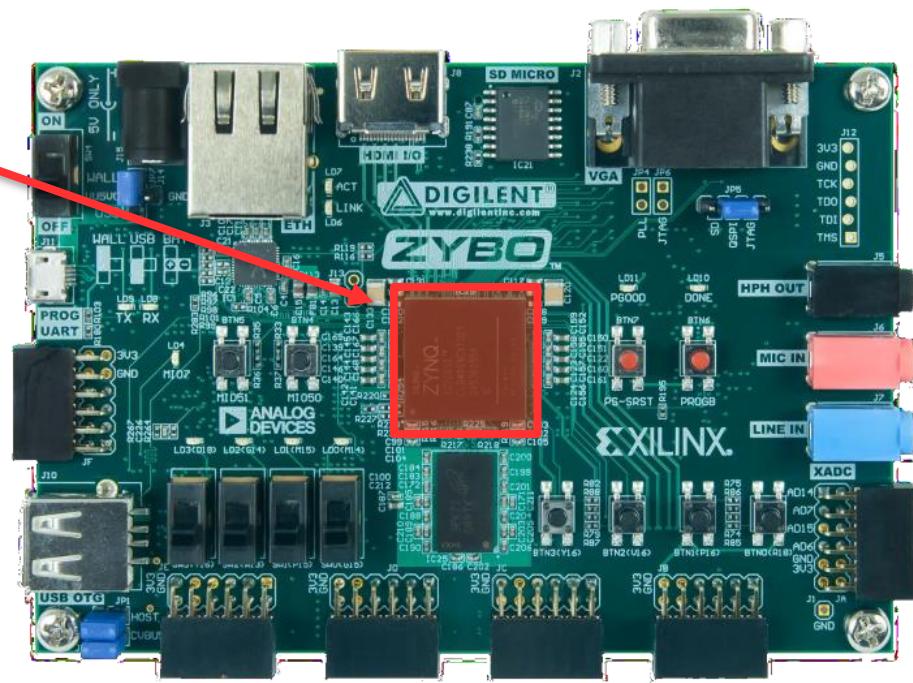
The ZYBO (**Z**Ynq **B**Oard) is a feature-rich, ready-to-use, entry-level embedded software and digital circuit development platform built around the smallest member of the Xilinx Zynq-7000 family, the Z-7010.

The Z-7010 is based on the Xilinx All Programmable System-on-Chip (AP SoC) architecture, which tightly integrates a dual-core ARM Cortex-A9 processor with Xilinx 7-series Field Programmable Gate Array (FPGA) logic.



ZyBo Development Board (2/3)

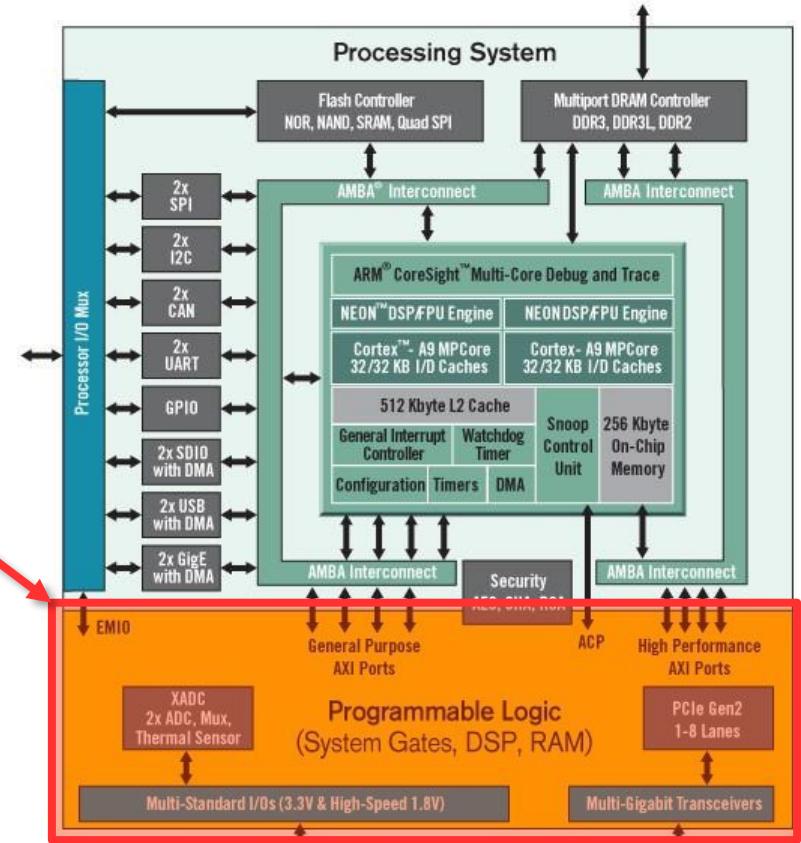
- **ZYNQ XC7Z010-1CLG400C**
- 512MB x32 DDR3 w/ 1050Mbps bandwidth
- Dual-role (Source/Sink) HDMI port
- 16-bits per pixel VGA source port
- Trimode (1Gbit/100Mbit/10Mbit) Ethernet PHY
- MicroSD slot (supports Linux file system)
- OTG USB 2.0 PHY (supports host and device)
- External EEPROM (programmed with 48-bit globally unique EUI-48/64™ compatible identifier)
- Audio codec with headphone out, microphone and line in jacks
- 128Mb Serial Flash w/ QSPI interface
- On-board JTAG programming and UART to USB converter
- GPIO: 6 pushbuttons, 4 slide switches, 5 LEDs
- Six Pmod connectors (1 processor-dedicated, 1 dual analog/digital, 3 high-speed differential, 1 logic-dedicated)



ZyBo Development Board (3/3)

ZYNQ XC7Z010-1CLG400C

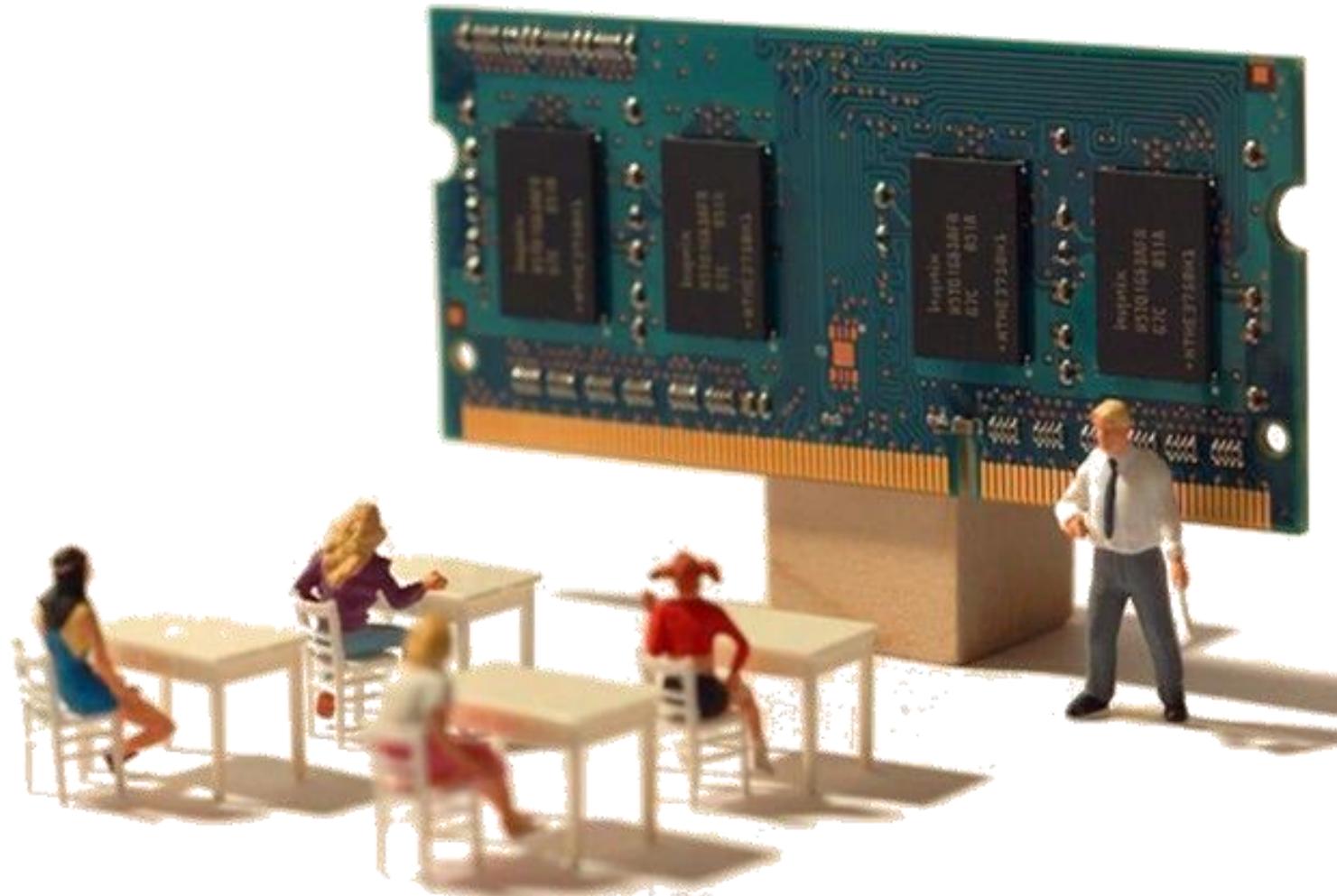
- 650Mhz dual-core Cortex-A9 processor
- DDR3 memory controller with 8 DMA channels
- High-bandwidth peripheral controllers: 1G Ethernet, USB 2.0, SDIO
- Low-bandwidth peripheral controller: SPI, UART, CAN, I2C
- **Reprogrammable logic equivalent to Artix-7 FPGA**
 - 4,400 logic slices, each with four 6-input LUTs and 8 flip-flops
 - 240 KB of fast block RAM
 - Two clock management tiles, each with a phase-locked loop (PLL) and mixed-mode clock manager (MMCM)
 - 80 DSP slices
 - Internal clock speeds exceeding 450MHz
 - On-chip analog-to-digital converter (XADC)



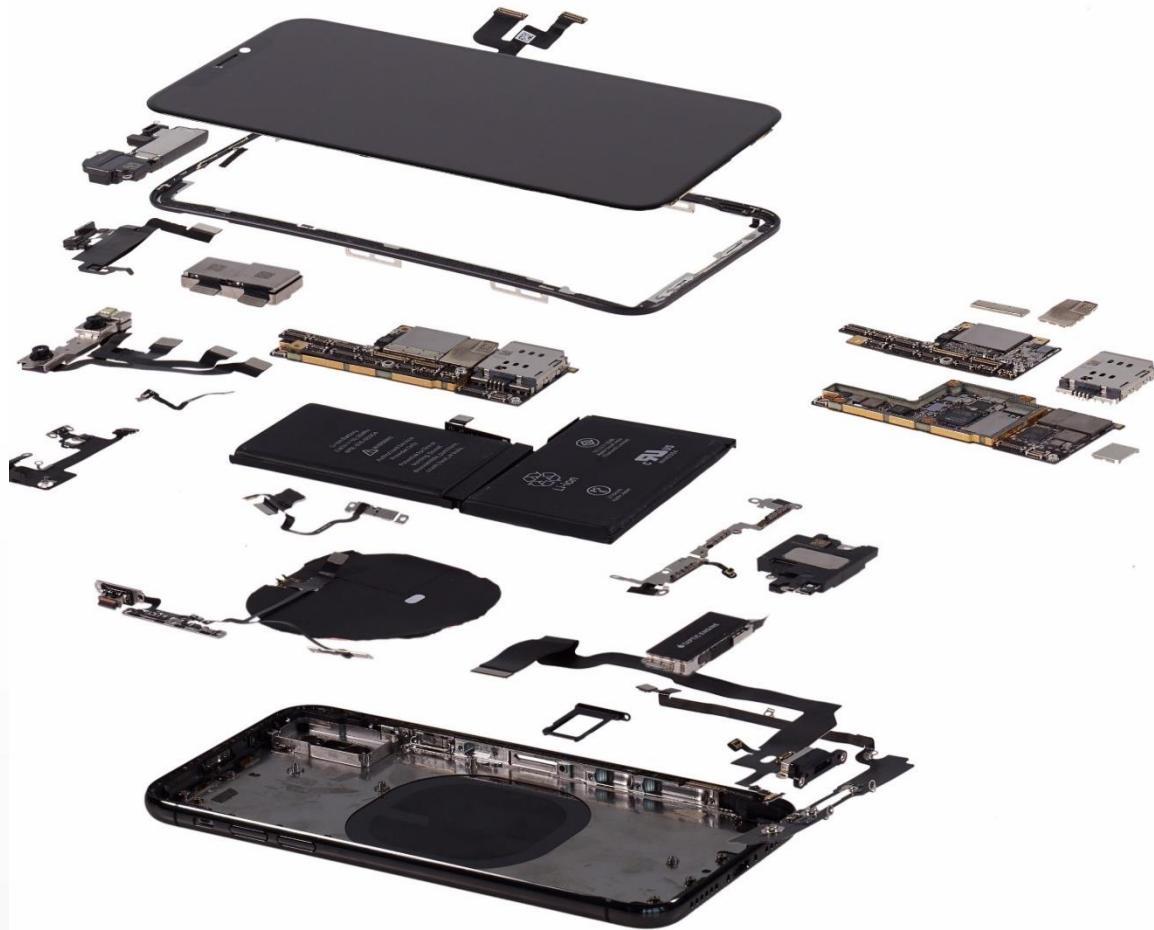
Exam

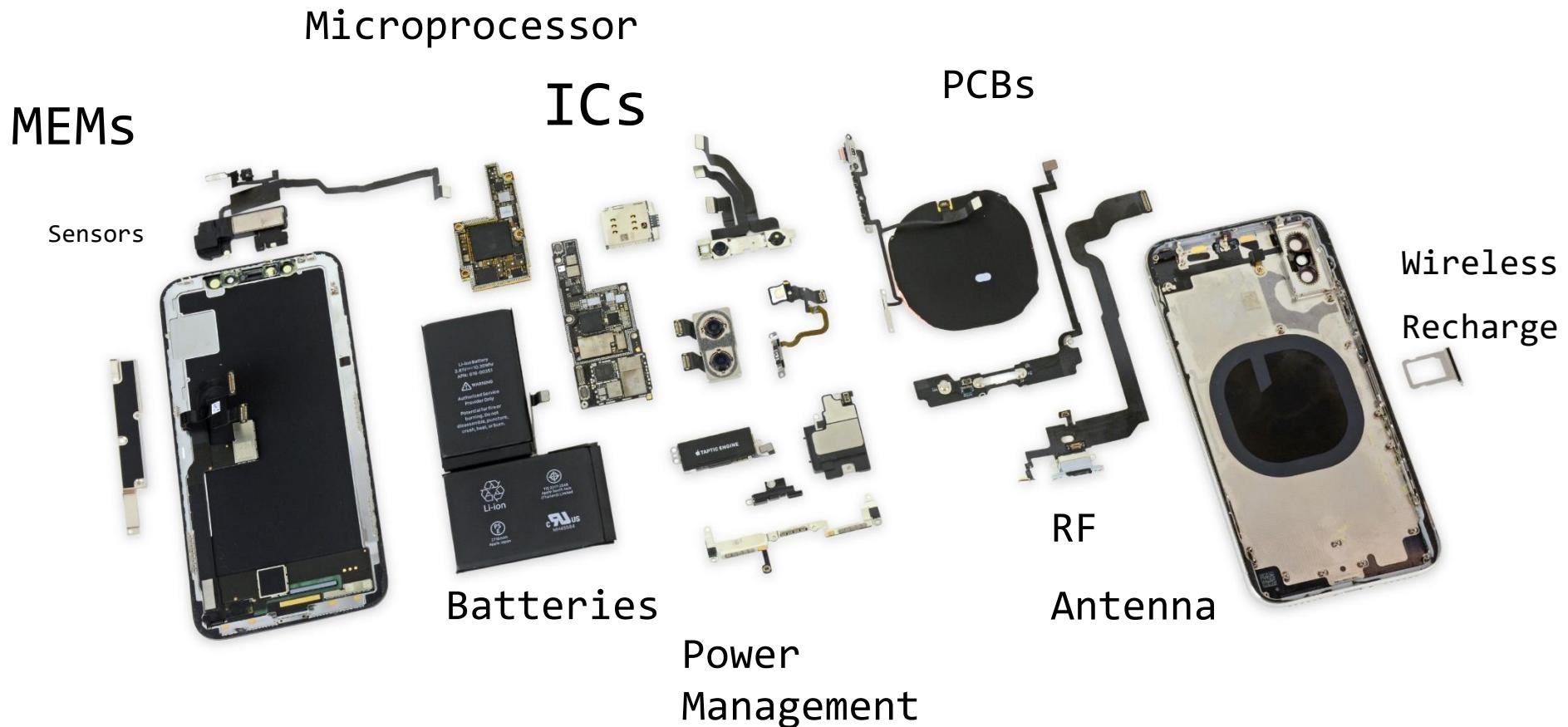
- Oral test on topics covered in the course
- Digital Design (VHDL and automatic logic synthesis for FPGA technology) -- (**optional BUT recommended**)
 - Realization of digital electronic system of similar complexity as seen during class hands-on exercises
 - 1 - 2 people
 - Request for project assignment via email
 - Email delivery of source code and testbench together with the technical report
 - Design Review/Discussion before the oral exam

Questions ?



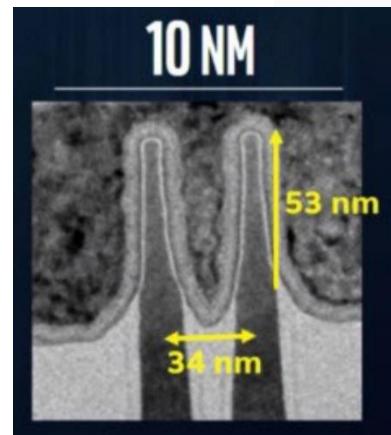
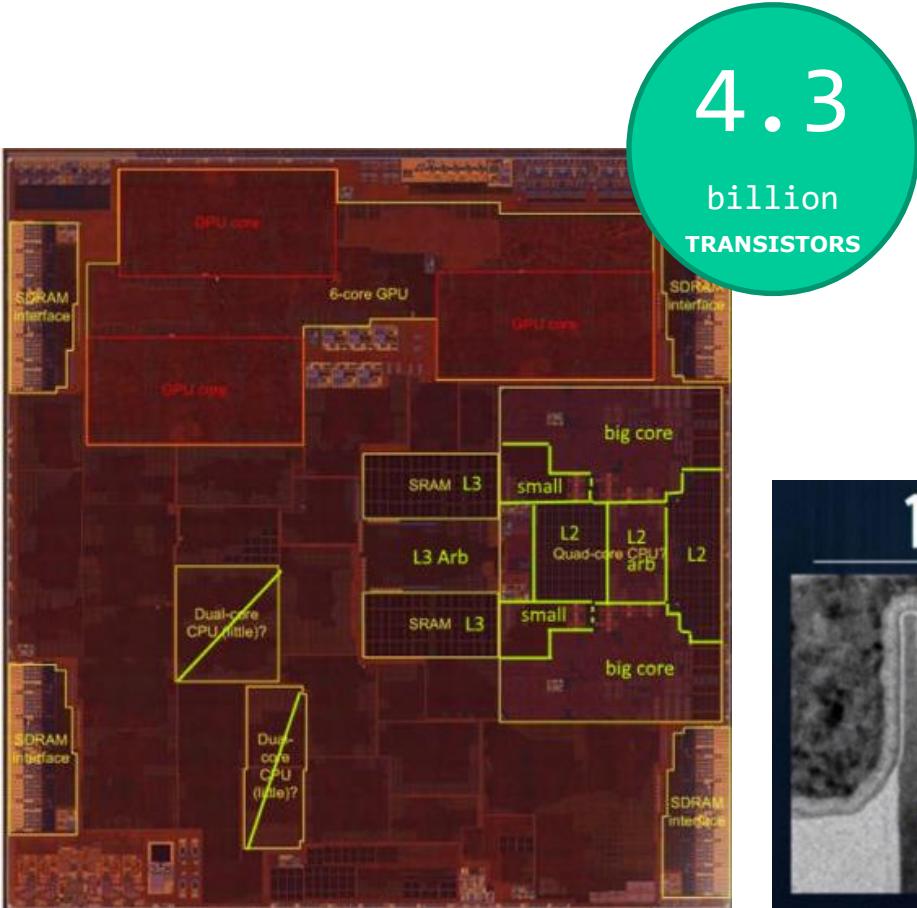
Let's start !!





MULTIDISCIPLINARITY

MicroProcessor

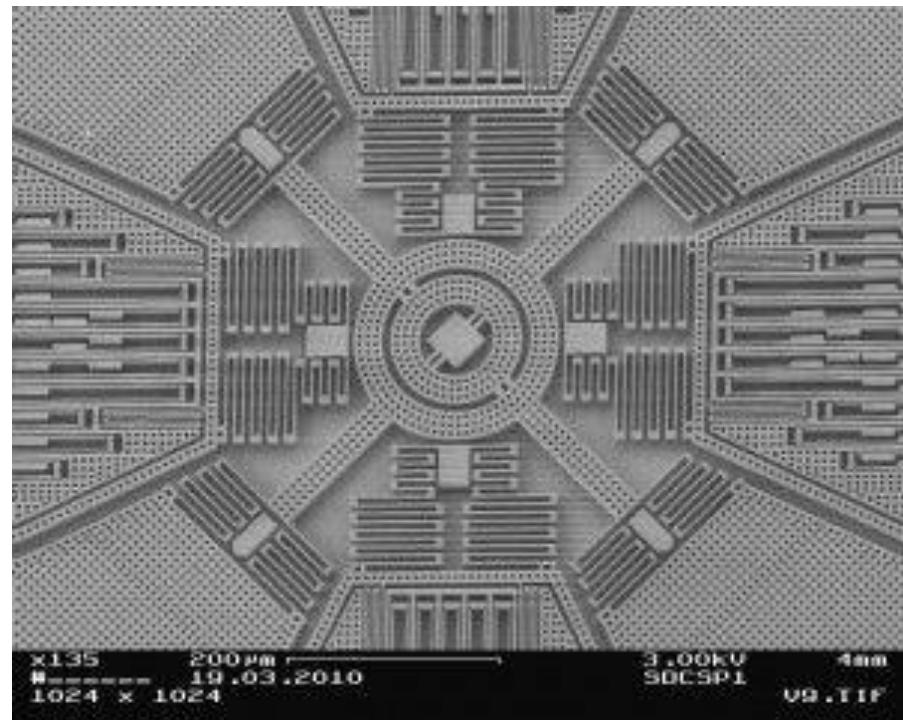


Sensors



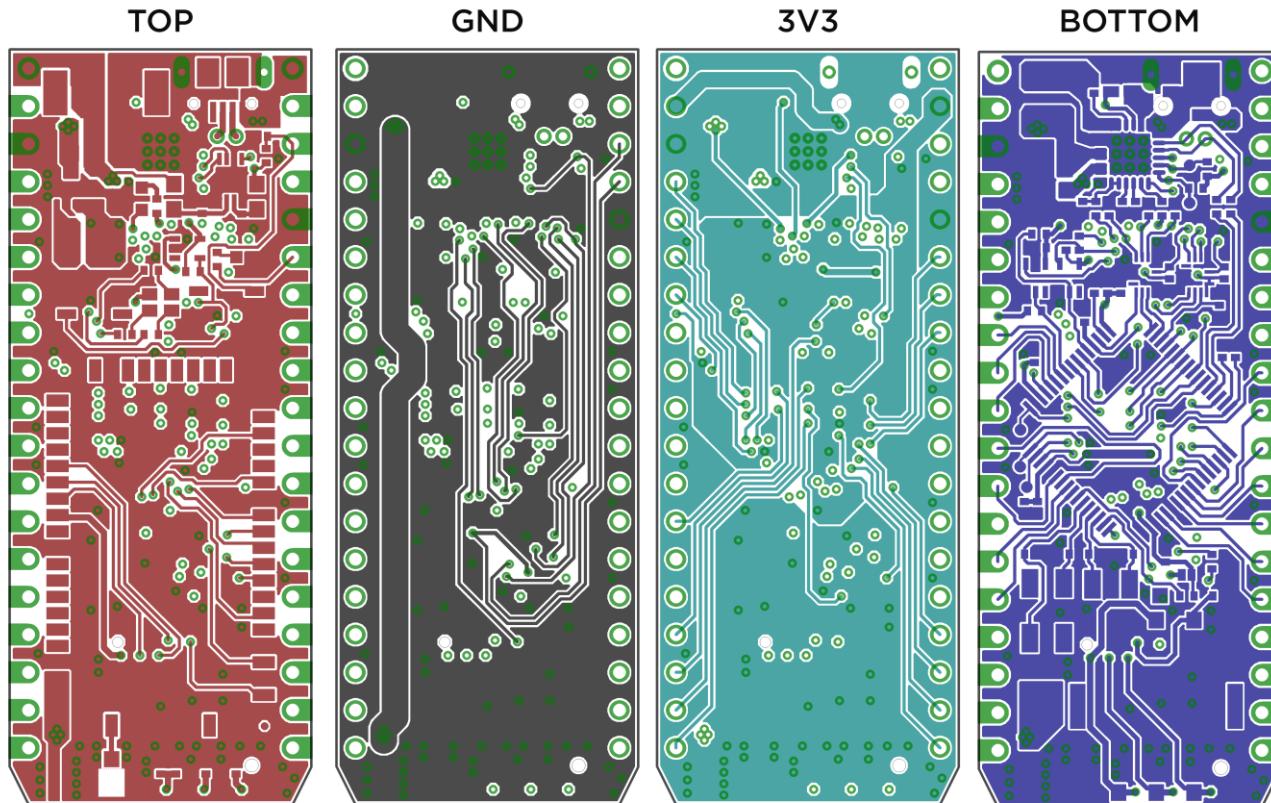
MEMs

Micro-Electro-Mechanical systems



PCB

Printed Circuit Boards



Batteries



Antenna



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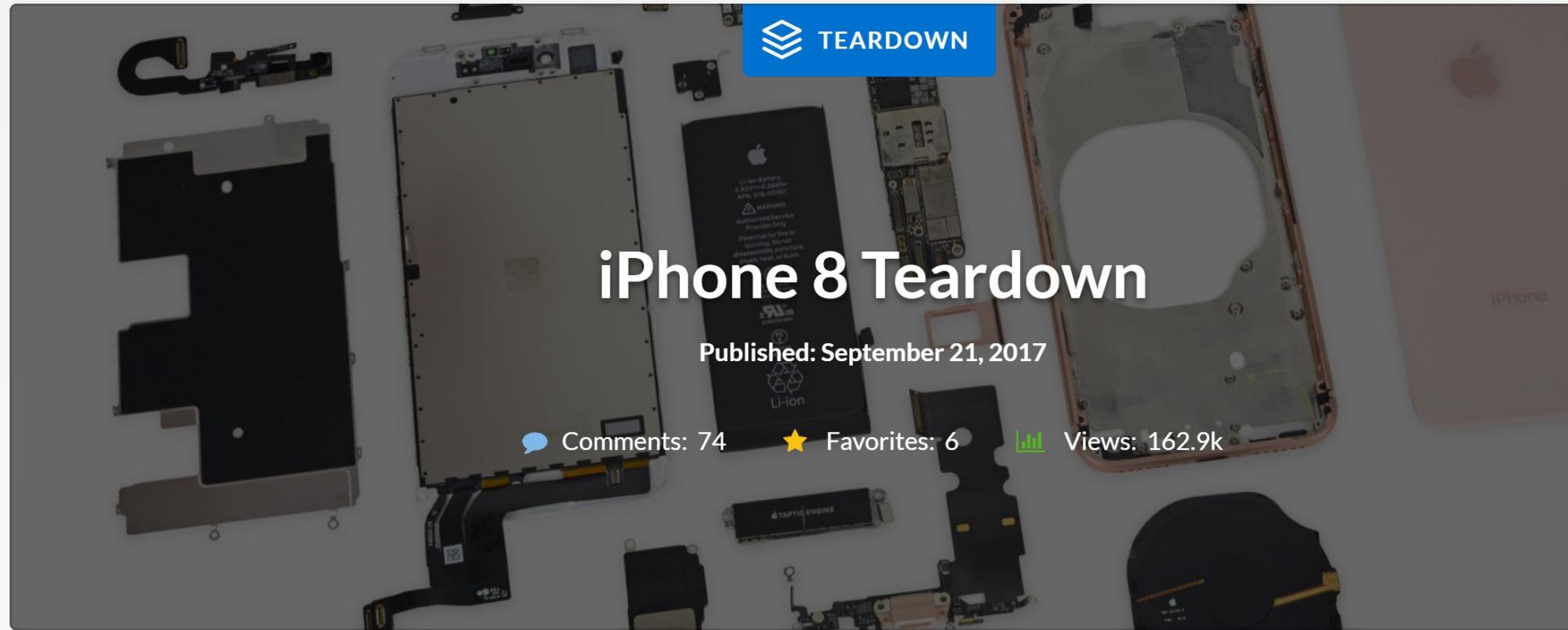
iPhone 8 Teardown

Published: September 21, 2017

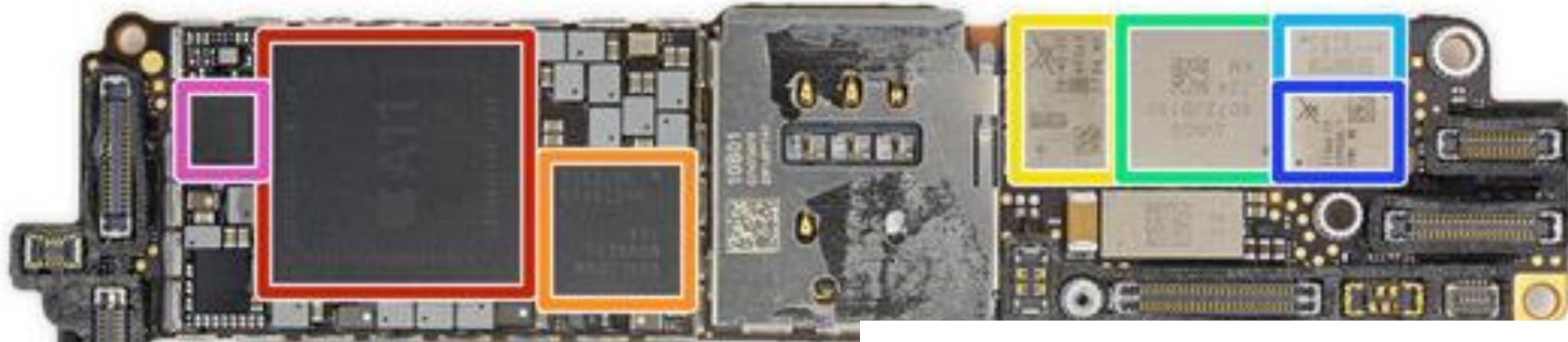
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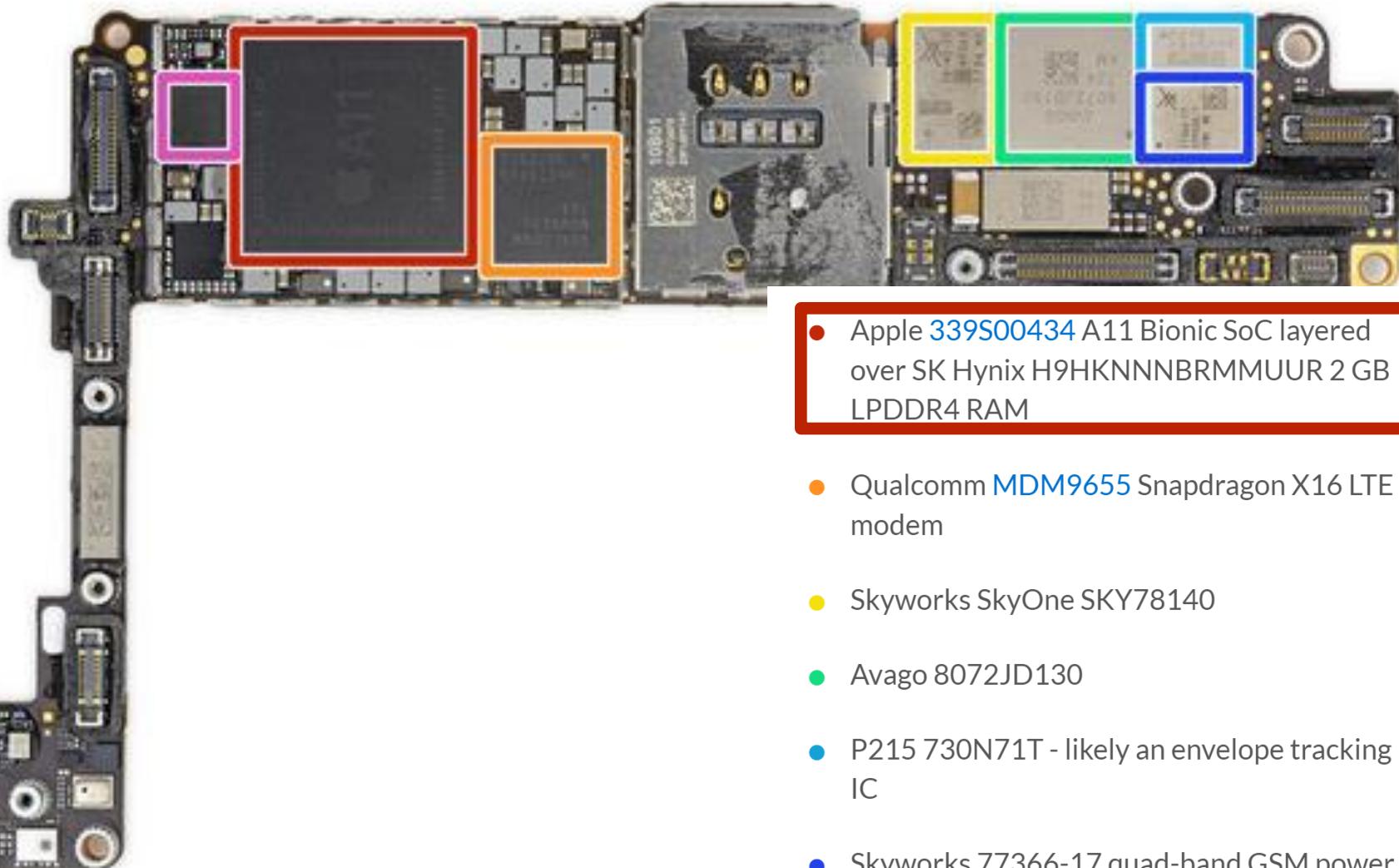
 Views: 162.9k



<https://www.ifixit.com/Teardown/iPhone+8+Teardown/97481>



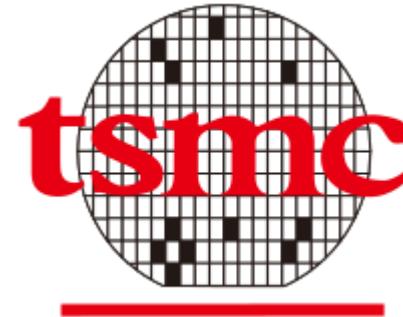
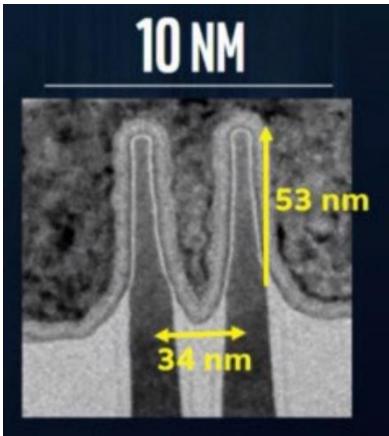
- Apple [339S00434](#) A11 Bionic SoC layered over SK Hynix H9HKNNNBRMMUUR 2 GB LPDDR4 RAM
- Qualcomm [MDM9655](#) Snapdragon X16 LTE modem
- Skyworks SkyOne SKY78140
- Avago 8072JD130
- P215 730N71T - likely an envelope tracking IC
- Skyworks 77366-17 quad-band GSM power amplifier module
- NXP [80V18](#) secure NFC module



- Apple [339S00434](#) A11 Bionic SoC layered over SK Hynix H9HKNNNBRMMUUR 2 GB LPDDR4 RAM
- Qualcomm [MDM9655](#) Snapdragon X16 LTE modem
- Skyworks SkyOne SKY78140
- Avago 8072JD130
- P215 730N71T - likely an envelope tracking IC
- Skyworks 77366-17 quad-band GSM power amplifier module
- NXP [80V18](#) secure NFC module

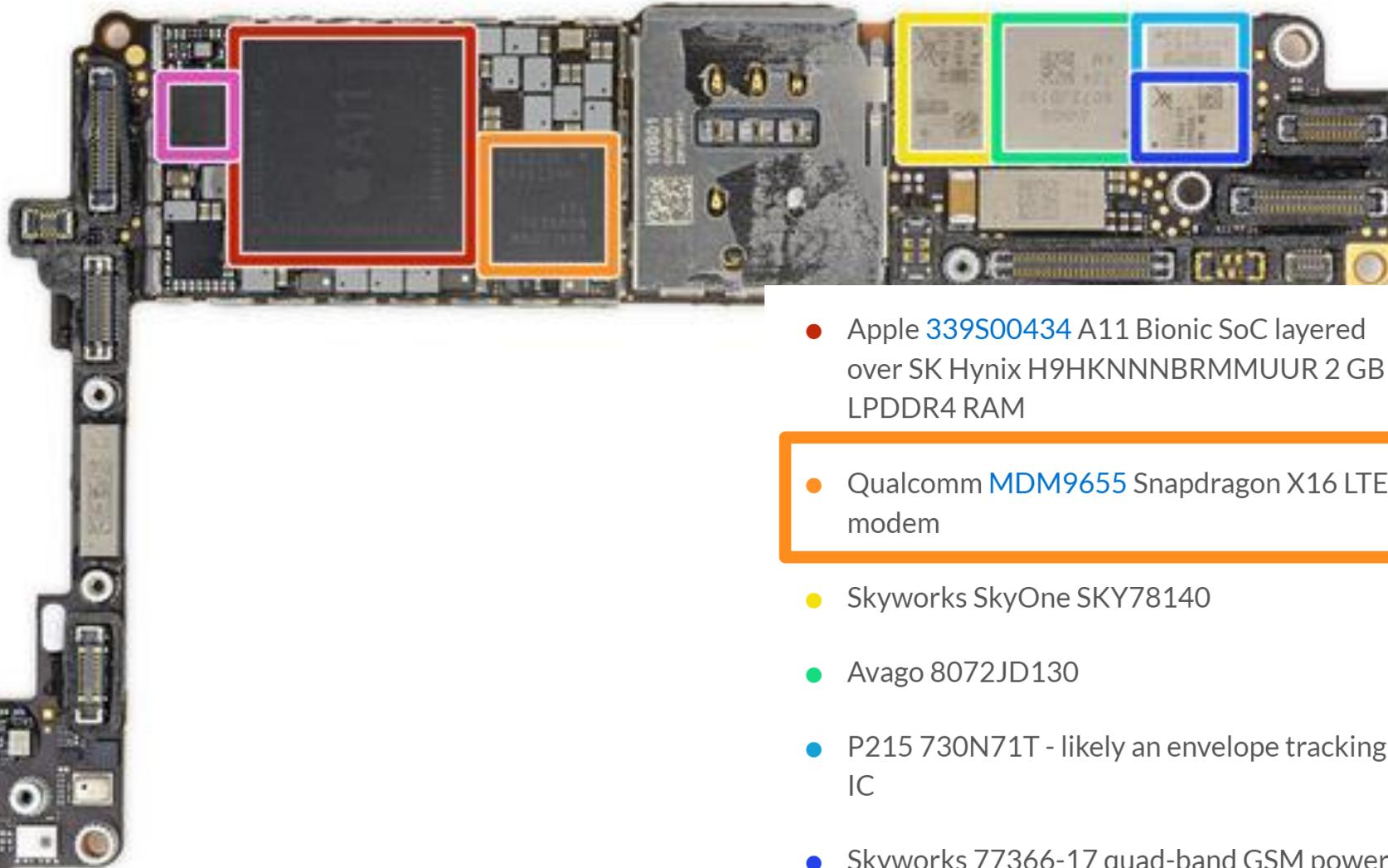


4.3
billion
TRANSISTORS



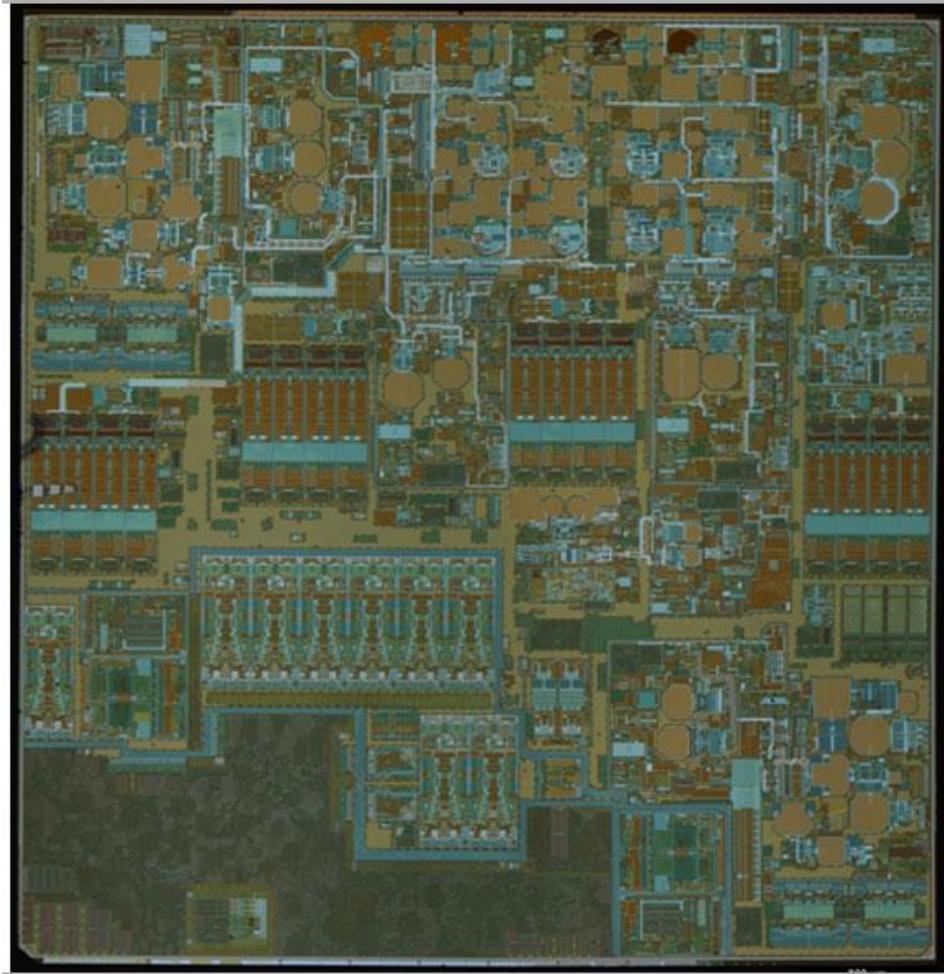
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iPhone 8



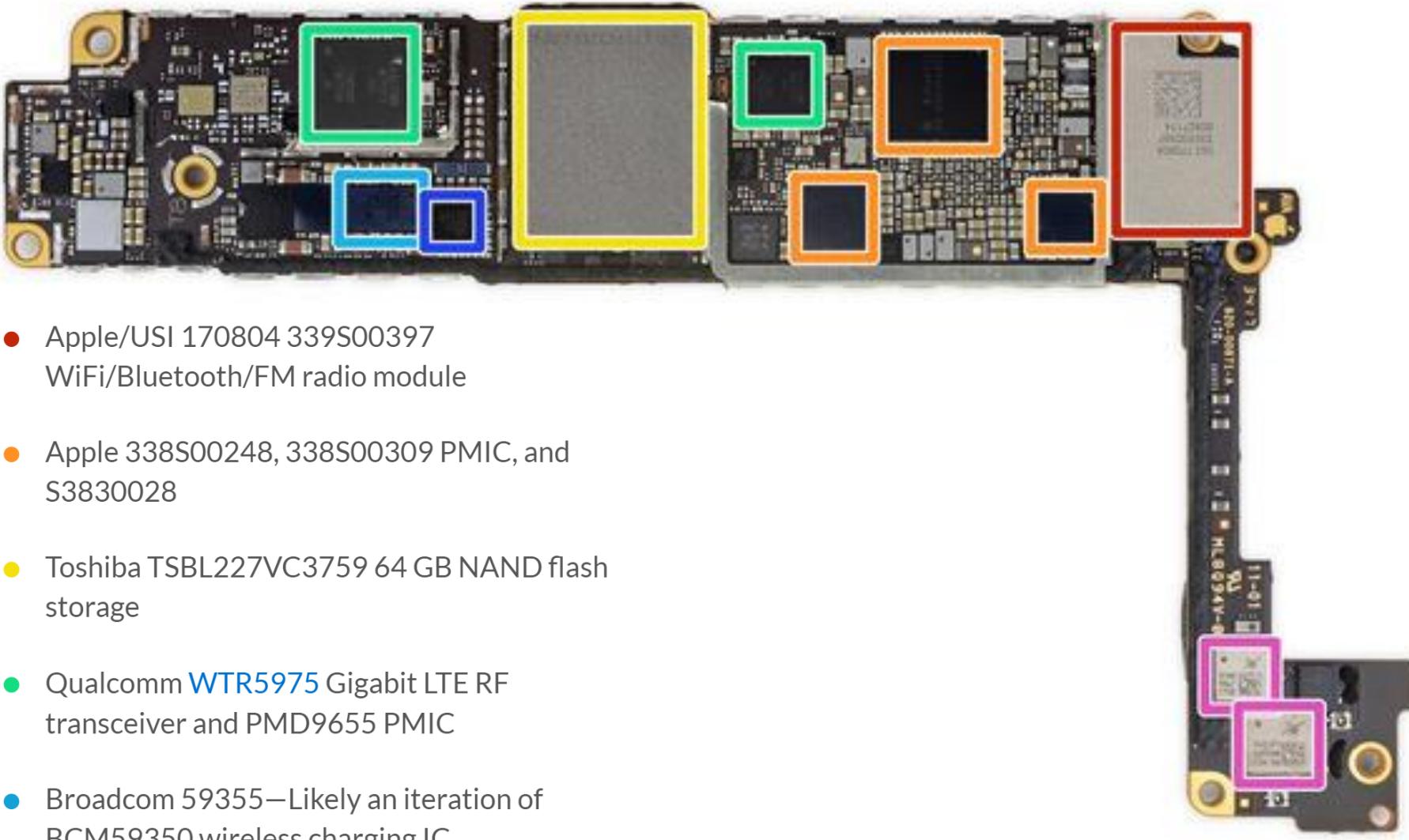
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<https://www.qualcomm.com/products/snapdragon-modems-4g-lte-x16>



- Apple [339S00434](#) A11 Bionic SoC layered over SK Hynix H9HKNNNBRMMUUR 2 GB LPDDR4 RAM
 - Qualcomm [MDM9655](#) Snapdragon X16 LTE modem
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 - Skyworks 77366-17 quad-band GSM power amplifier module
 - NXP [80V18](#) secure NFC module

iPhone 8



- Apple/USI 170804 339S00397 WiFi/Bluetooth/FM radio module
- Apple 338S00248, 338S00309 PMIC, and S3830028
- Toshiba TSBL227VC3759 64 GB NAND flash storage
- Qualcomm [WTR5975](#) Gigabit LTE RF transceiver and PMD9655 PMIC
- Broadcom 59355—Likely an iteration of BCM59350 wireless charging IC
- NXP 1612A1—Likely an iteration of the 1610 tristar IC
- Skyworks 3760 3576 1732 RF Switch and SKY762-21 247296 1734 RF Switch

Apple iPhone 8+ (A1864)
Preliminary Cost Summary

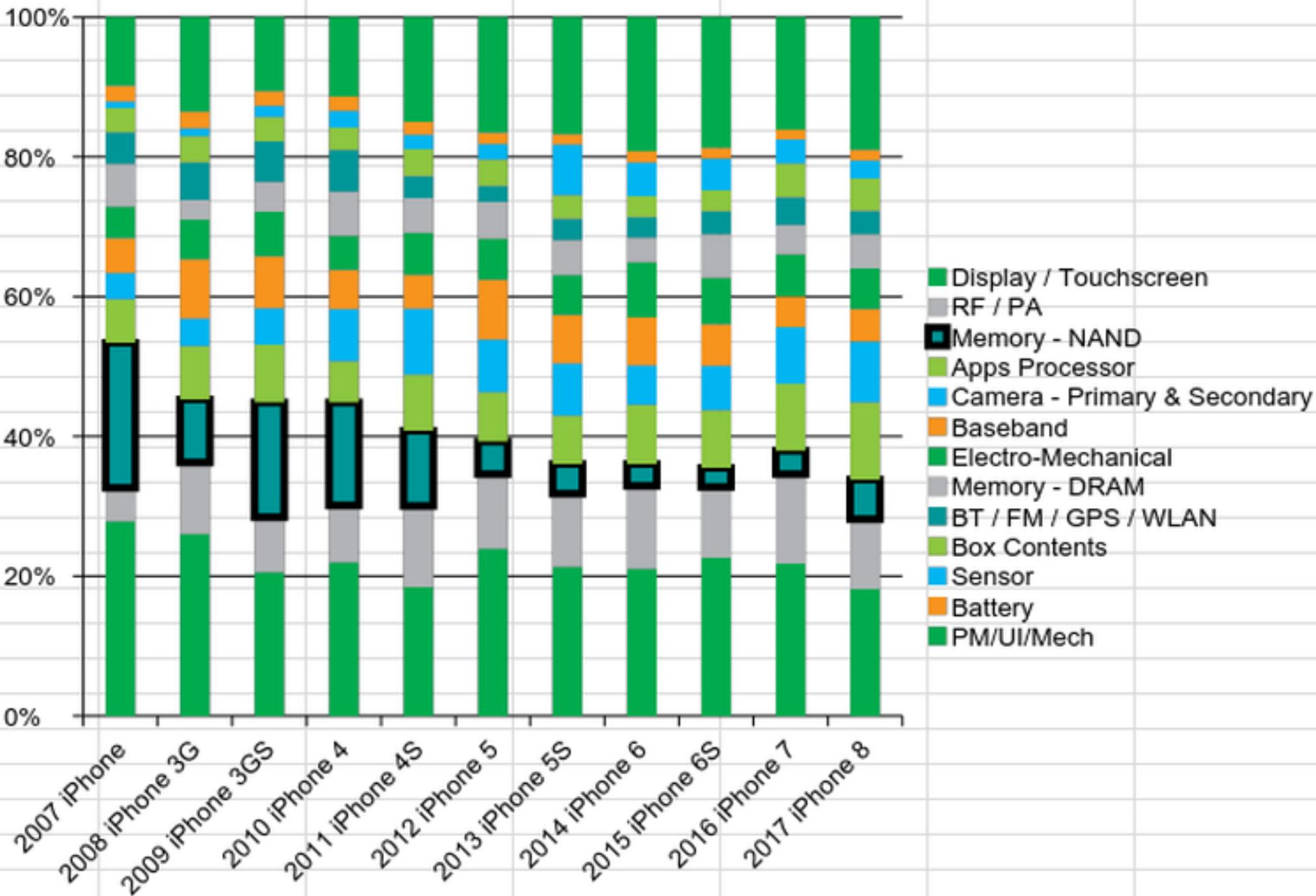
Total Cost Estimate 8+	\$288.08
<i>Cost Of Manufacturing</i>	\$7.36

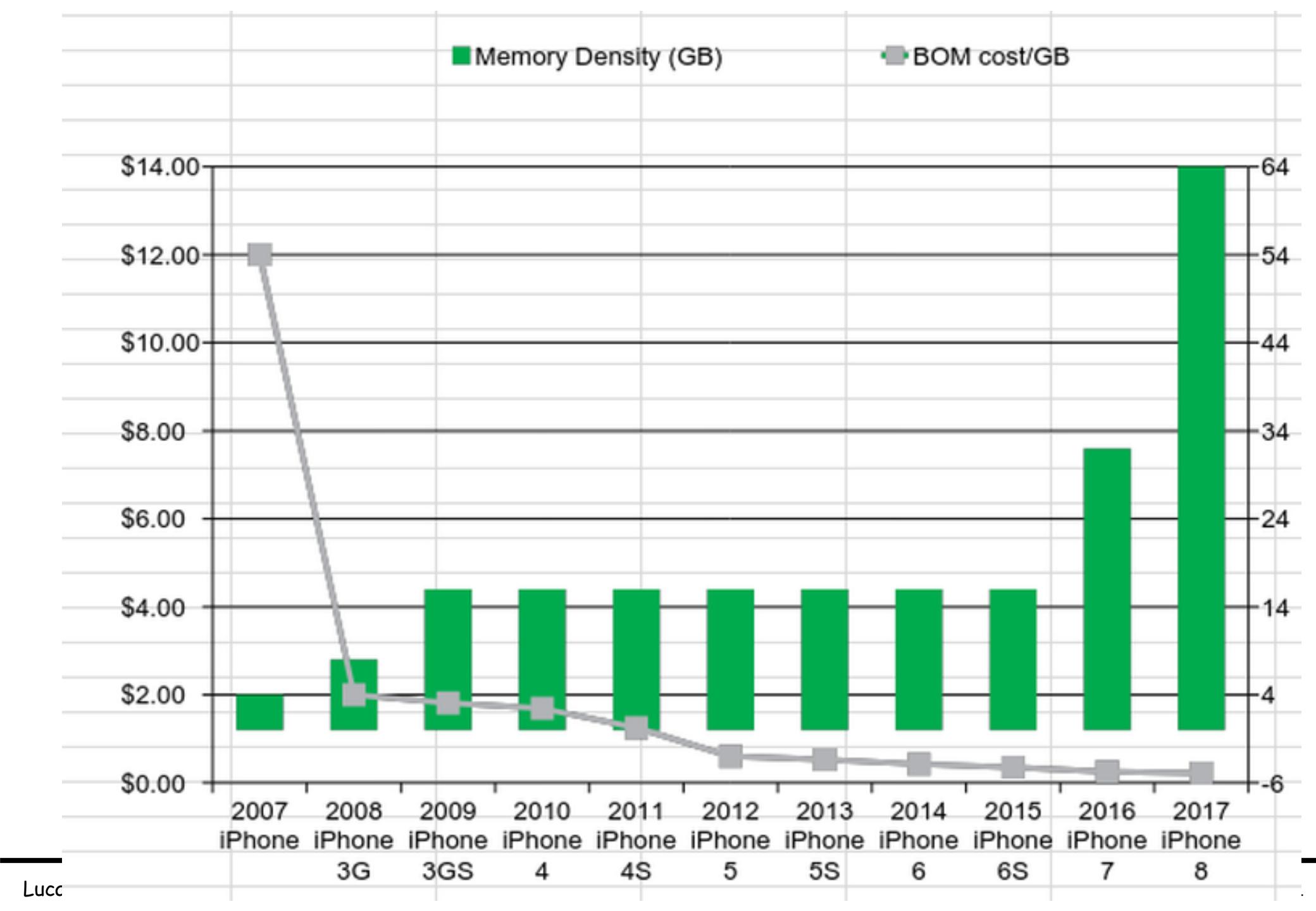
Total Cost Estimate 7+	\$270.88
<i>Cost Of Manufacturing</i>	\$6.78

<< iPhone 7 Plus Finalized

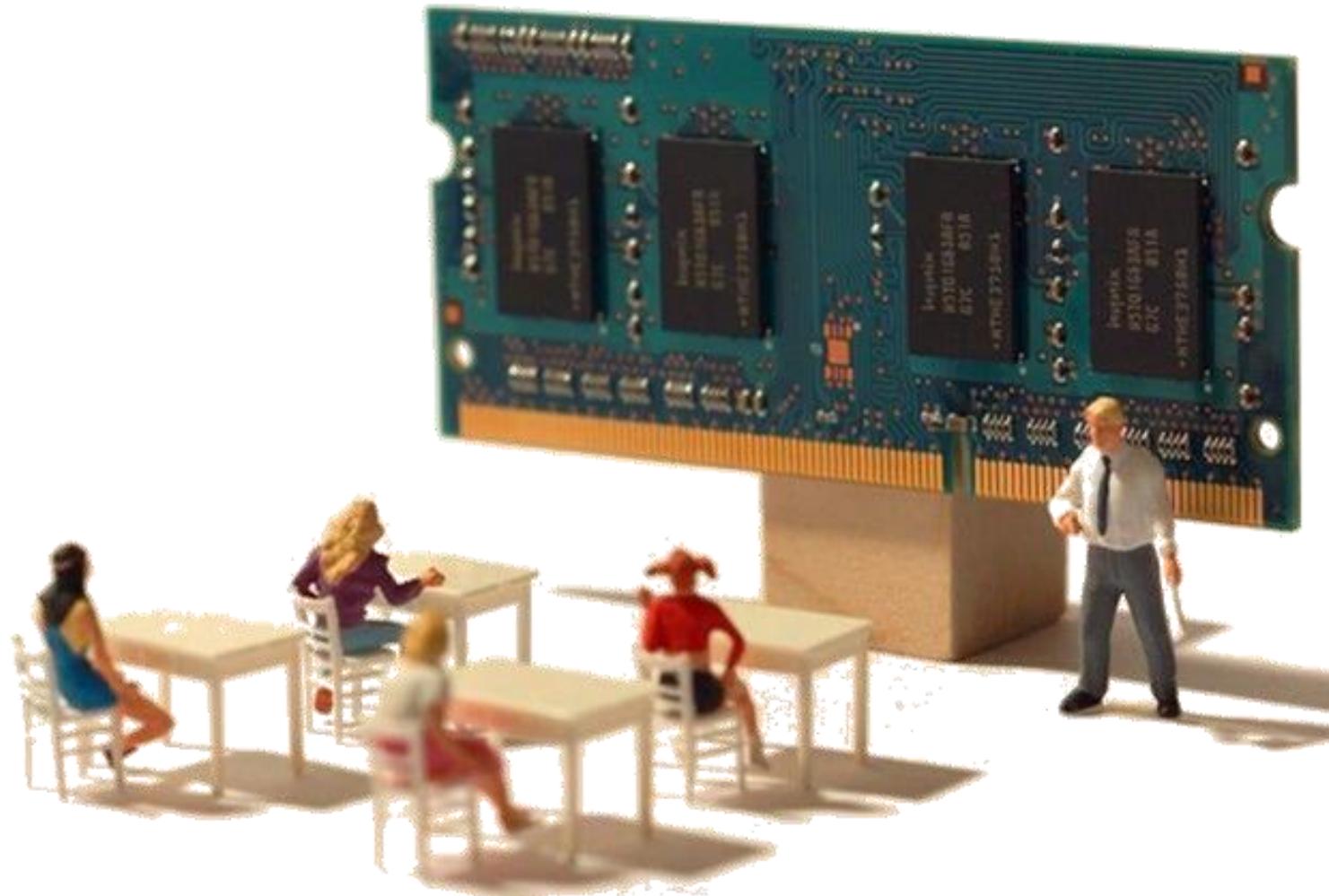
Itemized Components	MfgName	MfgPartNbr	Description	Total Cost	Comment
Display	JDI, LGD, Sharp		5.5" 1920x1080 IPS LCD w/ in-cell touch	\$52.5000	See comments tab
Mechanical / Electro-Mechanical Components				\$50.9500	
Chassis + Rear Enclosure			Enclosure, Main, Bottom, Machined 7000-Series Aluminum Alloy w/stainless insert and Gorilla glass rear cover		
Other Mechanical / Electro-Mechanical			PCBAs, Connectors, Taptic Engine, Other		
Cameras				\$32.5000	
Primary Camera Module			Dual, Wide-Angle F1.8 / Telephoto F2.8 12MP w/ OIS		1.2umx1.2um Pixel Size Wide Angle; 1.0x1.0um Pixel Size Telephoto
Secondary Camera Module			7MP F2.2		1.0umx1.0um Pixel Size
Memory				\$31.2000	
NAND (eMMC, MLC, ...)	SANDISK CORP	SDMPEGFI2 064G	Flash, NAND, 64GB, TLC		Samsung, Toshiba, SanDisk, Hynix are all vendors
DRAM	MICRON TECHNOLOGY INC	MT53D384M64D4NY-046 XT:D	SDRAM, LPDDR4, 3GB, PoP		
Apps Processor	Apple		Apple A11 Bionic, 64-Bit 6-Core CPU, 3- Core GPU, 10nm	\$27.5000	

Itemized Components	MfgName	MfgPartNbr	Description	Total Cost	Comment
RF / PA Section					\$24.6000
RF Transceiver	QUALCOMM	WTR5975	RF Transceiver, Multi-Mode, Multi-Band		
Transmit Modules	BROADCOM LTD	AFEM-8072	Transmit Module		
	SKYWORKS SOLUTIONS INC	SKY78140-22	Transmit Module		
PAMs	SKYWORKS SOLUTIONS INC	SKY77366-17	Transmit Module		
Other RF/PA			Remaining PAMs ad other RF components not listed above		
Power Management Components					\$16.0500
Apps Processor Power Management	DIALOG SEMICONDUCTOR GMBH		Power Management IC		
Baseband & Other Power Management	QUALCOMM	PMD9655	Power Management IC		
Wireless Charging Element + Supporting Compor	BROADCOM LTD	BCM59355A2IUB3G	Wireless Charging IC		
Other Power Management Components			Remaining power management lcs, regulators, converters, LED drivers, etc.		
Baseband IC	QUALCOMM	MDM9655	Baseband Processor, Multi-Mode, 14nm - CAT16 Modem	\$11.5000	
User Interface Components					\$11.2800
NFC Controller	NXP SEMICONDUCTORS	PN80V	NFC Controller		
Audio Codecs	CIRRUS LOGIC INC	338S00248	Audio Codec		
	CIRRUS LOGIC INC	CS35L26	Audio Power Amplifier		
Other			Includes camera flash, and other interface lcs		
Other Modules					
WLAN / BT Module(s)	MURATA	339S00399	BT / WLAN Module, IEEE802.11ac, Bluetooth 5.0	\$7.3500	
Sensors					\$6.6500
Fingerprint Sensor Module			Fingerprint Sensor Module		
Accelerometer / Gyroscope, 6-Axis			Accelerometer / Gyroscope, 6-Axis		
Electronic Compass	ALPS ELECTRIC CO LTD		Electronic Compass		
Barometric Pressure Sensor	BOSCH SENSORTEC GMBH	BMP28x	Barometric Pressure Sensor		
Color Sensor	AMS AG		Color Sensor		
Proximity - time-of-flight			Proximity - time-of-flight		
Battery Pack(s)	HUZHOU DESAY BATTERY CO LTD		Battery, Li-Polymer, 3.82V, 2691mAh, 10.28Wh	\$4.4500	
Box Contents					\$11.5500
Charger, 5V, 1A, AC to USB Type A			Includes pkg & literature		
Stereo w/ Apple Lightning Plug			Charger, 5V, 1A, AC to USB Type A		
Headphone Jack Adapter			Stereo w/ Apple Lightning Plug		
USB to Apple Lightning Cable			Headphone Jack Adapter		
			USB to Apple Lightning Cable		





Questions ?



Some Companies in this market

ARM®

TEXAS
INSTRUMENTS

intel®

BROADCOM®

NXP

QUALCOMM®

freescale™
semiconductor

M

MICROCHIP

dialog
SEMICONDUCTOR



ST
life.augmented

am u n

maxim
integrated™

infineon

ATMEL

Jobs' Profiles (some examples)

<https://www.apple.com/jobs/us/index.html>

<http://jobs.st.com/>

<http://www.qualcomm.com/careers>

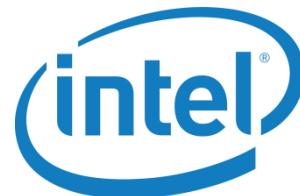
<http://www.imgtec.com/corporate/careers.asp>

<https://jobs.intel.com/page/show/careers>

<http://www.infineon.com/cms/en/corporate/career/infineon-jobsearch/>

<http://www.dialog-semiconductor.com/careers/>

<http://arm.com/careers/>



<https://www.apple.com/jobs/us/index.html>

The image shows the Apple Jobs homepage. At the top, there's a navigation bar with links for Mac, iPad, iPhone, Watch, TV, Music, Support, a search icon, and a shopping bag icon. Below the navigation, the title "Jobs at Apple" is displayed, along with links for About Apple, Teams, Apple Retail, Students, Profile, and a Search bar. The main visual features four large, stylized apples: one with a woman in a garden, one with a colorful outline, one with abstract geometric shapes, and one with a textured, colorful surface. In the bottom left corner, there's a cartoon apple character with a smiling face and a bite taken out of it. The central text "Join us. Be you." is displayed in large white letters, with a call-to-action "Watch the film" and a play button icon below it. The bottom right corner features a close-up of a yellow and orange apple.

Mac iPad iPhone Watch TV Music Support

Jobs at Apple

About Apple Teams Apple Retail Students Profile Search

Join us. Be you.

Watch the film

Digital Design Engineer

Livorno, Italy
Hardware

Summary

Posted: Feb 26, 2020
Role Number: 200154676

At Apple, we work every single day to craft products that enrich people's lives. Do you love working on challenges that no one has solved yet? Do you like changing the game? We have an opportunity for a visionary and uncommonly talented RTL Design Engineer. As a member of our dynamic group, you will have the rare and rewarding opportunity to craft upcoming products that will delight and inspire millions of Apple's customers every single day.

You will join the DDR PHY design team. We provide best-in-class PHY designs for high-performance, low power applications. As a logic design engineer, you will be involved in all phases of the design, from concept study, architecture definition, design and verification, to silicon bring-up and characterization.

Key Qualifications

- - The ideal candidate will have several years experience in digital design including RTL design experience
 - - Knowledge of best practices with respect to implementation of digital logic
 - - Understanding of digital design flow including RTL simulation, logic synthesis, timing constraints, timing closure, STA, back annotation of parasitics, gate level simulation, equivalence checking
 - - Understanding of Design Verification and the ability to write self-checking test suites
 - - Ability to write assembly level code and higher level code
 - - Ability to analyze a design and partition between HW implementation and SW control
 - - Experience in hands-on lab evaluation
 - - Understanding of ASIC test methodology such as scan insertion, memory BIST and test pattern generation
 - - Good written and verbal communication skills
 - - Experience in working with international teams
-

Description	<ul style="list-style-type: none">- Work with systems team to understand the top level requirements of the digital functions and develop detailed specifications- Implement the function in Verilog RTL to specification- Partition the function between HW and FW for most efficient implementation- Develop RTL and FW to implement the function- Perform unit level testing on the RTL function
	<p>Other responsibilities could include:-</p> <ul style="list-style-type: none">- RTL synthesis- Equivalence checking oStatic Timing Analysis- Support the DV team by writing self-checking tests as required- Develop FW to support DV and ATE environments

Education & Experience	Masters Degree in Electrical Engineering or equivalent experiences
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Additional Requirements	Apple is an Equal Opportunity Employer that is committed to inclusion and diversity. We also take affirmative action to offer employment and advancement opportunities to all applicants, including minorities, women, protected veterans, and individuals with disabilities. Apple will not discriminate or retaliate against applicants who inquire about, disclose, or discuss their compensation or that of other applicants.
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<http://www.qualcomm.com/careers>



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$$\begin{aligned}P_a &= P_i G_i C_i \\&\quad (K+R) \\S_f &= 4Vd \\&+ \left(\frac{I_0}{I_D} \right) \\&+ 7\% \uparrow\end{aligned}$$

Jobs' Profiles (some examples)



jobs.qualcomm.com/public/jobDetails.xhtml?requisitionId=1973218



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Job Postings

[Security Red-Team Engineers \(up to Senior Staff/Principal Engineer level\) - QCT, Cork, Ireland](#)

[Low Power Design/Methodology Engineer\(s\) All levels - QCT, Cork, Ireland](#)

Job Detail

Job Id E1973218

Job Title Digital ASIC Design Engineers (up to Senior Staff/Principal Engineer level) - QCT, Cork, Ireland

Post Date 02/25/2020

Job Detail

Job Id	E1973218
Job Title	<u>Digital ASIC Design Engineers</u> (up to Senior Staff/Principal Engineer level) - QCT, Cork, Ireland
Post Date	02/25/2020
Company	<u>Qualcomm Technologies, Inc.</u>
Job Area	Engineering - Hardware
Location	<u>Ireland - Cork</u>
Job Overview	<p>Qualcomm is a company of inventors that unlocked 5G ushering in an age of rapid acceleration in connectivity and new possibilities that will transform industries, create jobs, and enrich lives. But this is just the beginning. It takes inventive minds with diverse skills, backgrounds, and cultures to transform 5Gs potential into world-changing technologies and products. This is the Invention Age - and this is where you come in.</p>

About the role

We are seeking Digital Design Engineers for our SnapDragon team in Cork, Ireland. The Cork site is home to a range of digital IP teams working on cutting edge IP for the latest Snapdragon chip sets. The team work on IPs related to security, encryption, power control, contextual awareness, debug, profiling and processing. Each team is working with the latest tools and digital design and verification techniques in bleeding edge silicon nodes, 10nm and below. High quality and low cost are all key design points for our products.

Team members work directly with architecture, software and SoC teams in Ireland and other global Qualcomm locations. Low power micro-architecture and efficient verification are valued design techniques.

Successful candidates will be responsible for leading and participating in the design of leading-edge ASIC's and SoC's, in advanced digital CMOS processes for multi-function mobile platforms.



Where you will be working

Cork has a proud reputation as Ireland's second largest economic engine and is now one of the Top 20 location choices in Europe with 39,000 people being employed by over 170 overseas companies. There's a growing diversity in the region with people from many nationalities relocating to Cork, relishing the opportunity to work and live in a location that offers an excellent quality of life. A gateway to Europe, Cork airport provides access to almost 50 international destinations including transatlantic air routes.

About Us

Qualcomm Cork, a greenfield site based in the beautiful harbour city of Cork opened its doors in August 2013 and has been growing ever since across our QCT Engineering, OneIT and HR teams.

The Cork QCT engineering team is now over 220+ engineers strong and is continuing to expand. Our engineers work on all aspects of leading-edge technology (7nm, 5nm), including; Analog Mixed Signal, Security, Power Management, Sensors, Machine Learning, Modelling, Validation, Design Automation, Automotive and Physical Design. We are the R&D engine that benefits the world in three ways: Enabling Customers, Transforming Industries and Enriching Lives.

Equal Opportunities

We are an Equal Opportunity employer; all qualified applicants will receive consideration for employment without regard to race, colour, religion, sexual orientation, gender identity, national origin, disability, veteran status, or any protected classification.

Giving Back

Employees in Cork have a strong sense of community. We are encouraged through the philanthropic endeavours of the Qualcomm Foundation to support causes that matter to us.



Apart from working in an open, relaxed and collaborative space, you will enjoy:

- Salary, stock and performance related bonus
- Employee stock purchase scheme
- Matching pension scheme
- Education Assistance
- Relocation and immigration support
- Life, Medical, Income and Travel Insurance
- Subsidised gym membership
- Bicycle purchase scheme
- As much Nespresso as you can handle!!!
- Free fruit every Monday and Wednesday
- Employee run clubs, including, running, football, chess, badminton + many more
- Bachelor's degree in Science, Engineering, or related field.
- 2+ years ASIC design, verification, or related work experience.

Minimum Qualifications

*References to a particular number of years experience are for indicative purposes only. Applications from candidates with equivalent experience will be considered, provided that the candidate can demonstrate an ability to fulfil the principal duties of the role and possesses the required competencies.

This position requires detailed knowledge of:

- ASIC design experience including architecture, RTL design in Verilog/VHDL, low power design techniques, UPF.
- Experience with synthesis, and timing closure.
- Experience with DC, LINT, PTSI, and CDC.
- Experience working in a multi-disciplinary, global team focused on advanced, high volume applications

Required: Bachelor's, Electrical Engineering

Preferred: Master's, Electrical Engineering



<https://jobs.intel.com/page/show/careers>

The image shows the homepage of the Intel careers website. At the top, there is a blue header bar with the Intel logo and navigation links for "Discover Intel" and "Careers at Intel". On the right side of the header is a "Accessibility" button. Below the header is a large, semi-transparent overlay image of a woman with blonde hair, wearing a black and white striped shirt, resting her chin on her hand in a thoughtful pose. In the bottom left corner of this overlay, the text "FIND YOUR CAREER AT INTEL" is displayed in large, bold, white letters. Below this main heading, the tagline "Take a Look Inside" appears in smaller white text. In the top right corner of the overlay, there is a green rectangular button with the text "Join the talent network". The background of the page is a blurred photograph of several people in what appears to be a professional office or conference setting.

<https://www.infineon.com/cms/en/careers/>

The screenshot shows the Infineon careers page. At the top, there's a navigation bar with links for Newsletter, Contact, Where to Buy, English (dropdown), myInfineon (dropdown), Cart, and a search bar. Below the navigation is a main menu with links for Products, Applications, Tools, About Infineon, Discoveries, and Careers (which is highlighted in red). Under the Careers link, there are sub-links for Job Search, Working at Infineon, Our Locations, Opportunities and Benefits, Students & Pupils, and How to apply. The main content area features a large image of a man sitting with three young children (two girls and one boy) looking at a laptop screen. To the right of this image is a green sidebar with the title "Work-Life Balance". It contains a testimonial: "Martin from Warstein manages 12 employees – in part time to share responsibility with his wife to raise their three children..". Below the testimonial is a "Find out more" button with a right-pointing arrow. At the bottom of the main image, there are five small circular dots, with the third one being dark grey to indicate it's the current slide.

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Work-Life Balance

Martin from Warstein manages 12 employees – in part time to share responsibility with his wife to raise their three children..

Find out more >



You are here: Home / Career Service



Avvisi

- » Samsung Innovation Campus 2022 - Calendario ed aule
- » Recruiting Sport Day - Decathlon: il 26 ottobre metti in campo le tue competenze!
- » Career Labs 2022: Calendario dei prossimi mesi!
- » Consulenza e appuntamenti on-line: posti disponibili. Prenotate sul portale Career Center
- » Eventi di Public Engagement: come darne visibilità

Vedi tutto

Offerte di lavoro



Aggiorna il tuo CV



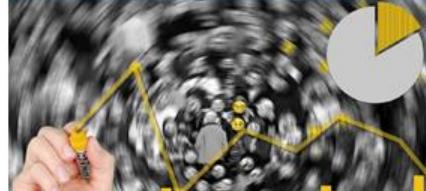
Workshop e consulenza



Le aziende si presentano



Indagini e studi



Alumni



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[!\[\]\(1c9e8c35be91781cc2540a51bf5e7c28_img.jpg\) For researchers](#)[!\[\]\(03c8e8920460c0d6fad49390c7dfeb8b_img.jpg\) For industry](#)[!\[\]\(eda778e550f84ec809f42c07f6480eb4_img.jpg\) For projects and interest groups](#)[!\[\]\(9612336da27a48522ca3249f80364abe_img.jpg\) For students](#)[!\[\]\(439156975fc820919f408e67be503370_img.jpg\) For innovators](#)

HiPEAC provides grants for industrial and academic placements, and opportunities to learn from the best computing professors in the world. It is an incubator for the next generation of computing systems talent.

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- Take part in a Student Heterogeneous Programming Challenge and Inspiring Futures careers session at [Computing Systems Week](#)
- Publish your 'three-minute thesis' or internship report in the [HiPEAC magazine](#)

Questions ?

