Electronics and Communication Systems
Electronics Systems

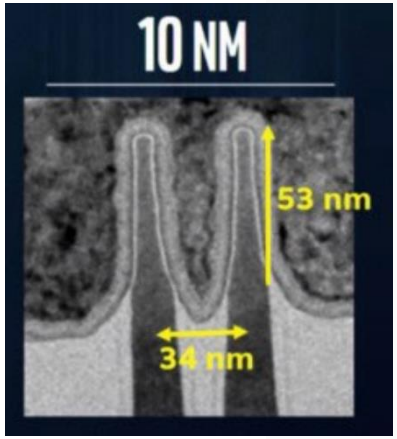
Master Degree in Computer Engineering

https://computer.ing.unipi.it/ce-lm

Luca Fanucci
Dipartimento Ingegneria dell'Informazione
Via Caruso 16 - I-56122 - Pisa - Italy
Phone: +39 050 2217 668
Fax: +39 050 2217 522
Mobile: +39 347 5013837
Email: luca.fanucci@unipi.it

MicroProcessor

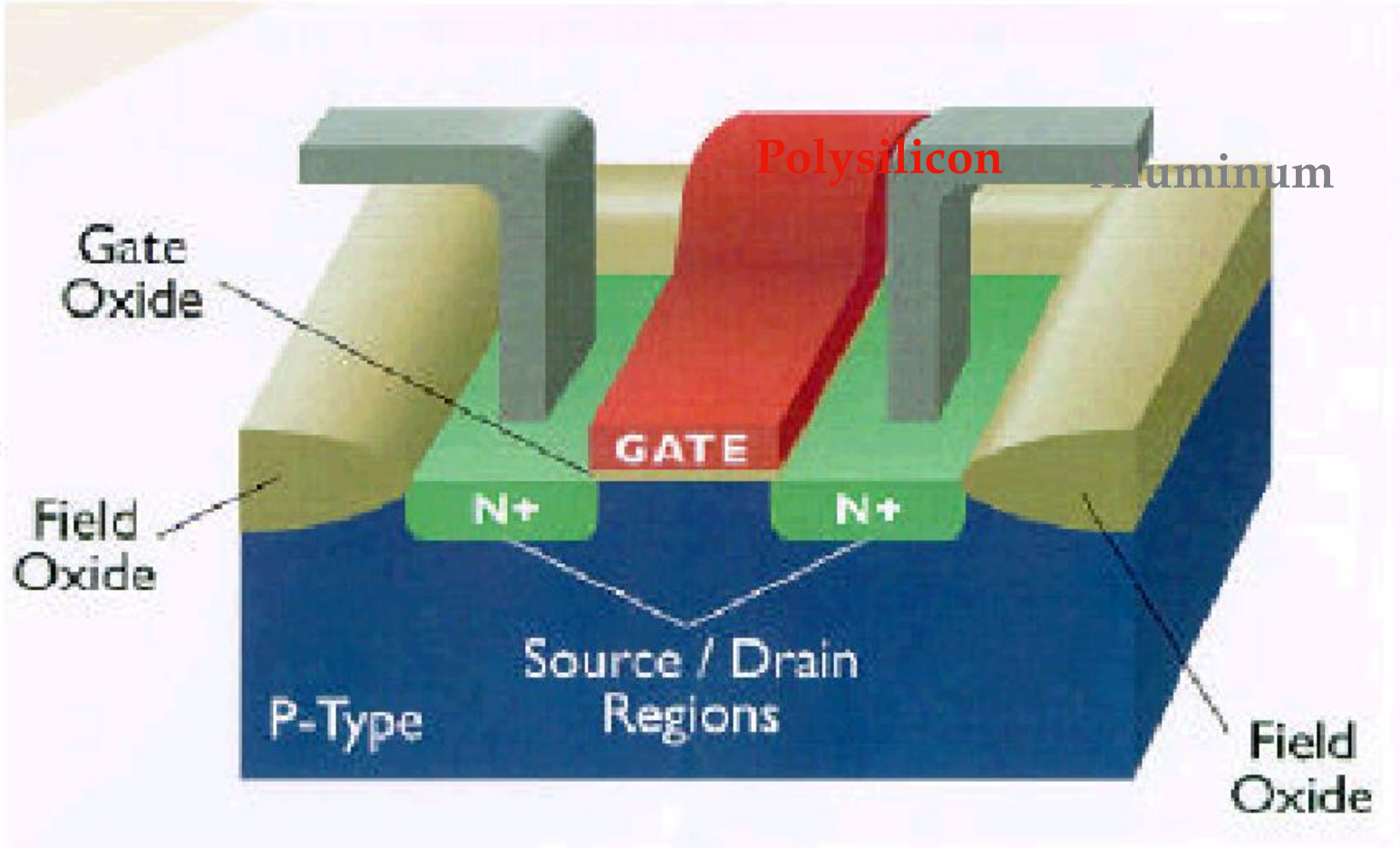
4.3
billion
TRANSISTORS



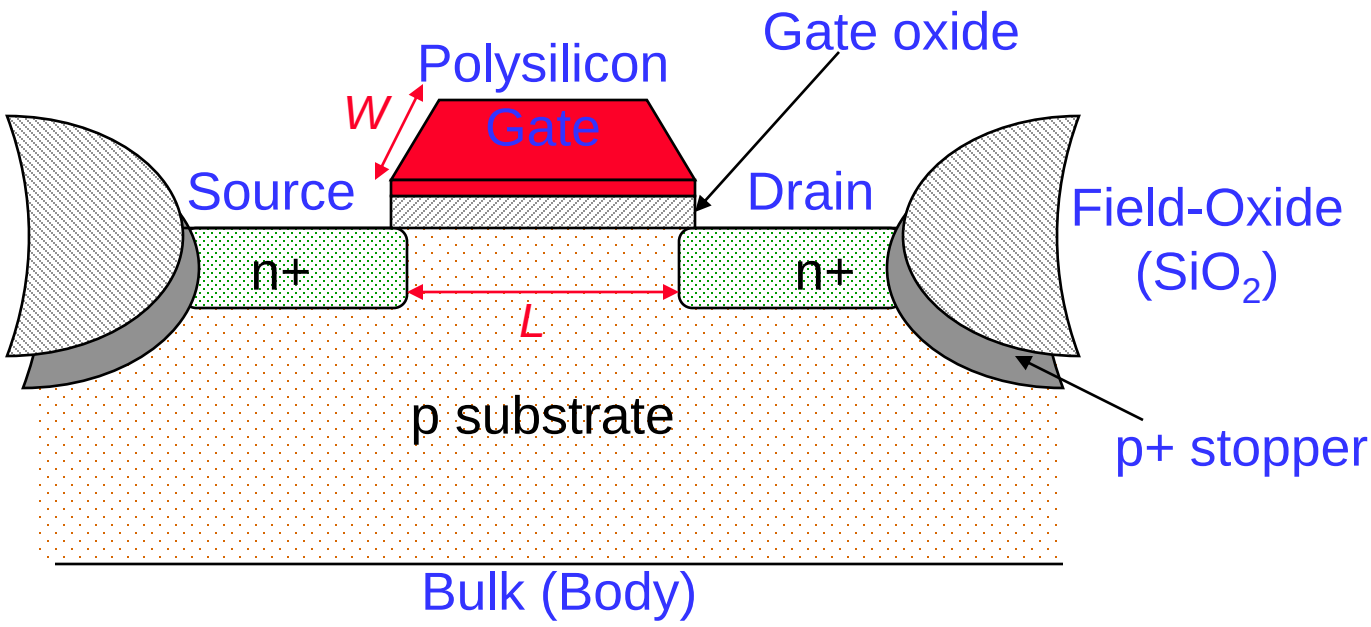
Outline

- MOS Transistor Switch Model
- Pass Gate
- Inverter
- Review of IC Manufacturing

The MOS Transistor



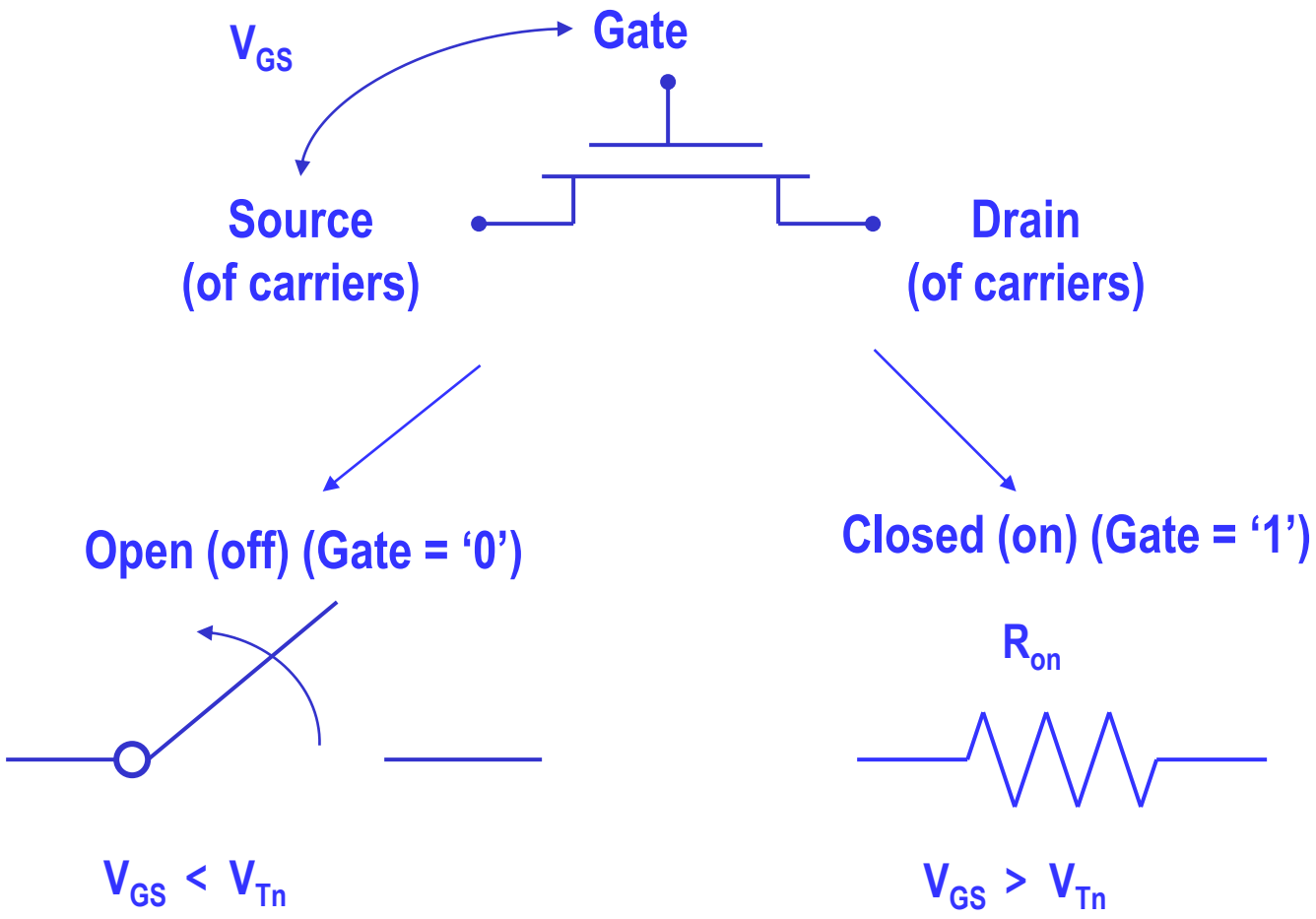
The NMOS Transistor Cross Section



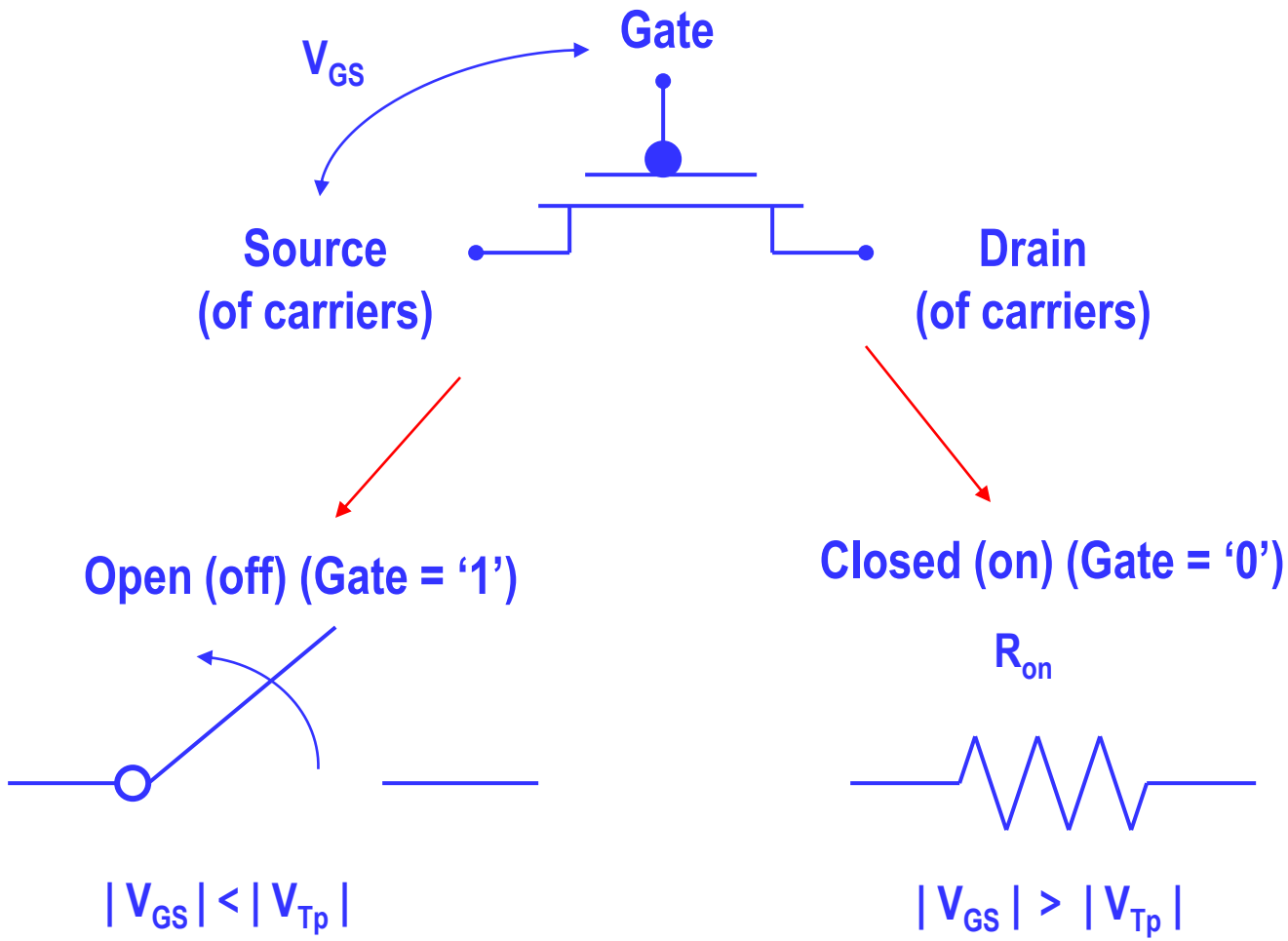
The NMOS – Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5 V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, 0.8, 0.7, …
  - Gradually scaling down as transistors shrink

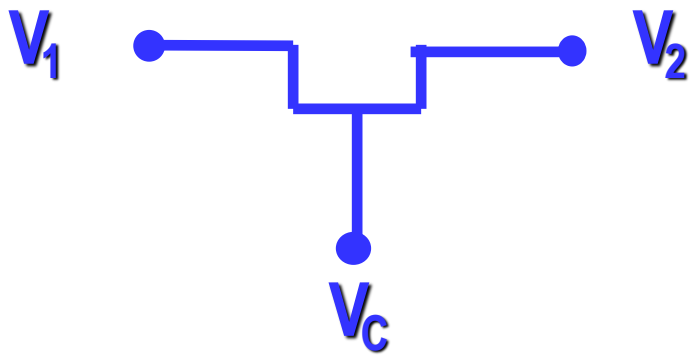
Switch Model of NMOS Transistor



Switch Model of PMOS Transistor



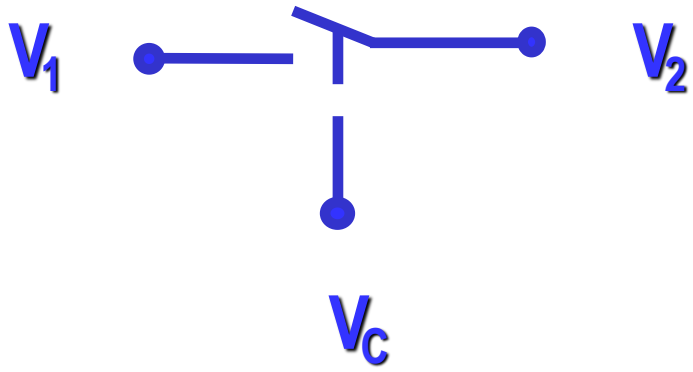
CONTROLLED SWITCH



$V_C = V_H$ CONDUCT

$V_C = V_L$ BLOCK

CONTROLLED SWITCH

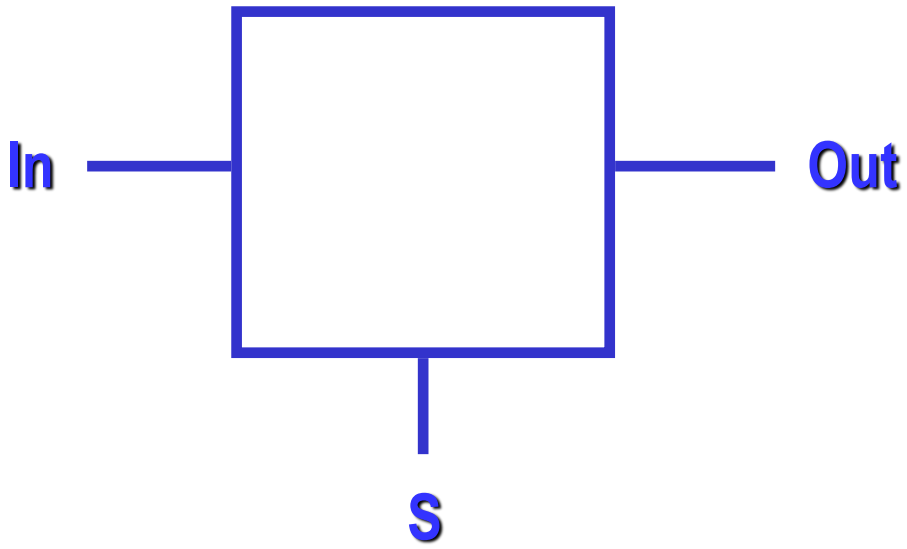


$V_C = V_H$ CLOSE

$V_C = V_L$ OPEN

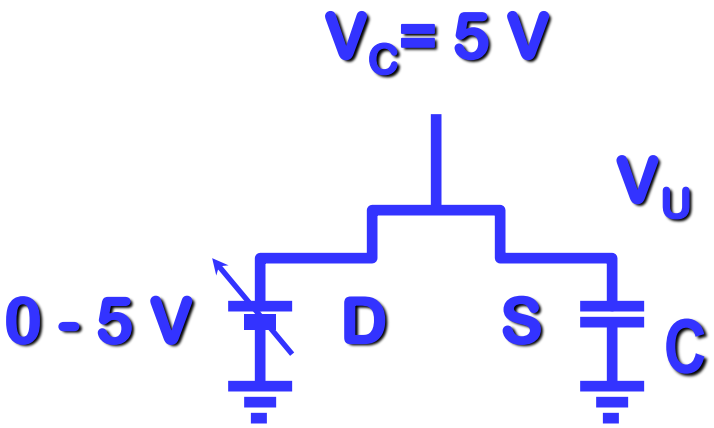
PASS GATE

- Three-state logic gates: high (H), low (L) and high-impedance (Z)



S	In	Out
0	0	Z
0	1	Z
1	0	0
1	1	1

PASS TRANSISTOR
Equivalent Resistance



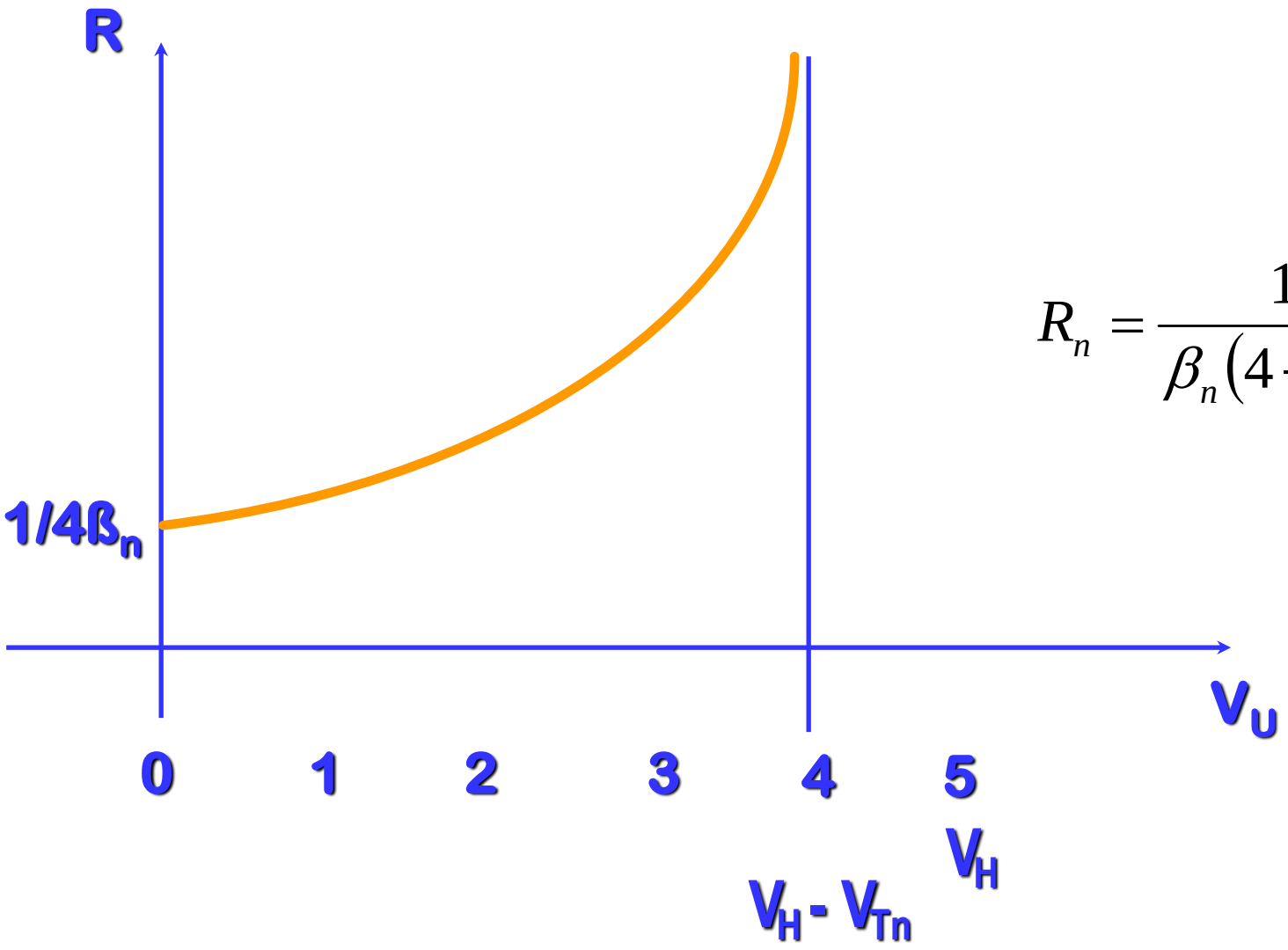
$$I_D = \beta_n\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \approx \beta_n\left(V_{GS} - V_T\right)V_{DS}$$

$$\frac{1}{R} = \frac{dI_D}{dV_{DS}} = \beta_n\left(V_{GS} - V_T\right)$$

$$R = \frac{1}{\beta_n\left(V_{GS} - V_T\right)} = \frac{1}{\beta_n\left(4 - V_U\right)}$$

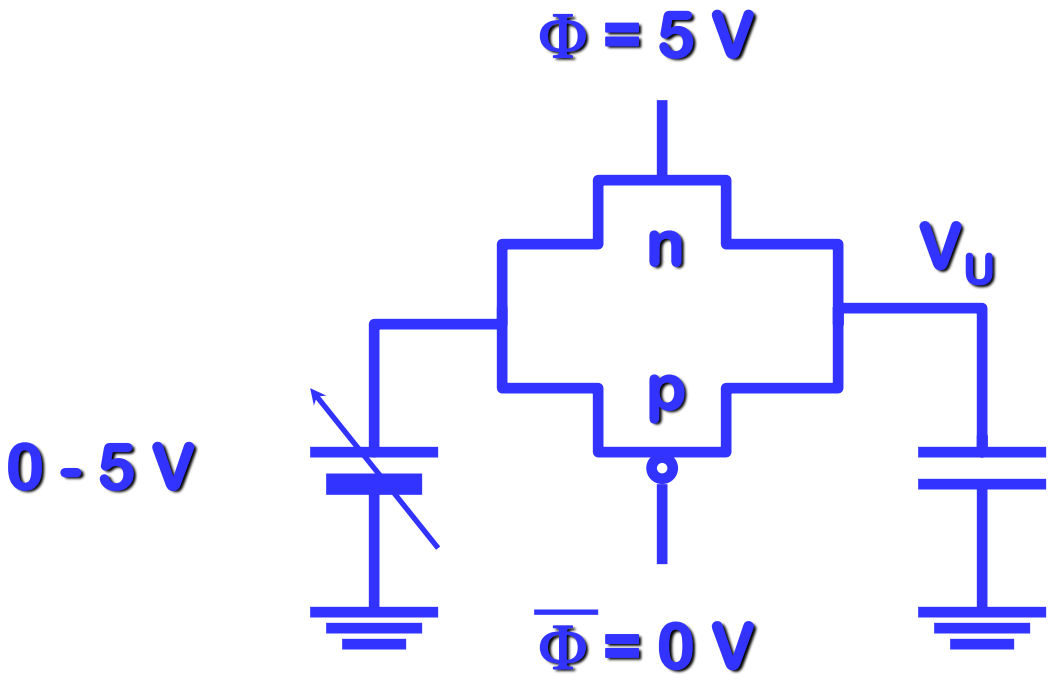
$V_T = 1\ V$

Equivalent Resistance Graph



$$R_n = \frac{1}{\beta_n (4 - V_U)}$$

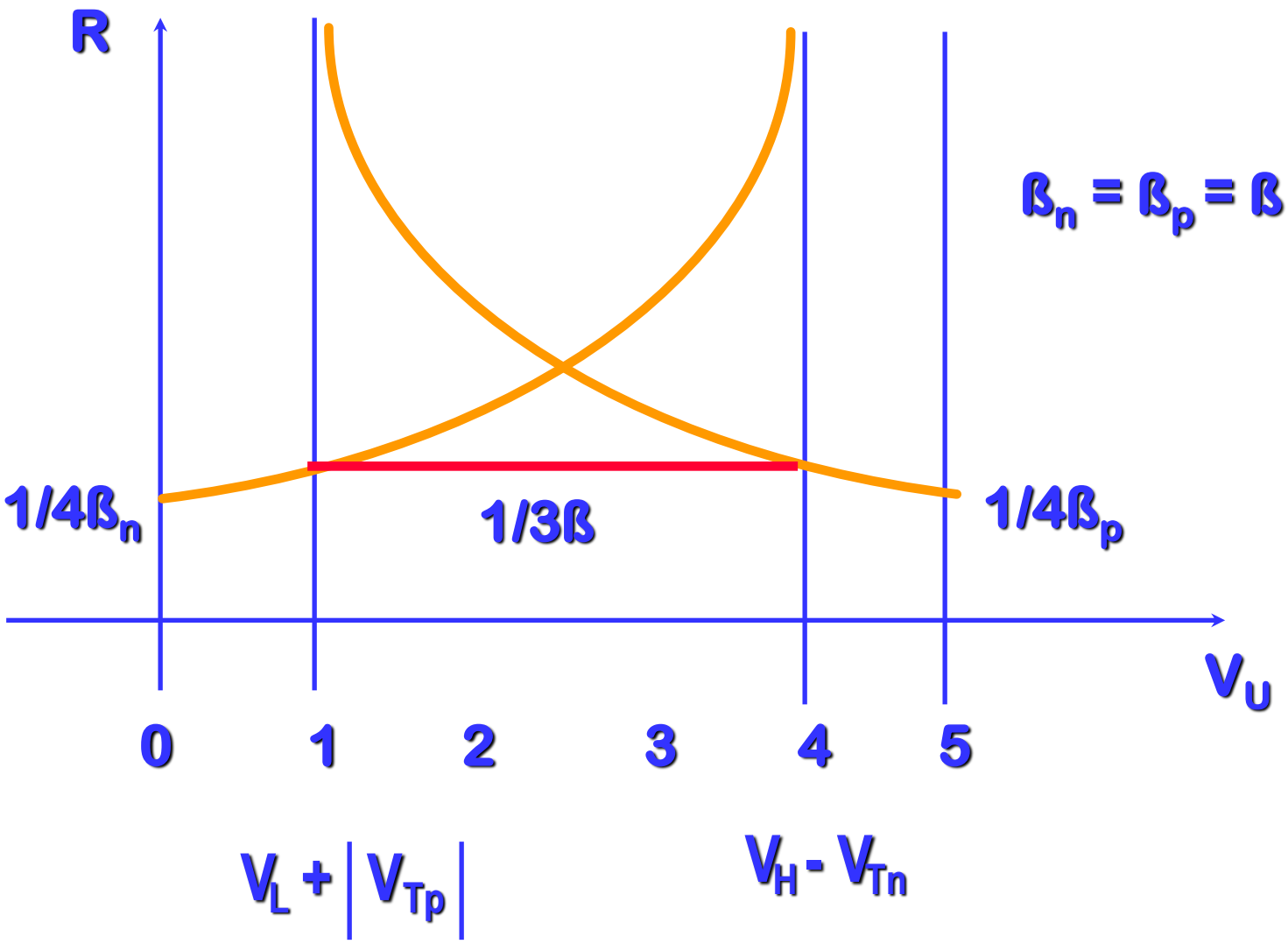
PASS GATE Equivalent Resistance



$$R_n = \frac{1}{\beta_n\left(4 - V_U\right)}$$

$$R_p = \frac{1}{\beta_p\left(V_U - 1\right)}$$

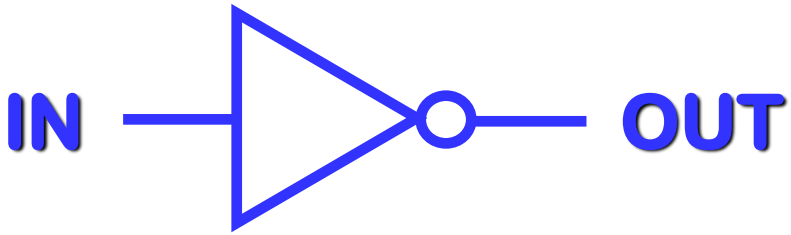
Equivalent Resistance Graph



INVERTER

- Implementation of the logic NOT Function

Logic Symbol

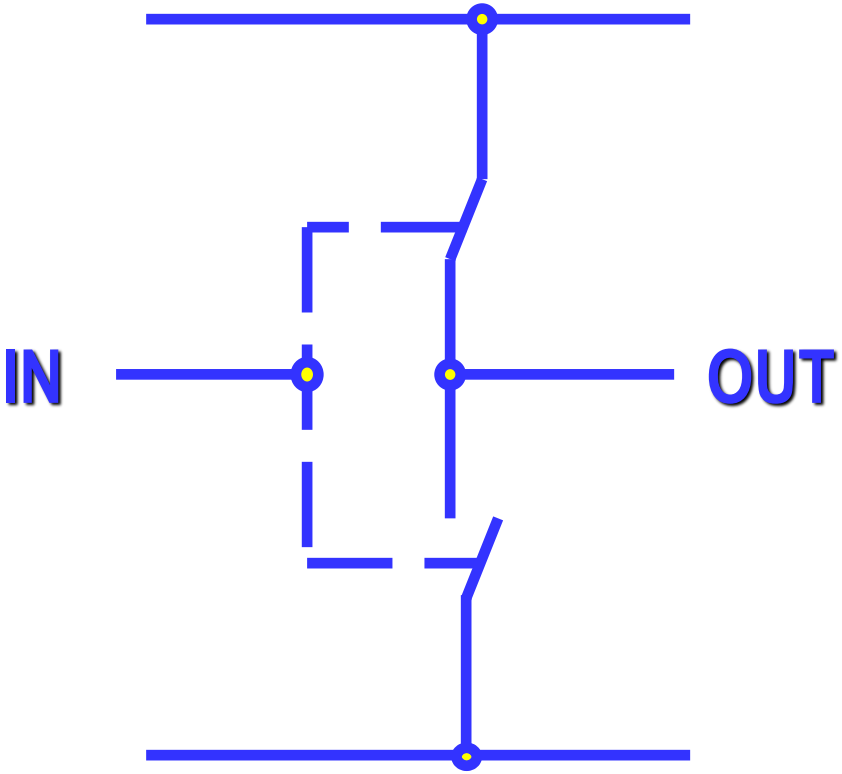


Truth Table

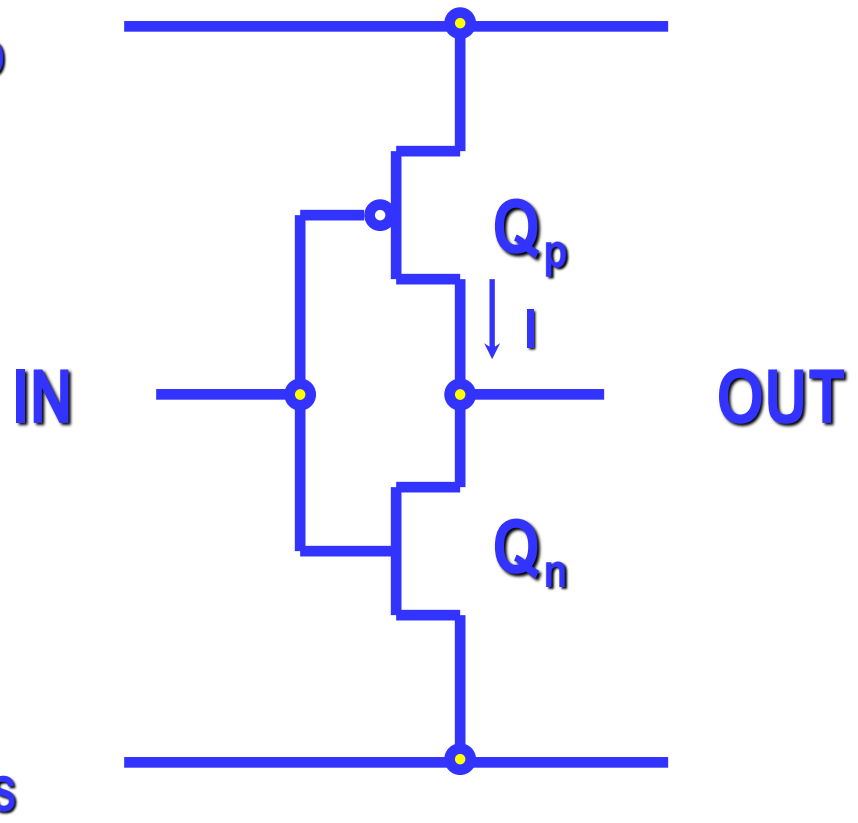
IN	OUT
0	1
1	0

INVERTER Circuit

Switch based idea

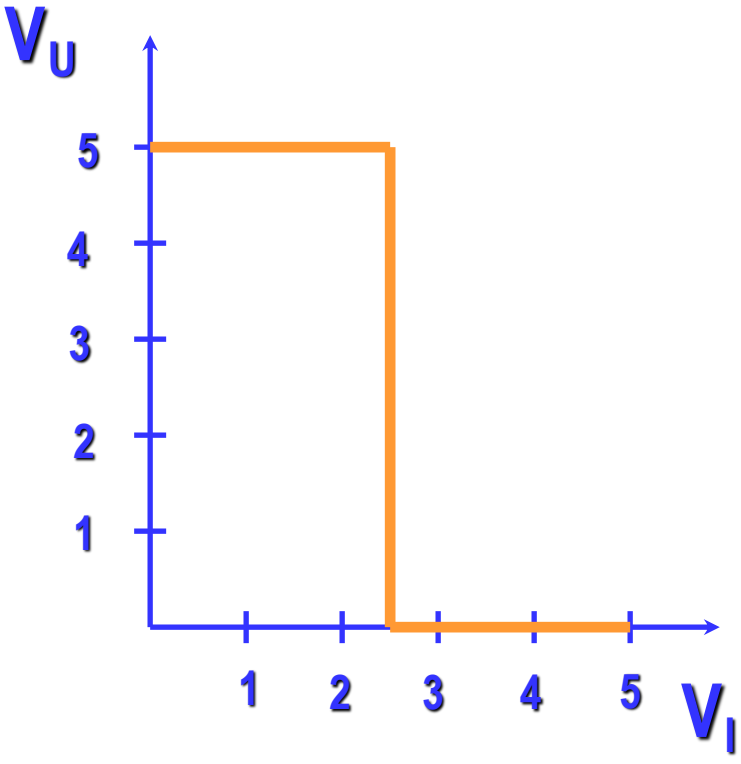


CMOS

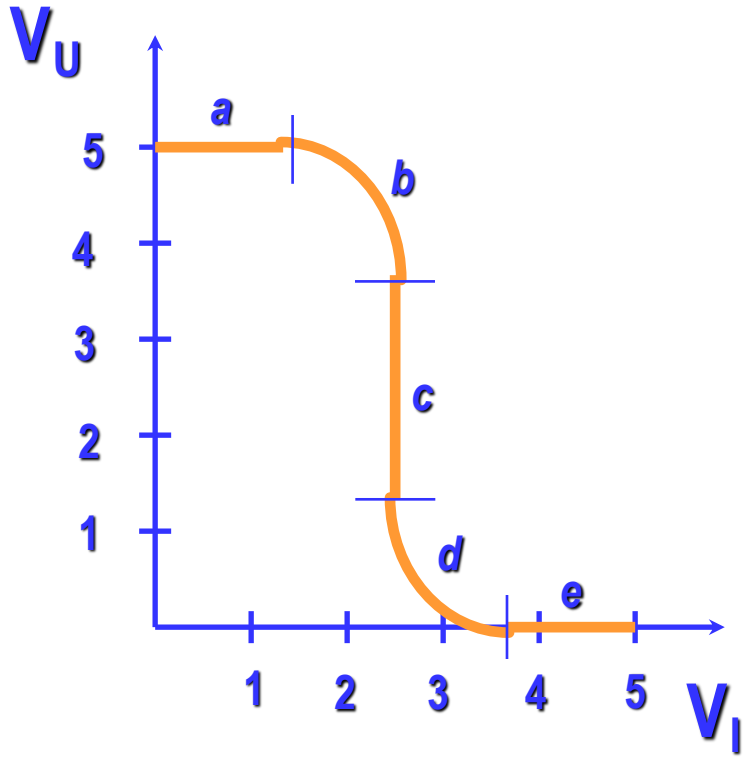


INVERTER Voltage Transfer Curve

IDEAL

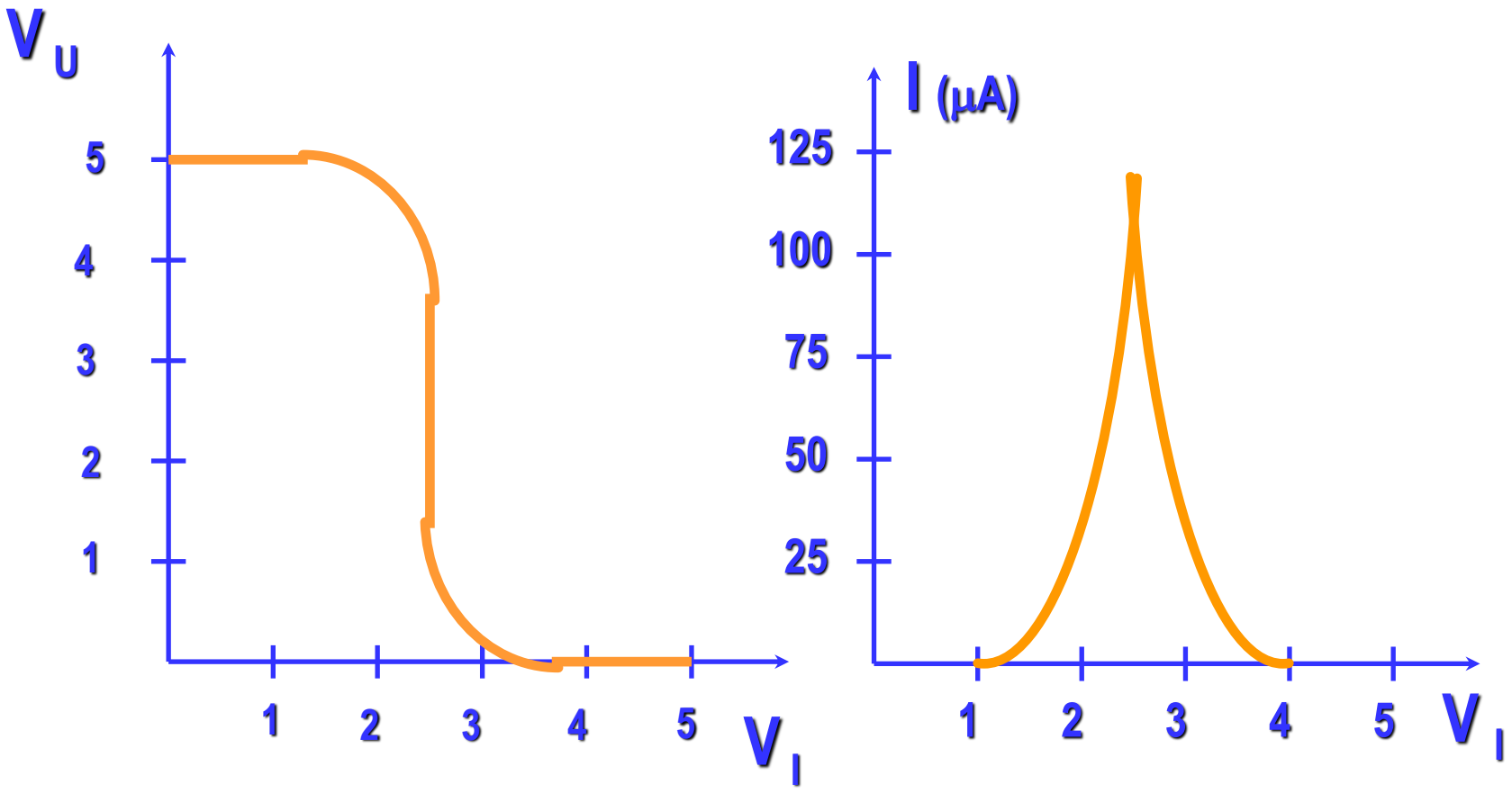


REAL

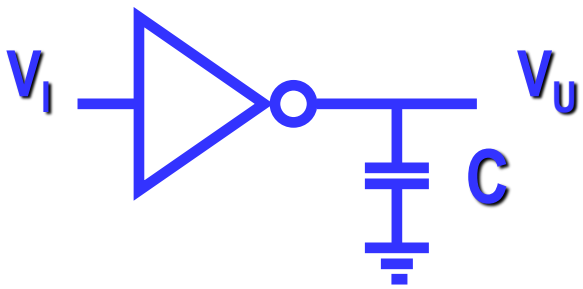


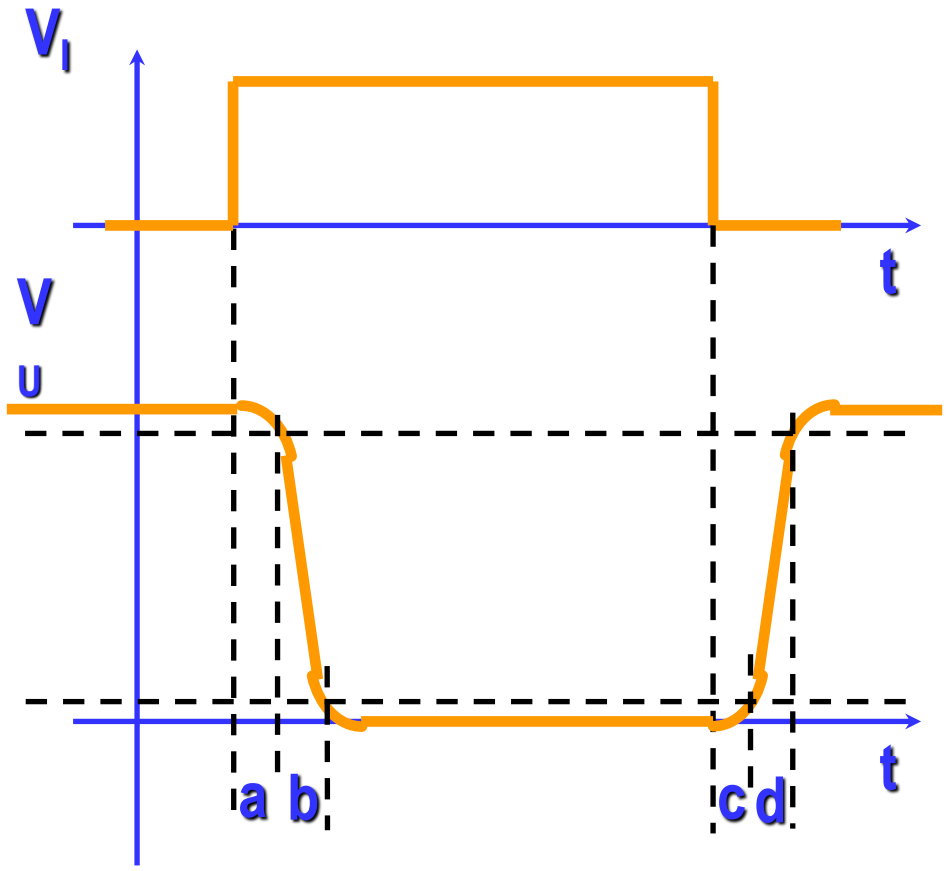
Current Transfer Curve

✧ With $\beta_n = \beta_p$



Driving Capacitive Loads



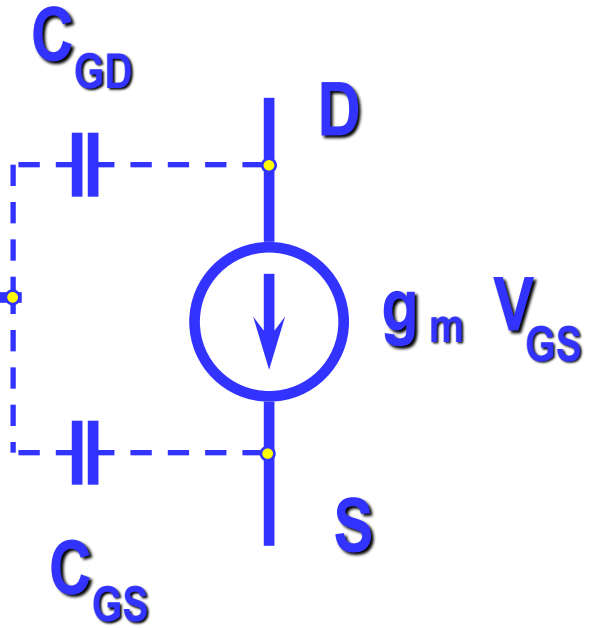


Capacitance

- Input Capacitance of driven Gates
- Drain-Sub and Source-Sub Juction Capacitance

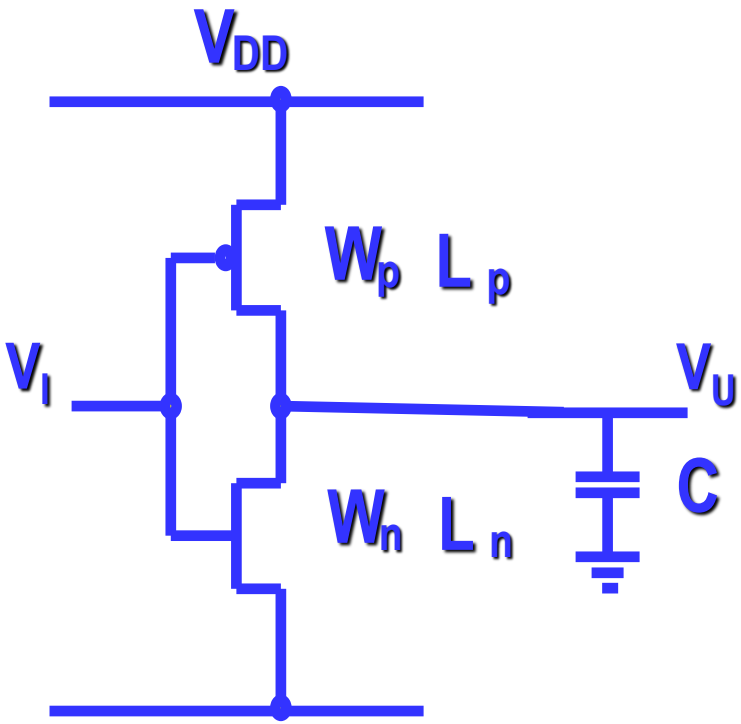
$C_G = C_{ox} W*L$

$C_{ox} = \varepsilon_{ox} / t_{ox}$

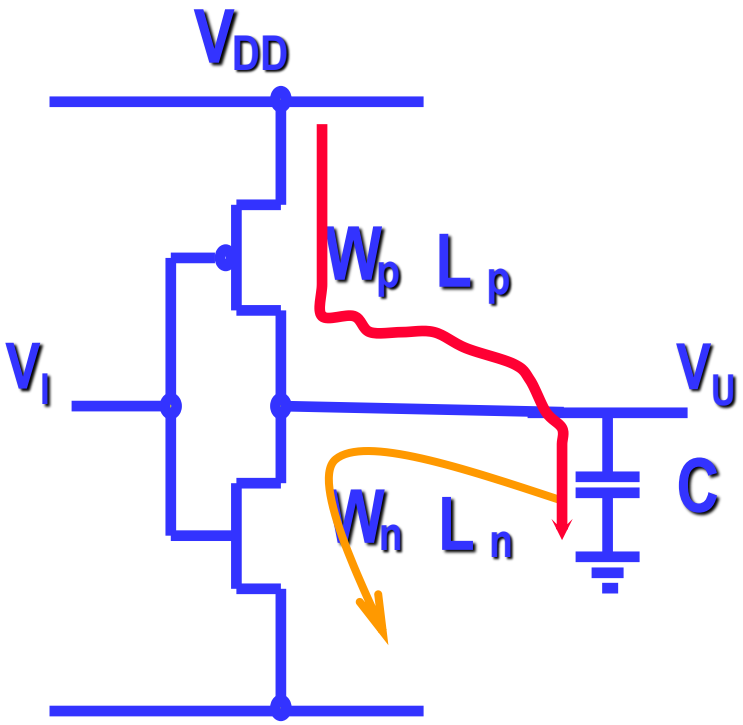


- Routing Capacitance

Propagation Delay



Propagation Delay



$$t_{pHL} \propto \frac{KC}{\beta_n} \frac{1}{V_{DD} - V_{Tn}}$$

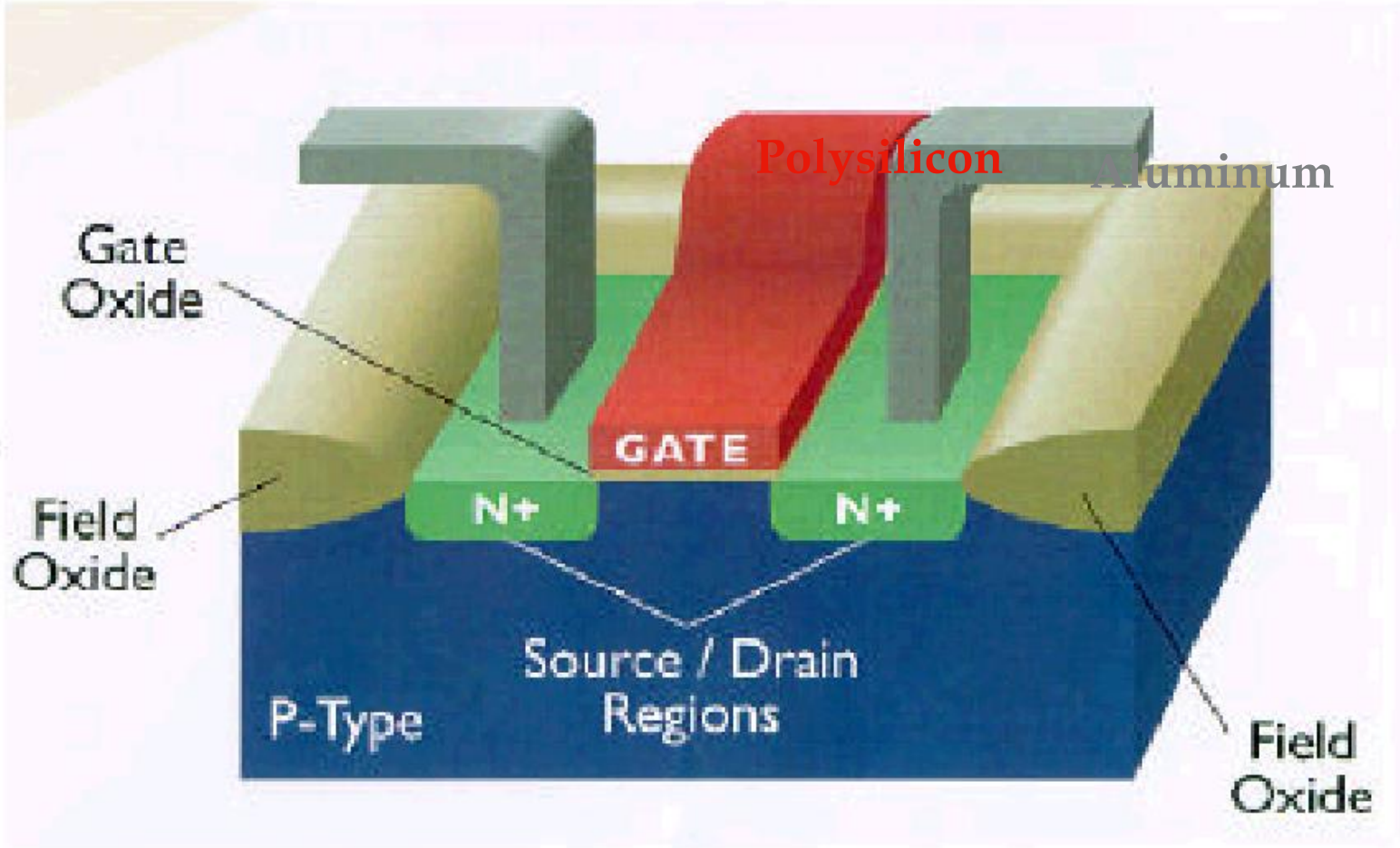
$$t_{pLH} \propto \frac{KC}{\beta_p} \frac{1}{V_{DD} + V_{Tp}}$$

$$\beta_n = \mu_n C_{ox} \frac{W_n}{L_n} \qquad \beta_p = \mu_p C_{ox} \frac{W_p}{L_p}$$

Power Consumption

- **Charge**: Capacitor store energy $E_C = ½ CV^2$
- Power Supply provides energy $E_f = CV^2$
- **Discharge**: Capacitor gives its energy to the inverter
- In one cycle the inverter consumes an energy equal to $E_D = CV^2$
- In the time T the inverter consumes a power cosuption of $P_D = E_D/T = P_D = C V^2 / T = C V^2 f$

The MOS Transistor

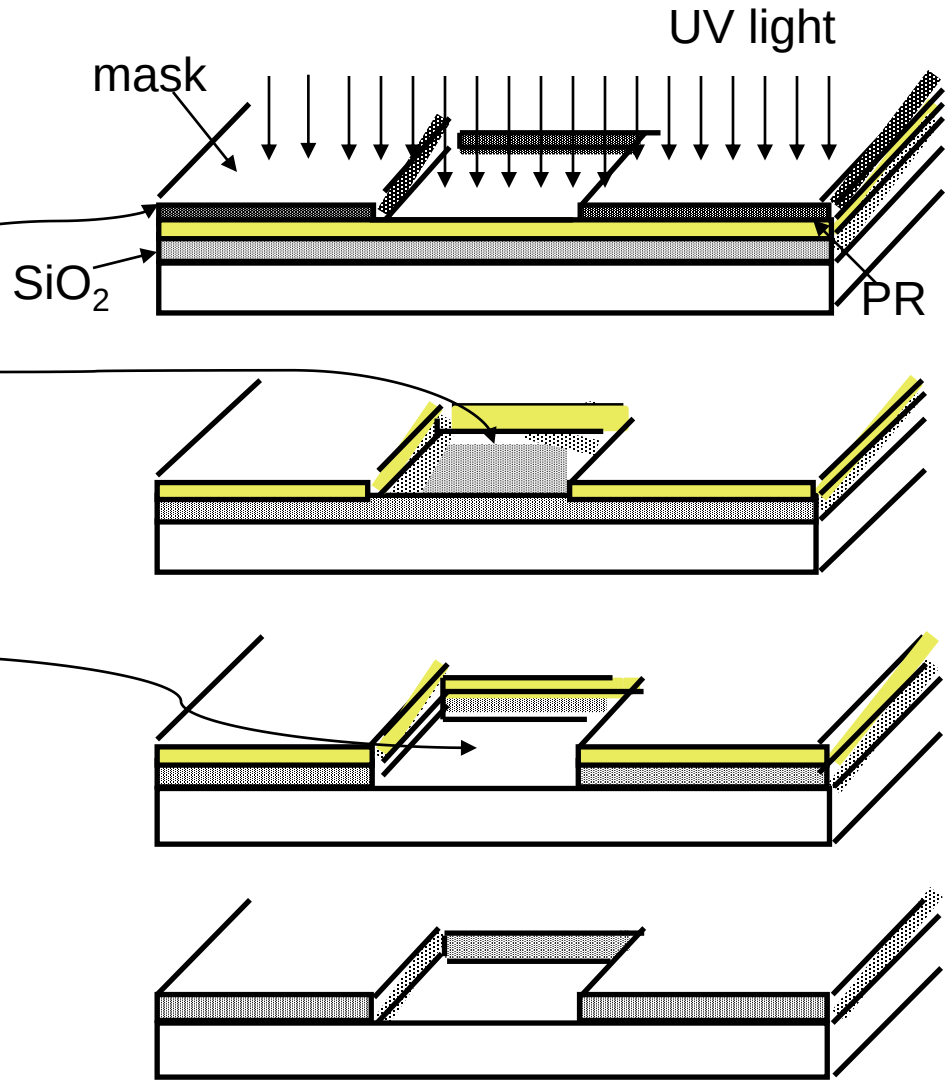


CMOS Fabrication

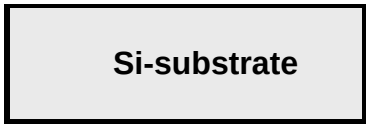
- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

Patterning - Photolithography

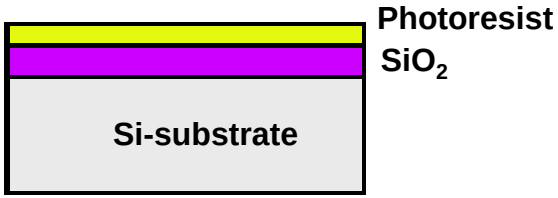
1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure
4. Photoresist development and bake
5. Acid etching
   - Unexposed (negative PR)
   - Exposed (positive PR)
6. Spin, rinse, and dry
7. Processing step
   - Ion implantation
   - Plasma etching
   - Metal deposition
8. Photoresist removal (ashing)



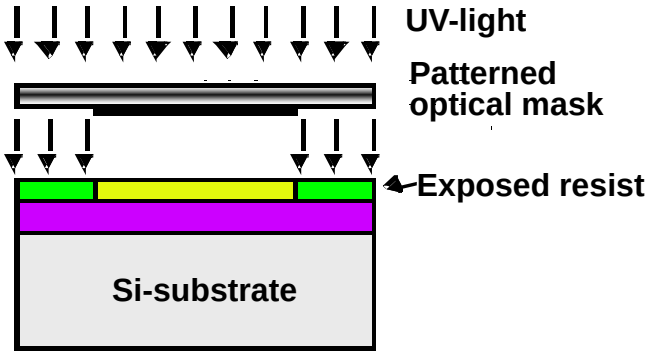
Example of Patterning of SiO2



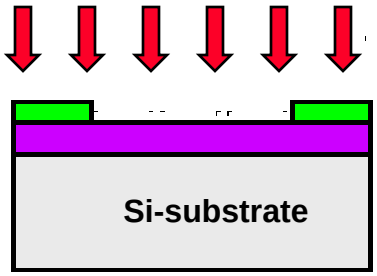
Silicon base material



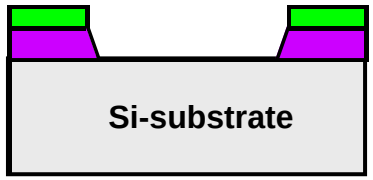
1&2. After oxidation and deposition of negative photoresist



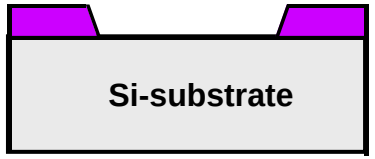
3. Stepper exposure



4. After development and etching of resist, chemical or plasma etch of SiO_2



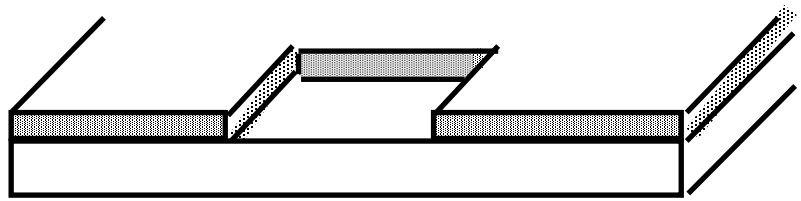
5. After etching



8. Final result after removal of resist

Diffusion and Ion Implantation

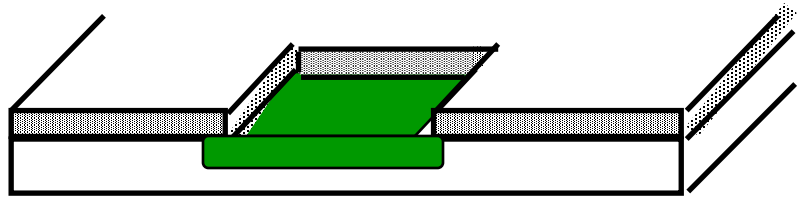
1. Area to be doped is exposed (photolithography)



2. Diffusion

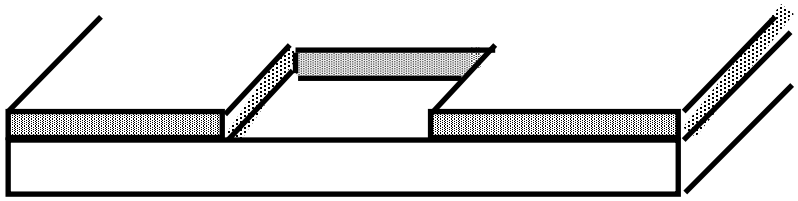
   or

   Ion implantation

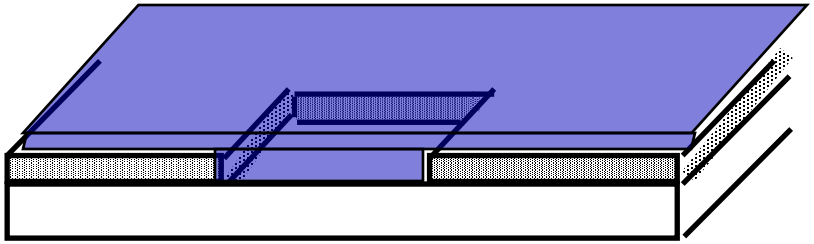


Deposition and Etching

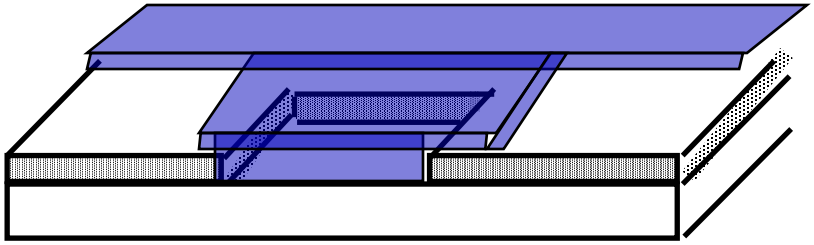
1. Pattern masking (photolithography)



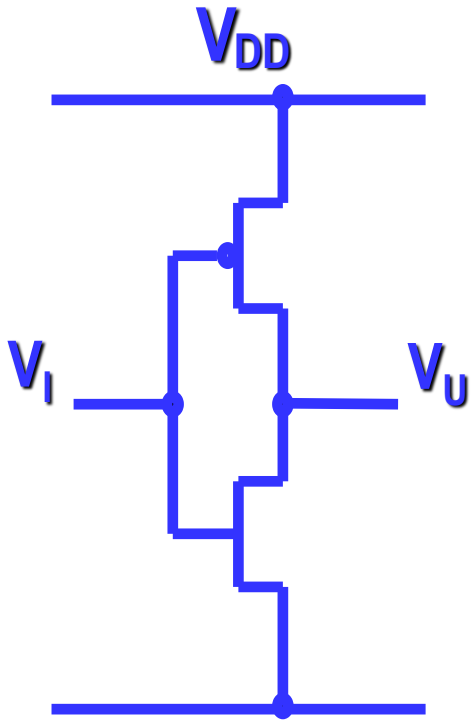
2. Deposit material over entire wafer
   - CVD (Si_3N_4)
   - chemical deposition (polysilicon)
   - sputtering (Al)



3. Etch away unwanted material
   - wet etching
   - dry (plasma) etching

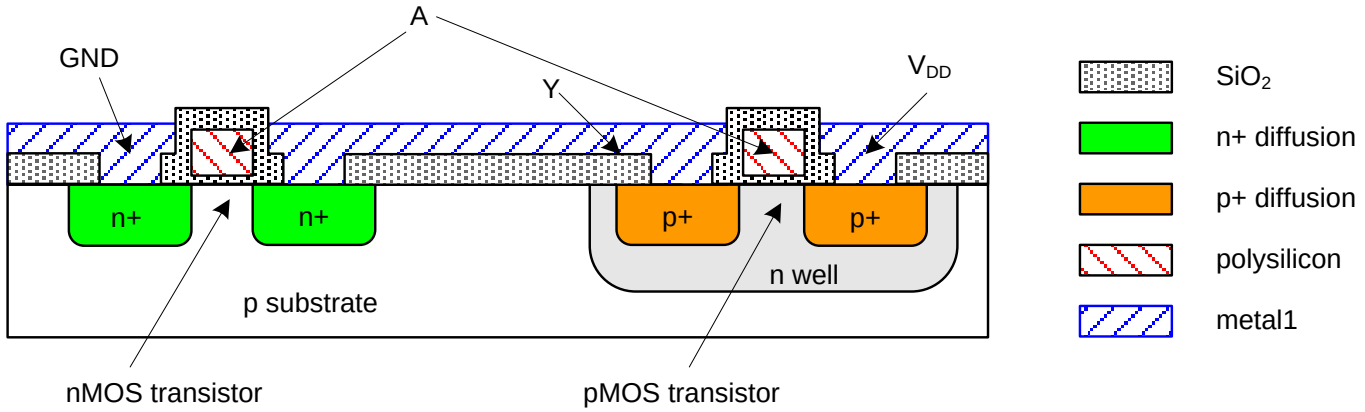


Inverter fabrication



Inverter Cross-section

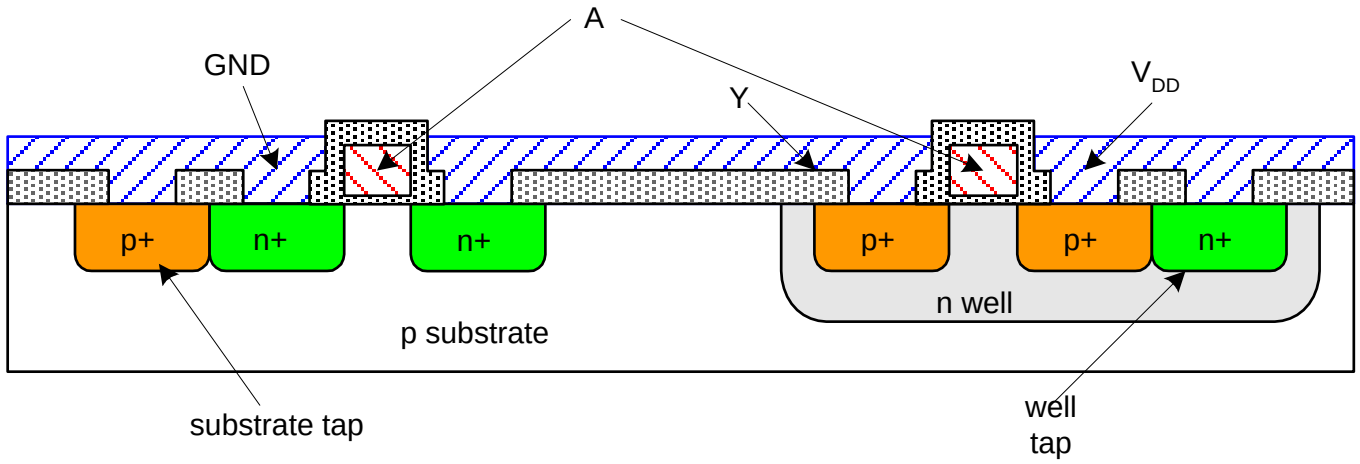
- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors
  - So pMOS p-type source/drain doesn't short to p-type substrate



Courtesy of ARM

Well and Substrate Taps

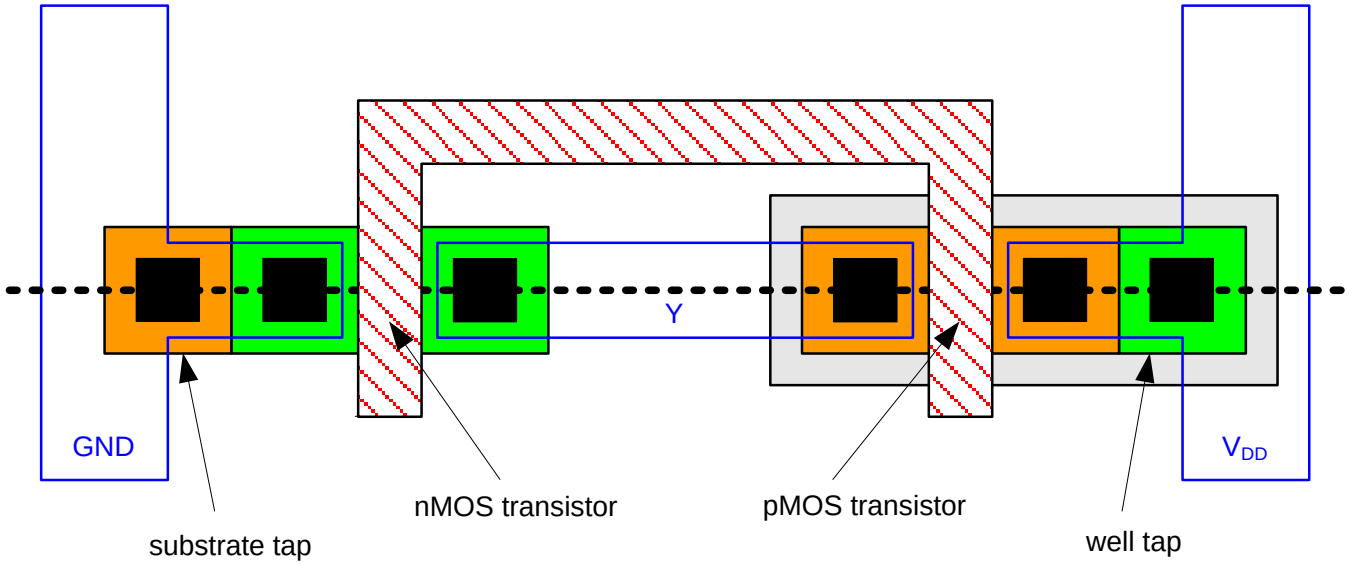
- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly doped semiconductor forms poor connection called Schottky Diode
- Use heavily doped well and substrate contacts/taps



Courtesy of ARM

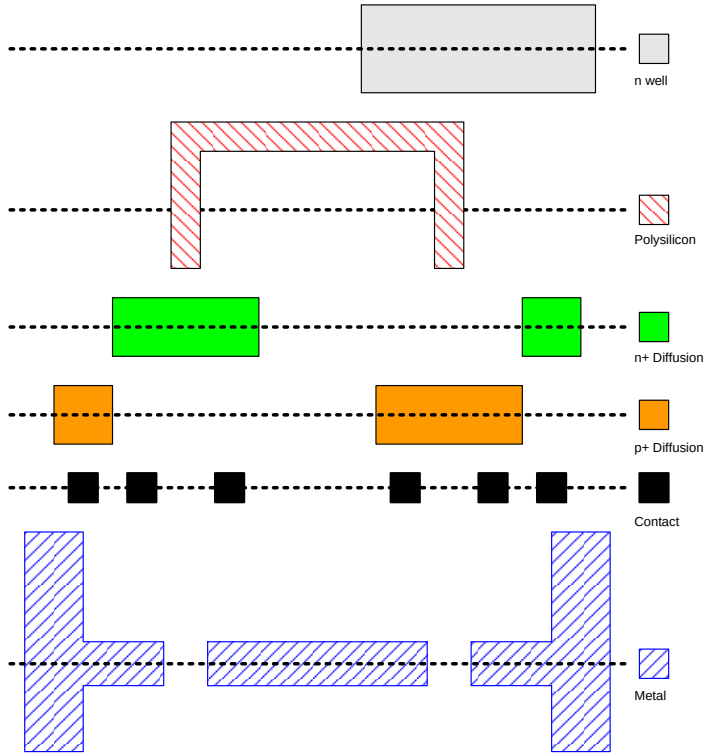
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



Courtesy of ARM

Fabrication

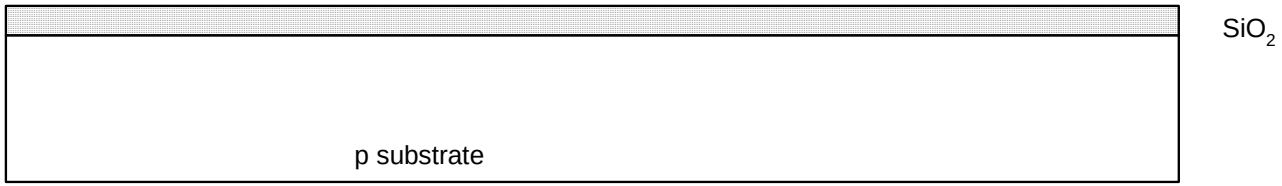
- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields, costing billions of dollars

Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

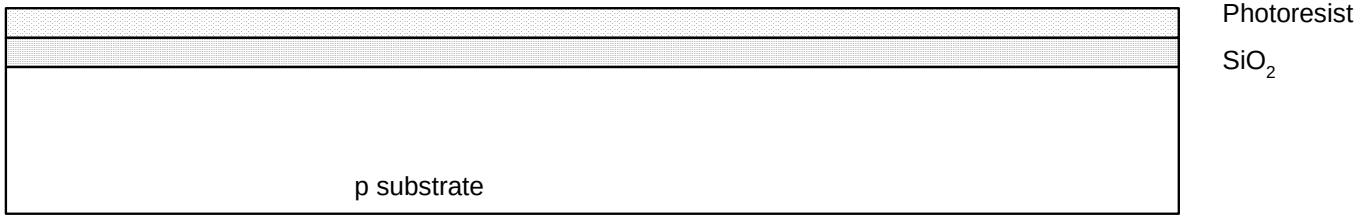
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 °C with H_2O or O_2 in oxidation furnace



Photoresist

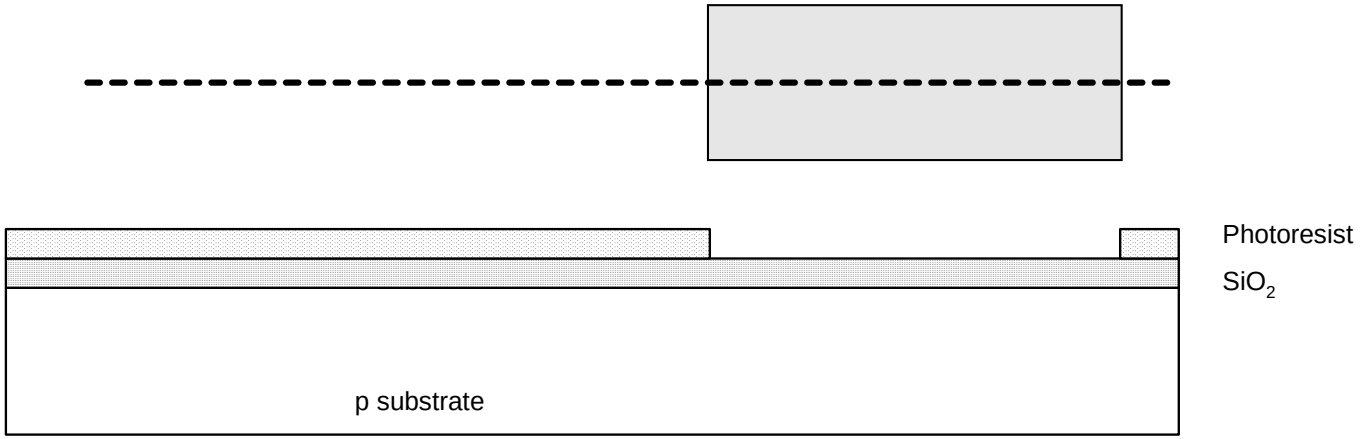
- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



Courtesy of ARM

Lithography

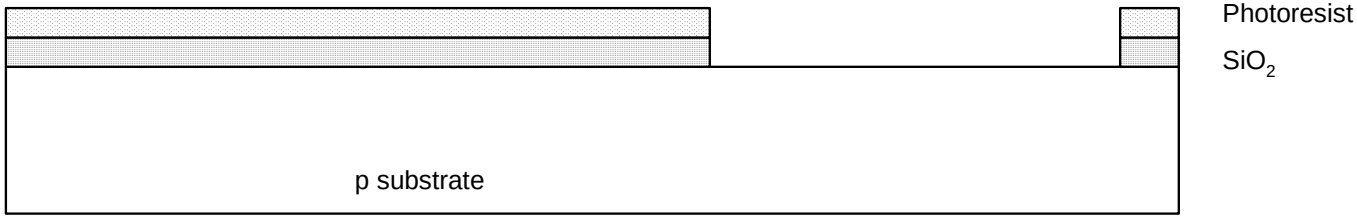
- Expose photoresist through n-well mask
- Strip off exposed photoresist



Courtesy of ARM

Etch

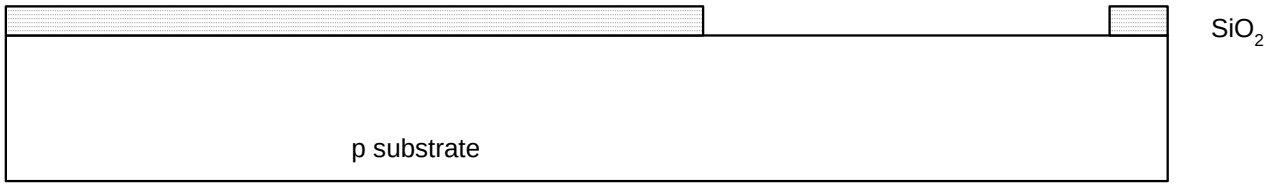
- Etch oxide with hydrofluoric acid (HF)
- Only attacks oxide where resist has been exposed



Courtesy of ARM

Strip Photoresist

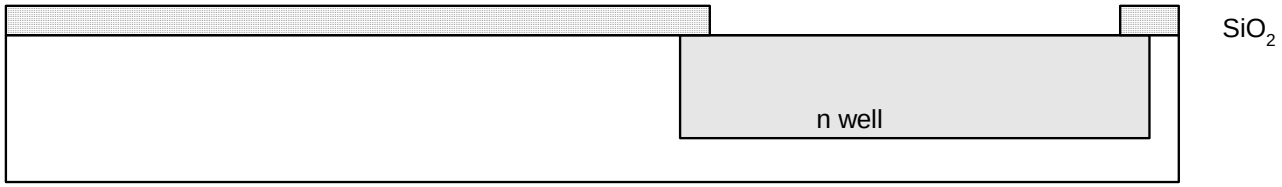
- Strip off remaining photoresist
  - Use a mixture of acids called piranha etch
- Resist doesn't melt in the next step



Courtesy of ARM

n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with a beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si



Courtesy of ARM

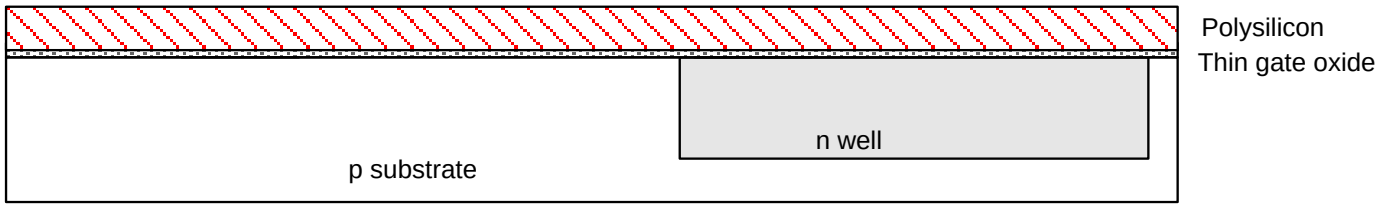
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

Courtesy of ARM

Polysilicon

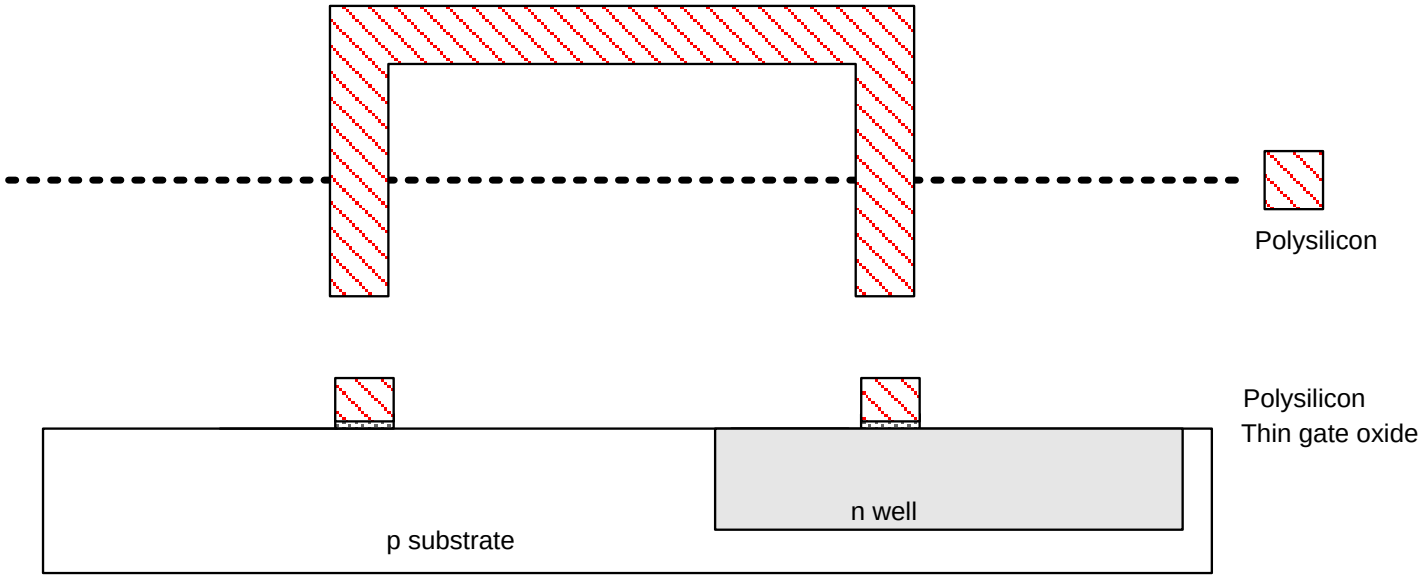
- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



Courtesy of ARM

Polysilicon Patterning

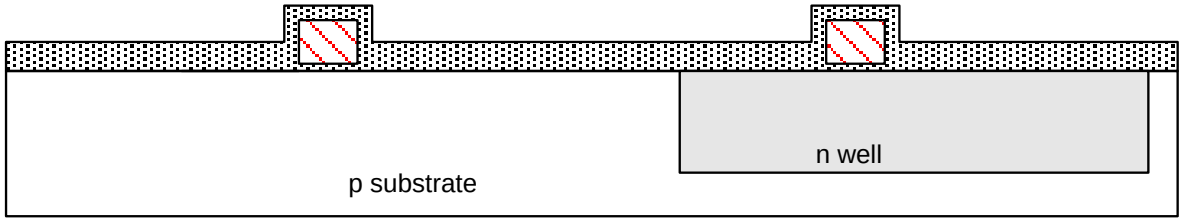
- Use the same lithography process to pattern polysilicon



Courtesy of ARM

Self-Aligned Process

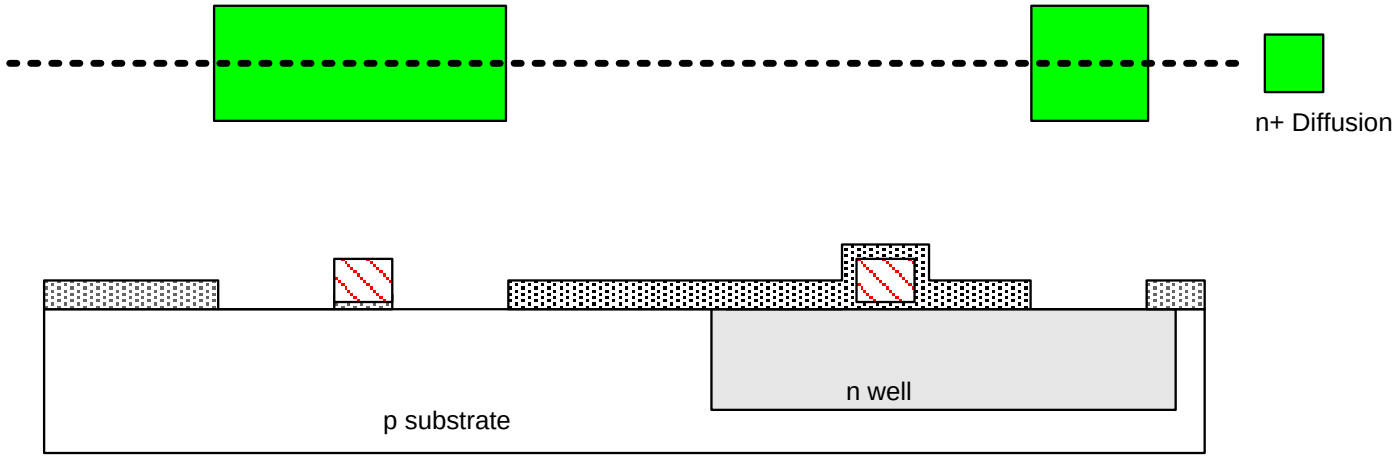
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



Courtesy of ARM

N-diffusion

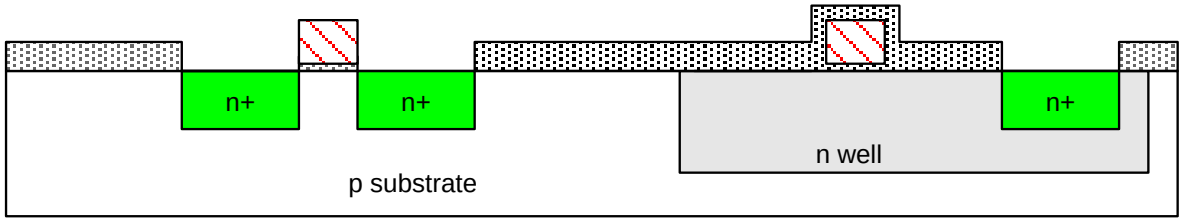
- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



Courtesy of ARM

N-diffusion cont.

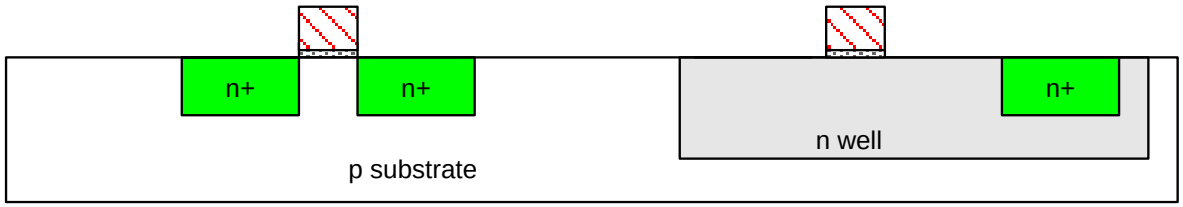
- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



Courtesy of ARM

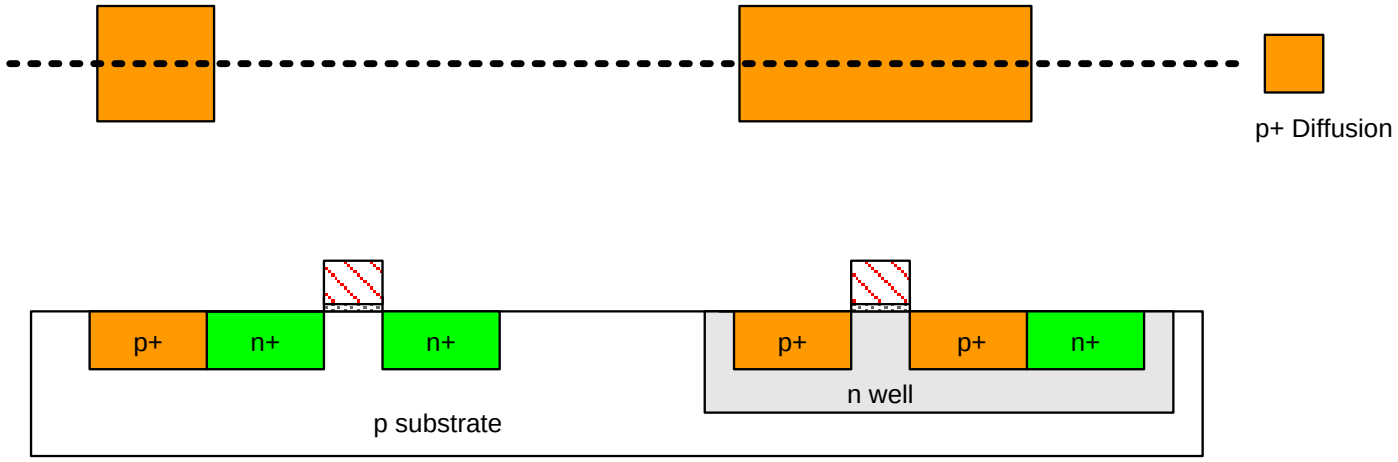
N-diffusion cont.

- Strip off oxide to complete patterning step



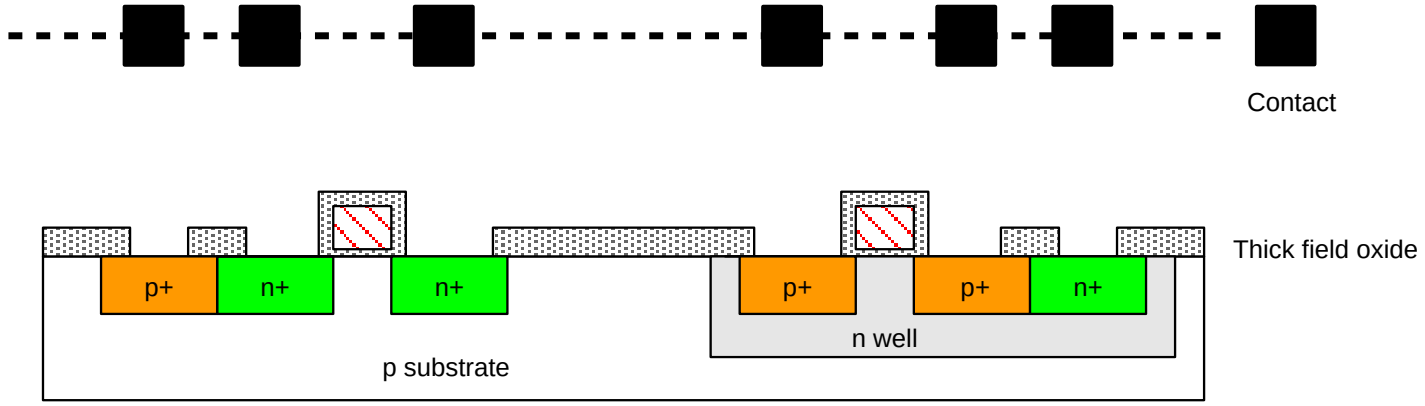
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



Contacts

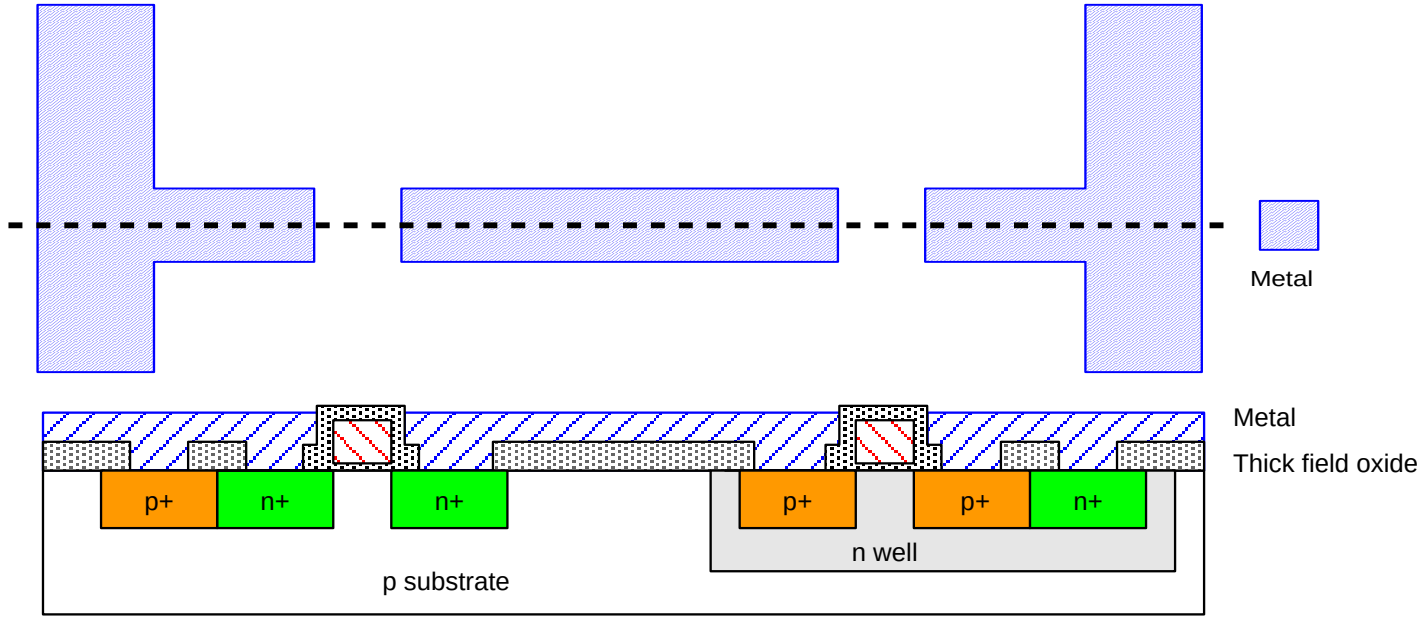
- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Courtesy of ARM

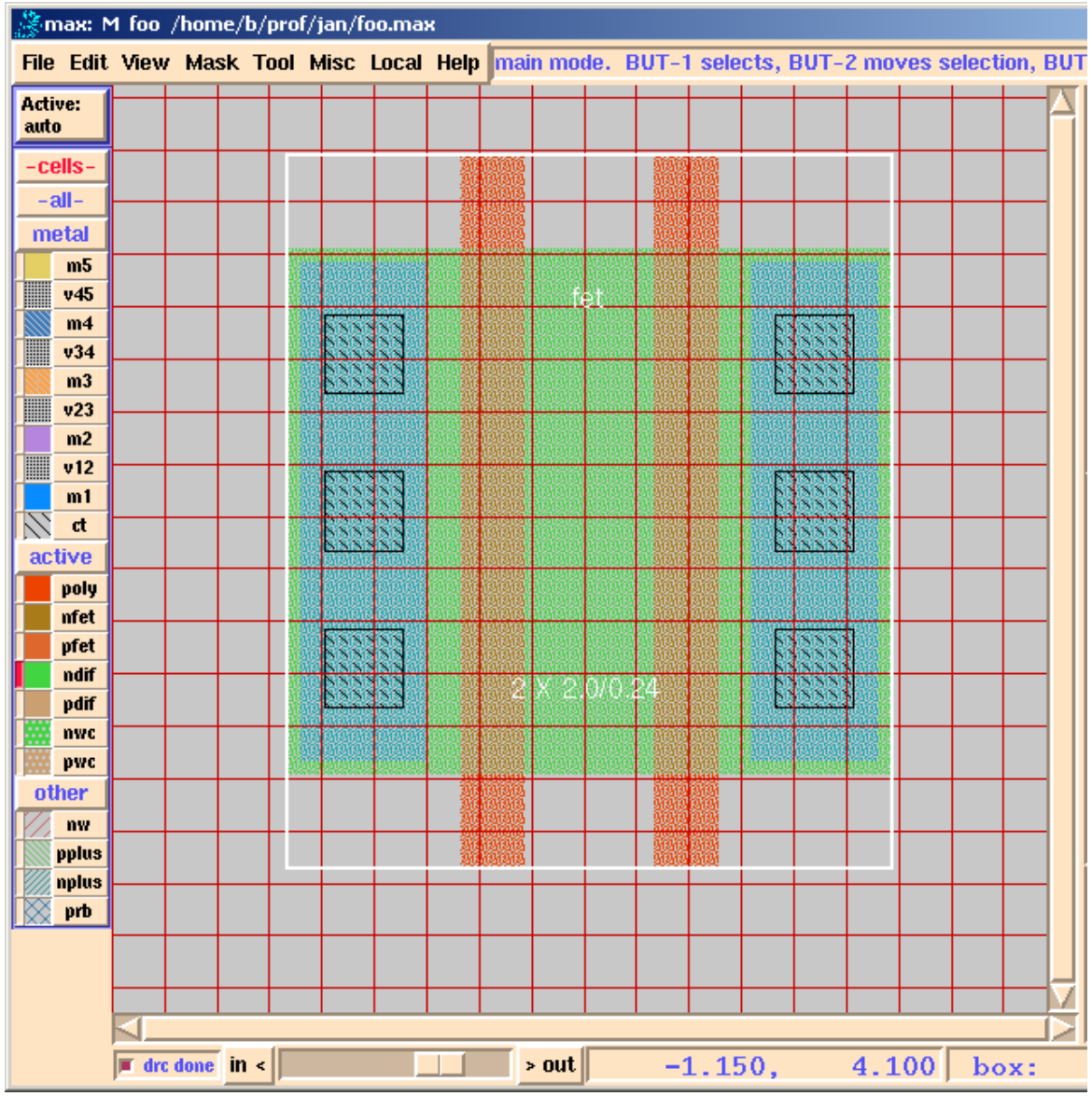
Metallization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

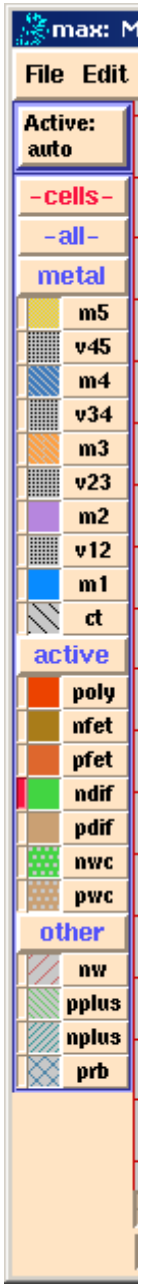


Courtesy of ARM

Layout Editor: *max* Design Frame

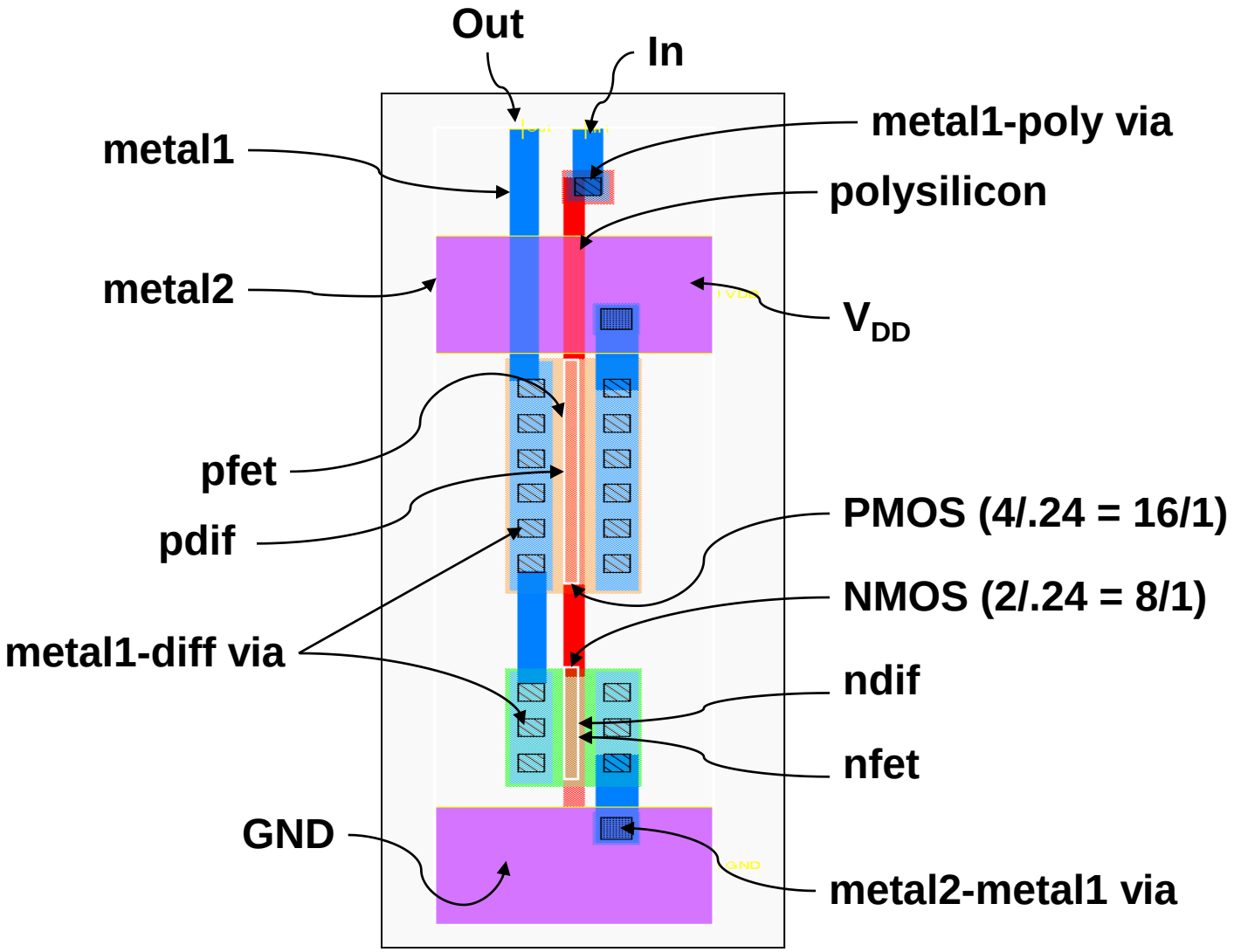


max Layer Representation



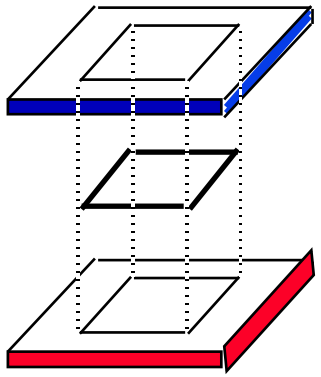
- Metals (five) and vias/contacts between the interconnect levels
  - Note that m5 connects only to m4, m4 only to m3, etc., and m1 only to poly, ndif, and pdif
  - Some technologies support “stacked vias”
- Active – active areas on/in substrate (poly gates, transistor channels (nfet, pfet), source and drain diffusions (ndif, pdif), and well contacts (nwc, pwc))
- Wells (nw) and other select areas (pplus, nplus, prb)

CMOS Inverter *max* Layout



Simplified Layouts in *max*

- Online design rule checking (DRC)
- Automatic fet generation (just overlap poly and diffusion and it creates a transistor)
- Simplified via/contact generation
  - v12, v23, v34, v45
  - ct, nwc, pwc

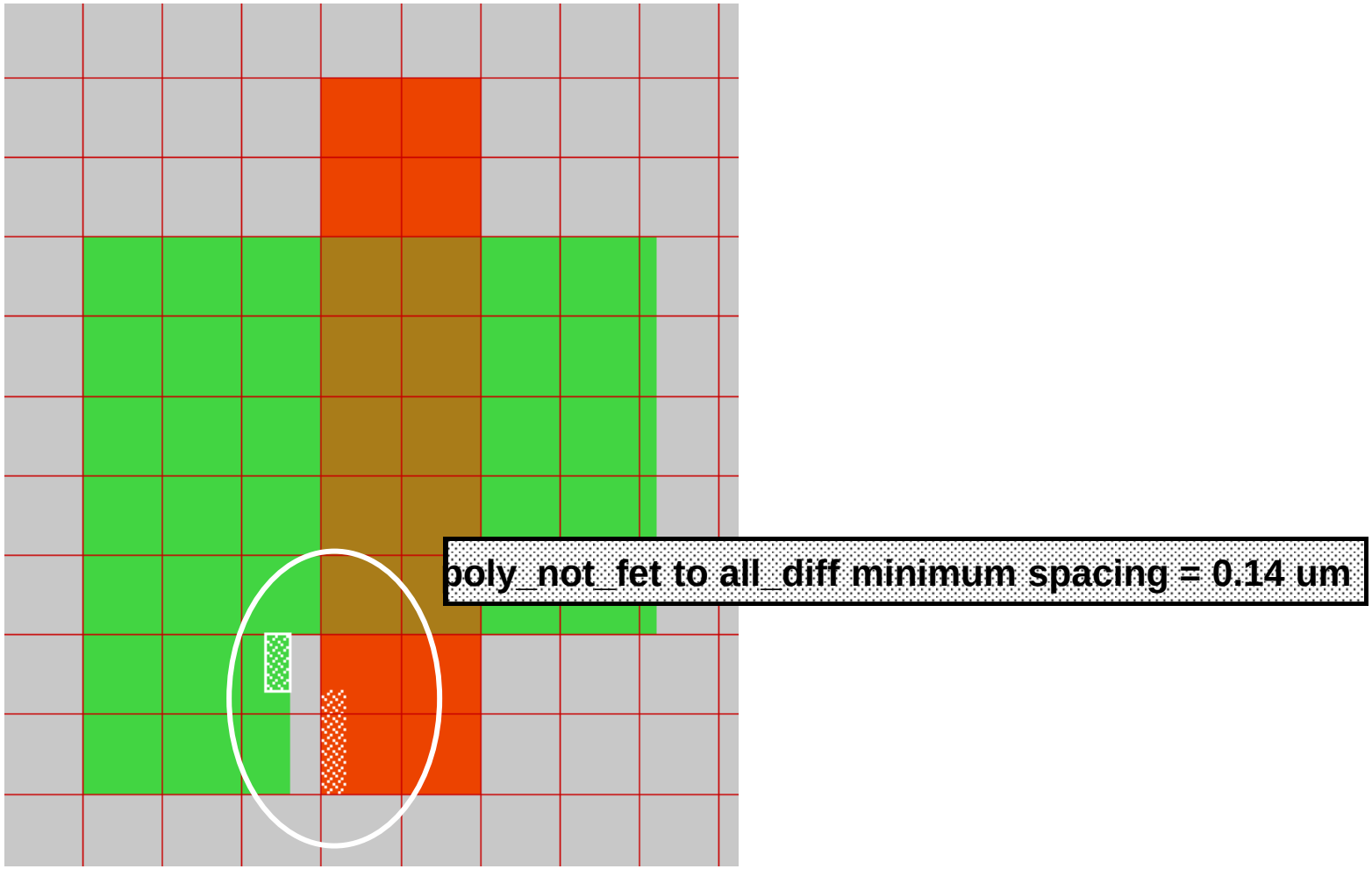


0.44 x 0.44 m1

0.3 x 0.3 ct

0.44 x 0.44 poly

Design Rule Checker



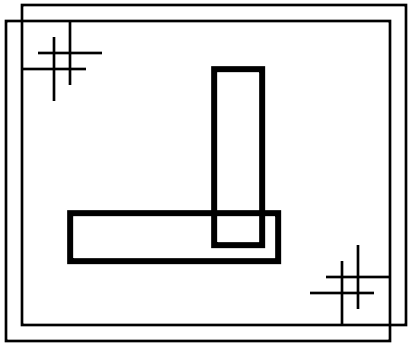
Design Rules

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

Why Have Design Rules?

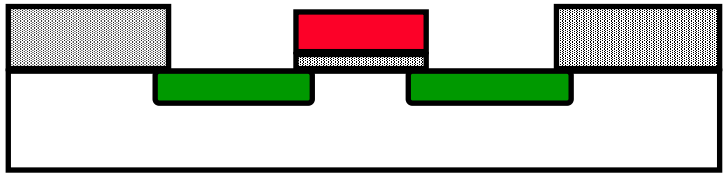
- To be able to tolerate some level of fabrication errors such as

1. Mask misalignment



2. Dust

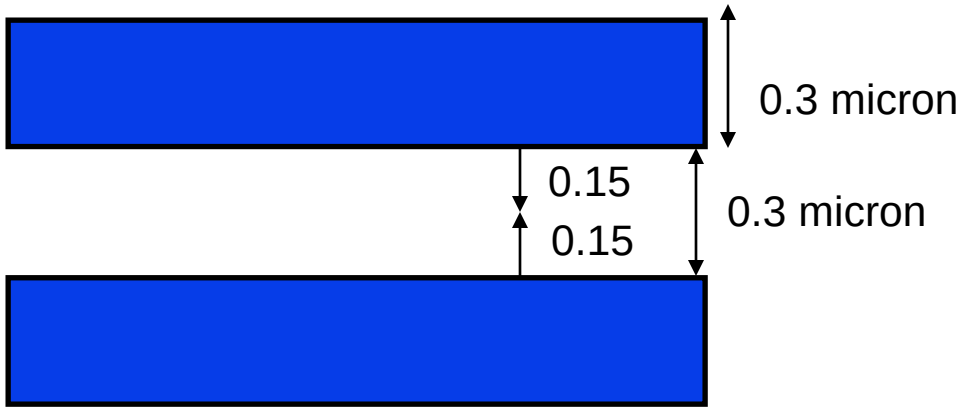
3. Process parameters (e.g., lateral diffusion)



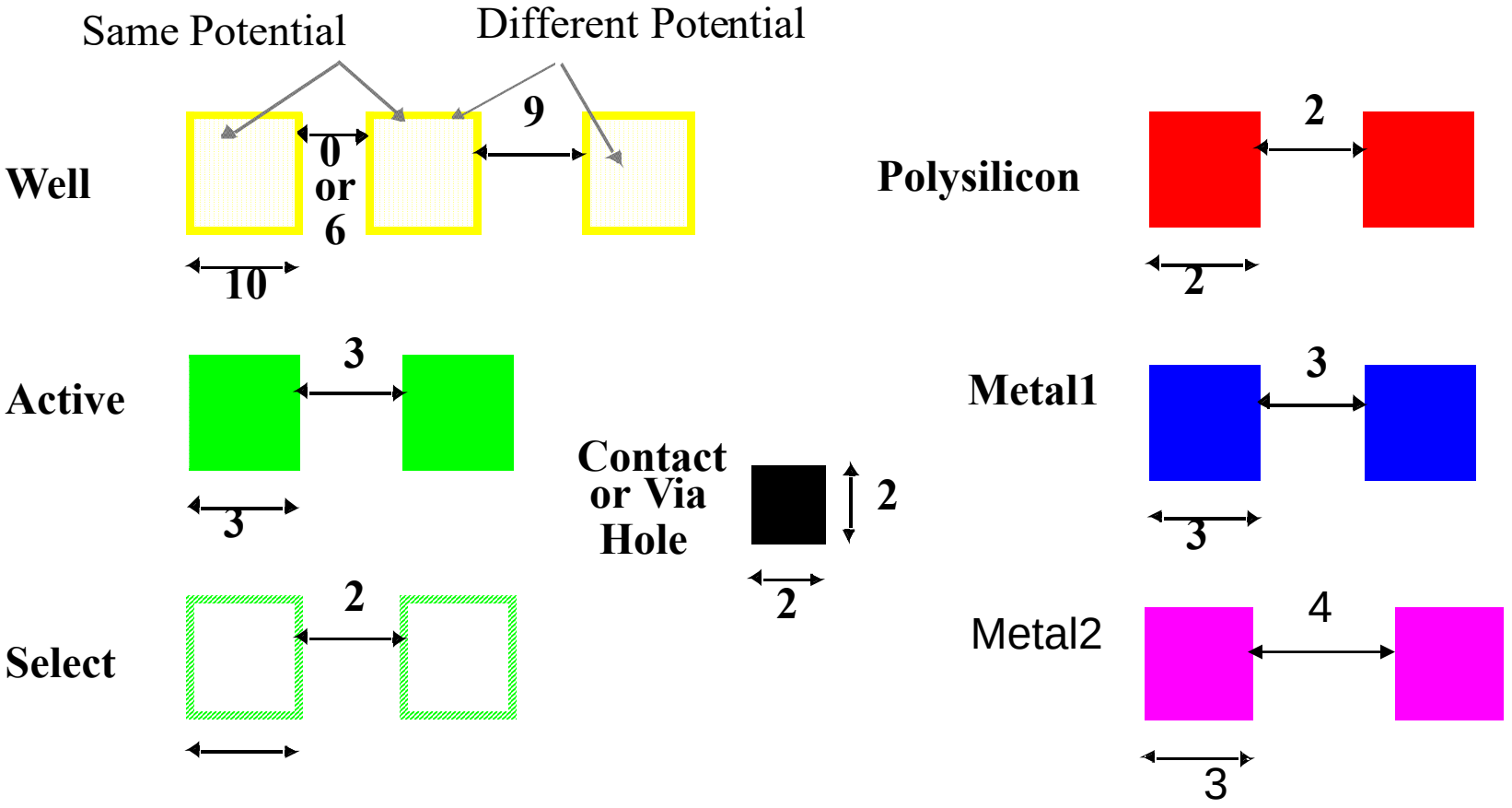
4. Rough surfaces

Intra-Layer Design Rule Origins

- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab



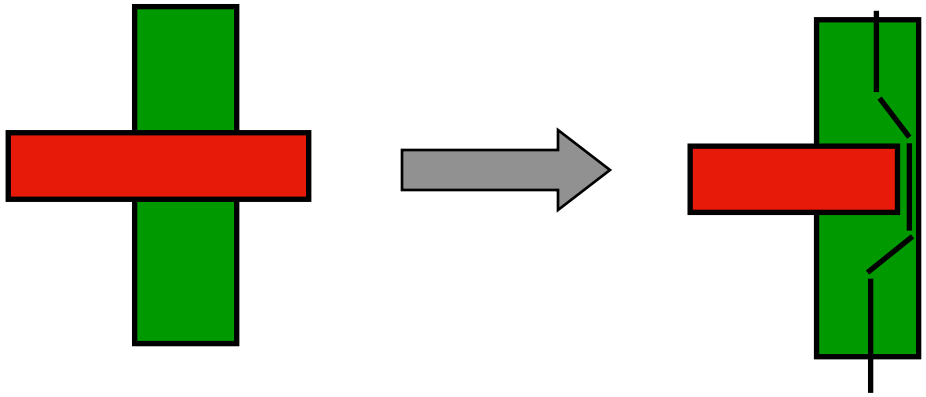
Intra-Layer Design Rules



Inter-Layer Design Rule Origins

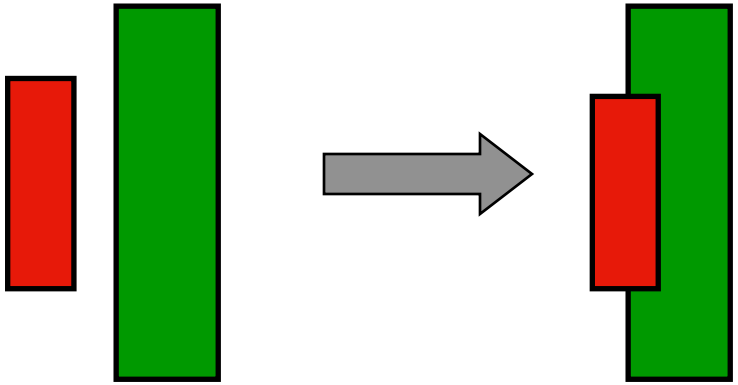
1. Transistor rules – transistor formed by overlap of active and poly layers

Transistors



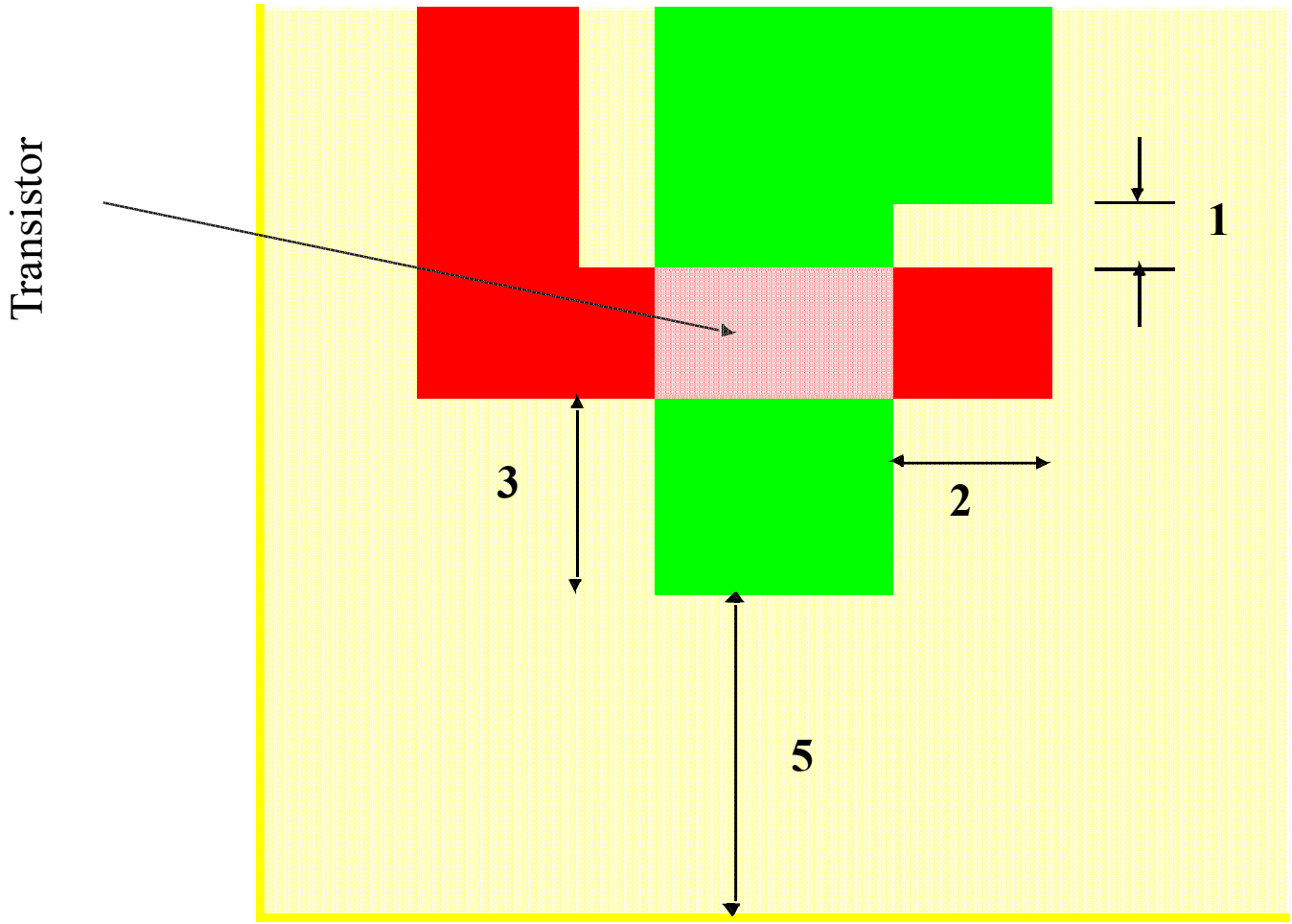
Catastrophic error

Unrelated Poly & Diffusion

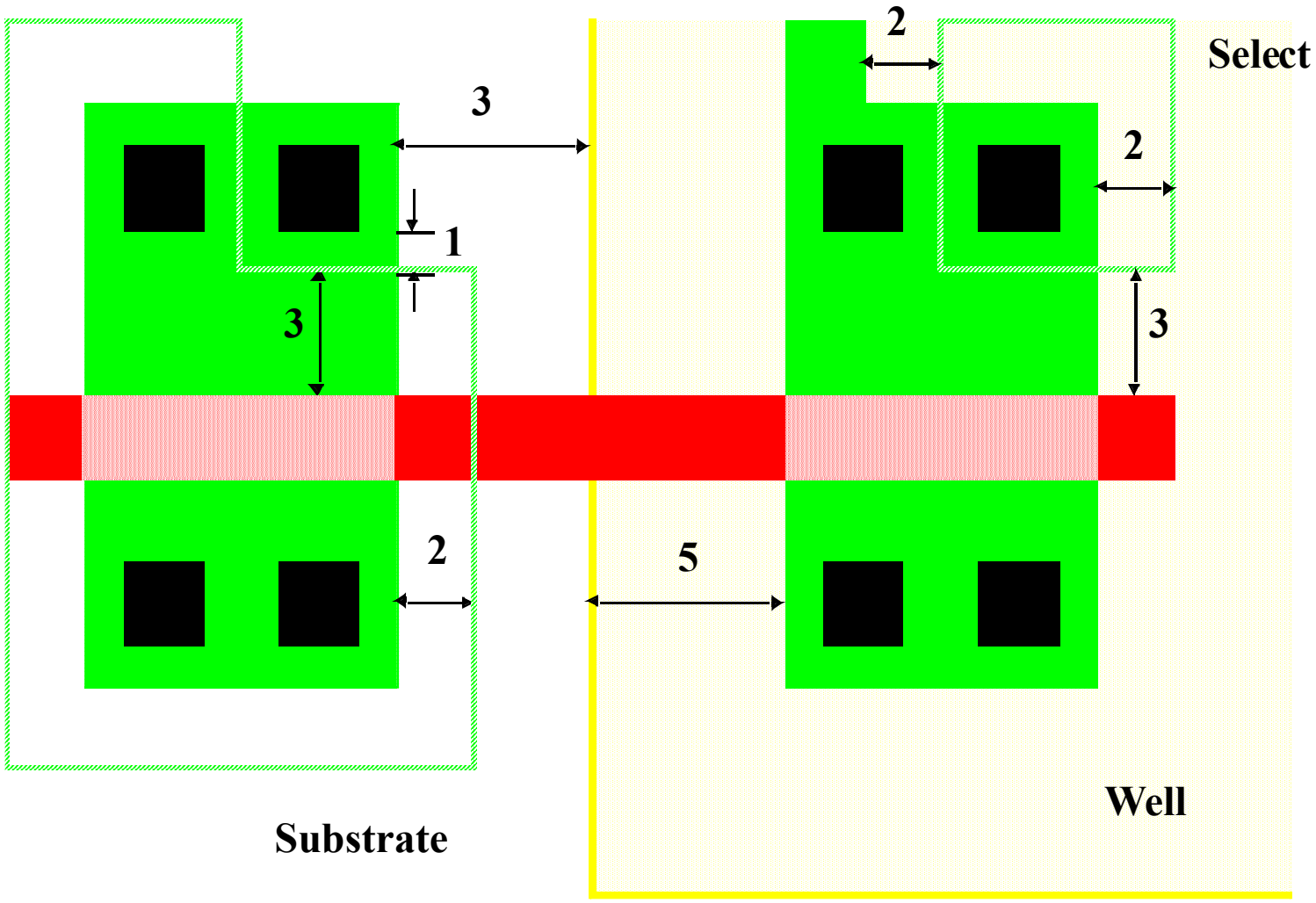


Thinner diffusion, but still working

Transistor Layout



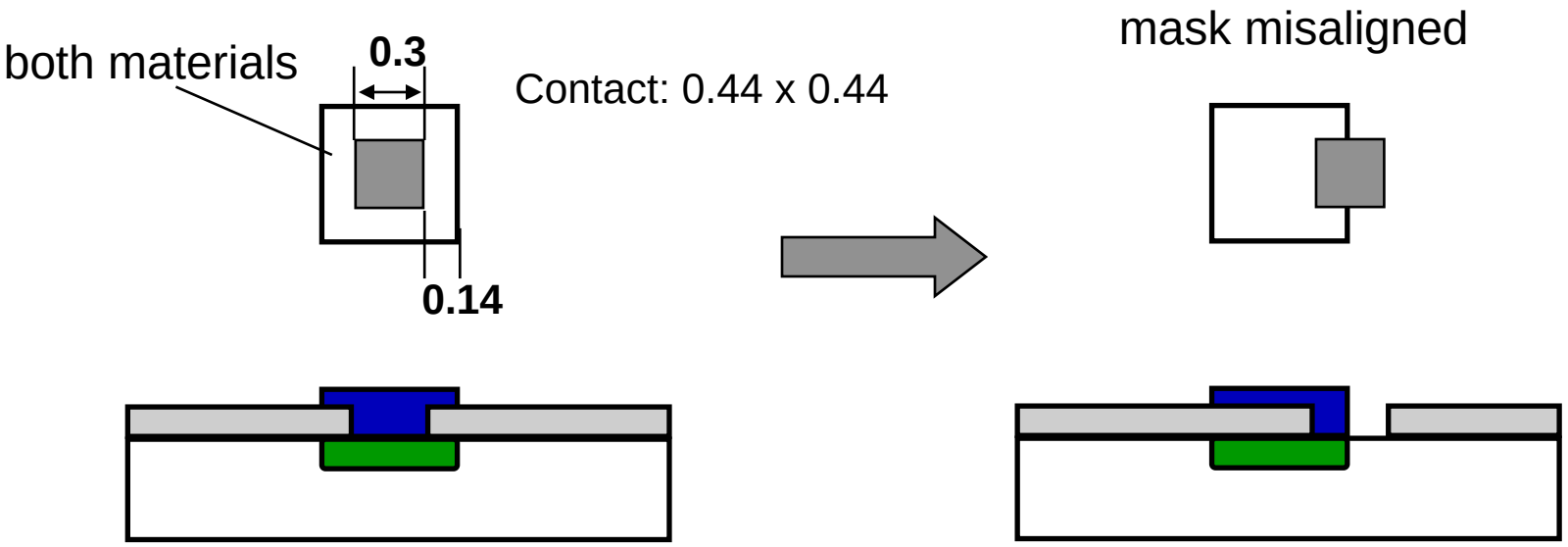
Select Layer



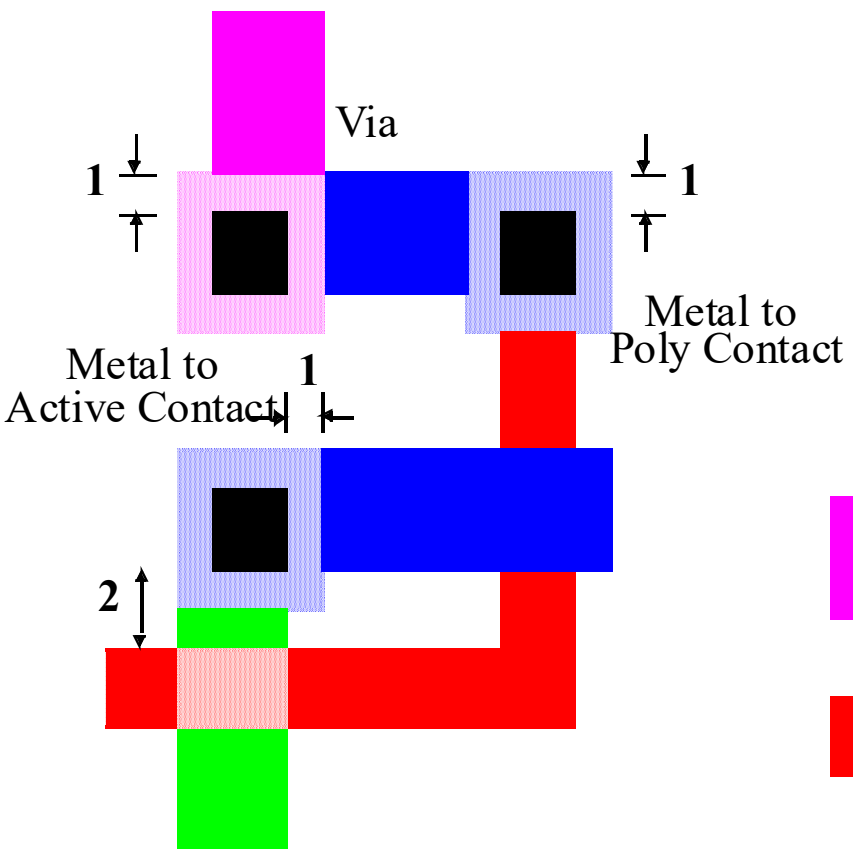
Inter-Layer Design Rule Origins, Con't

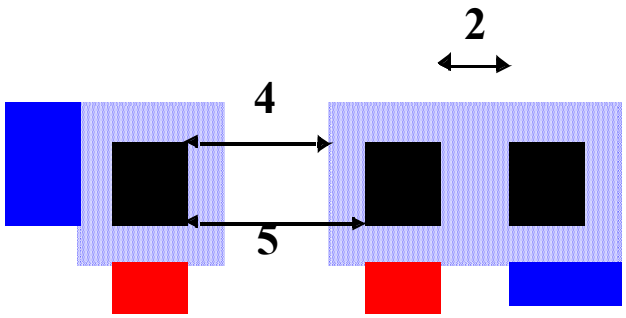
2. Contact and via rules

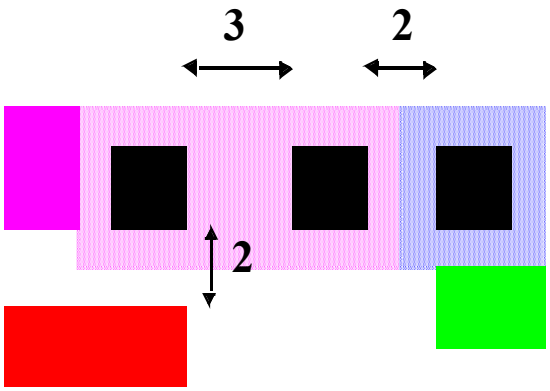
M1 contact to p-diffusion M1 contact to n-diffusion M1 contact to poly	Contact Mask
Mx contact to My	Via Masks



Vias and Contacts







End, Questions ?

- MOS Transistor Switch Model
- Pass Gate
- Inverter
- Review of IC Manufacturing