Electronic Systems

ZyBo Development Board
Xilinx VIVADO

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Agenda

1) ZyBo Development Board
2) Zynq 7000 APSoC
3) DDFS Implementation on ZyBo
4) Xilinx VIVADO Design Suite
5) Vivado Design Flow

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1) ZyBo Development Board
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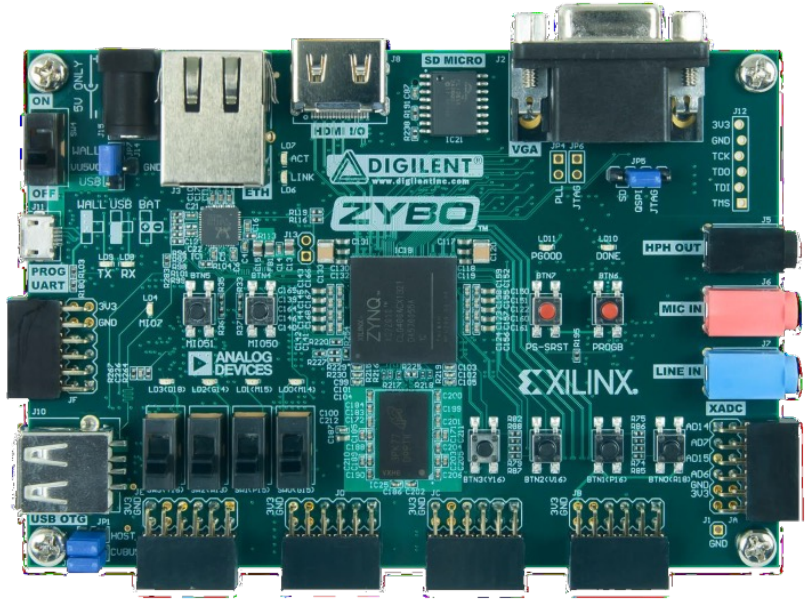
ZyBo Development Board

The ZYBO (ZYnq BOard) is a feature-rich, ready-to-use, entry-level embedded software and digital circuit development platform built around the smallest member of the Xilinx Zynq-7000 family, the Z-7010.

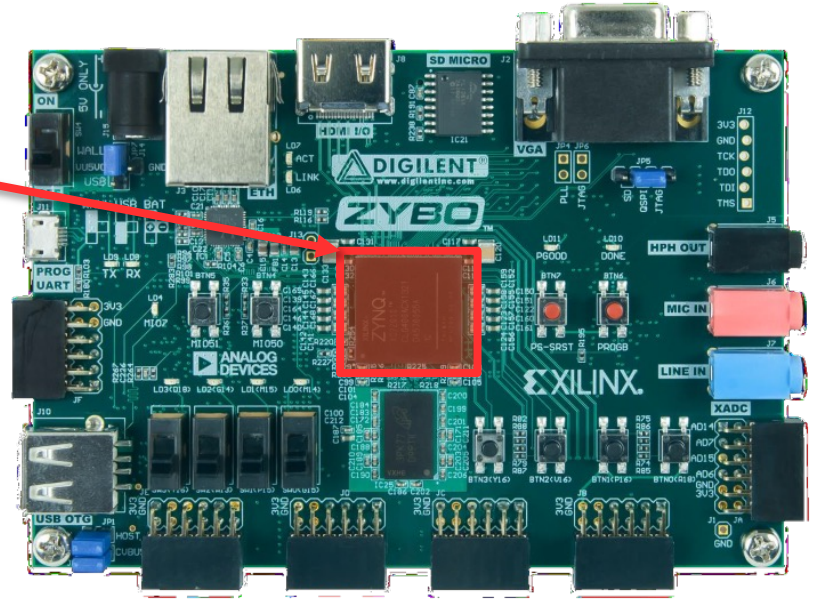
The Z-7010 is based on the Xilinx All Programmable System-on-Chip (AP SoC) architecture, which tightly integrates a dual-core ARM Cortex-A9 processor with Xilinx 7-series Field Programmable Gate Array (FPGA) logic.



ZyBo Development Board

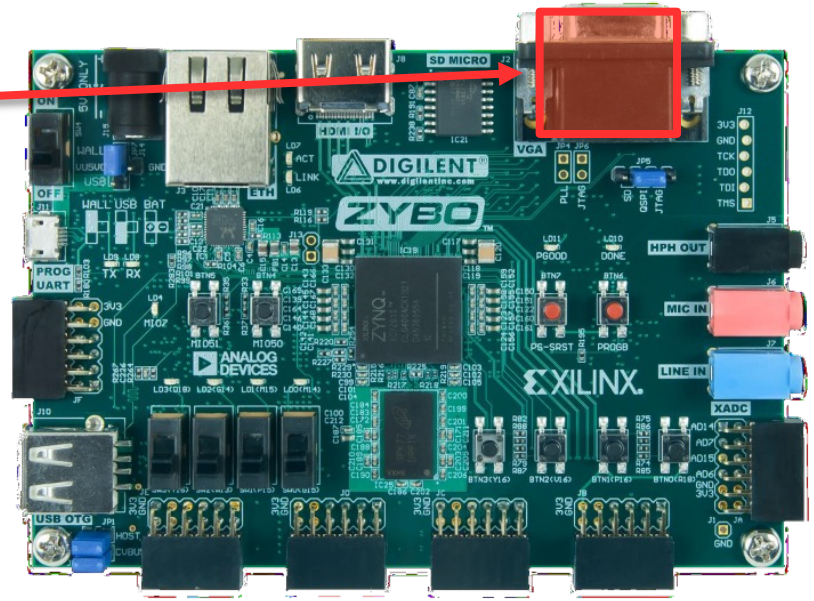
- ZYNQ XC7Z010-1CLG400C
- Others: ZyBo datasheet

  https://www.xilinx.com/support/documentation/university/XUP%20Boards/XUPZYBO/documentation/ZYBO_RM_B_V6.pdf



ZyBo Development Board

- ZYNQ XC7Z010-1CLG400C
- 16-bits VGA port



ZyBo Development Board

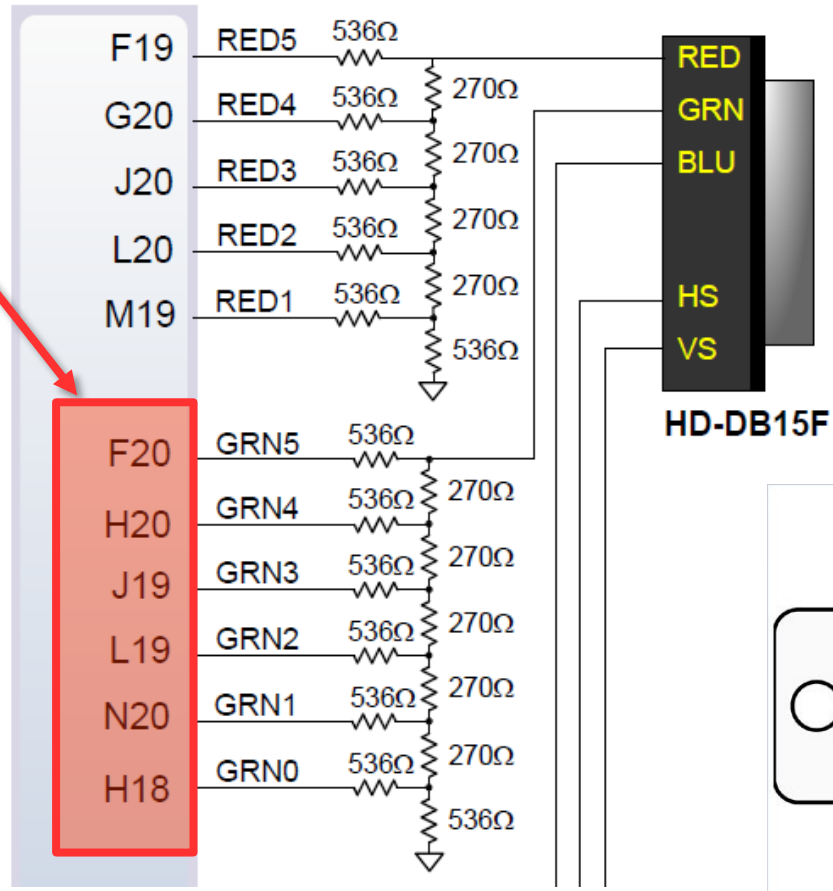
The VGA Port:

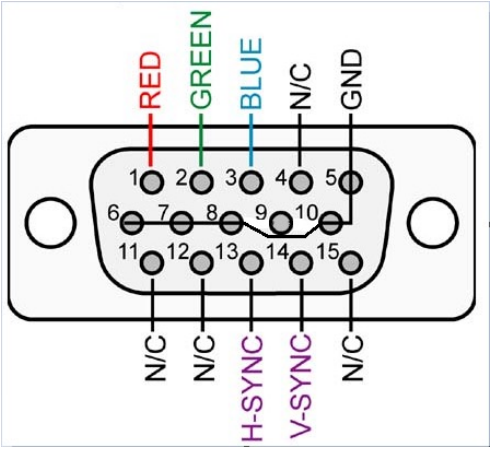
- 6 bits DAC on GRN channel
- R-2R ladder soldered on board

ZYNQ I/O pin VIO = 3.3 V

If GRN[5:0] = “111111”

$V_{DAC}(63) \approx 3.2\ V$

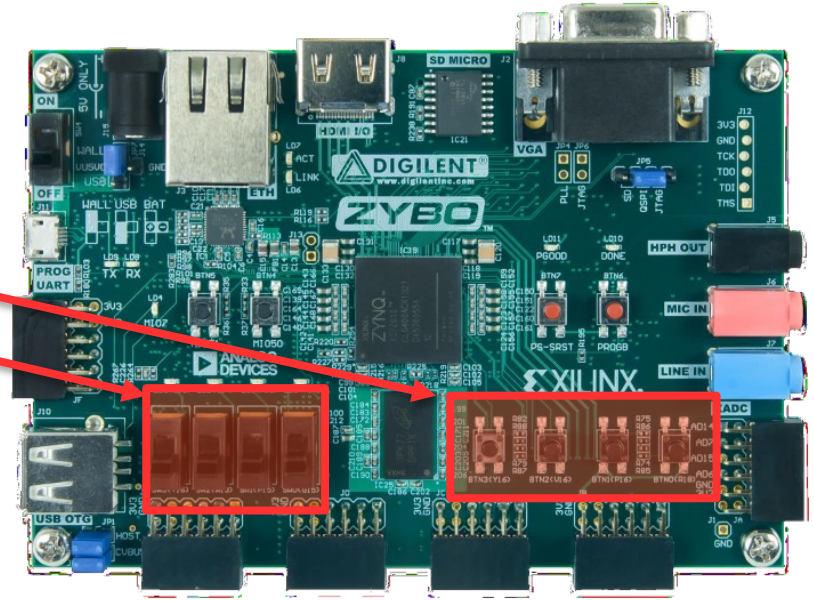




Bottom view!

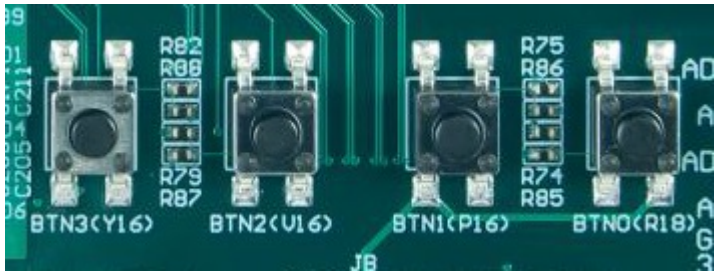
ZyBo Development Board

- ZYNQ XC7Z010-1CLG400C
- 16-bits VGA port
- GPIO:
  - 4 pushbuttons
  - 4 slide switches
  - 4 LEDs

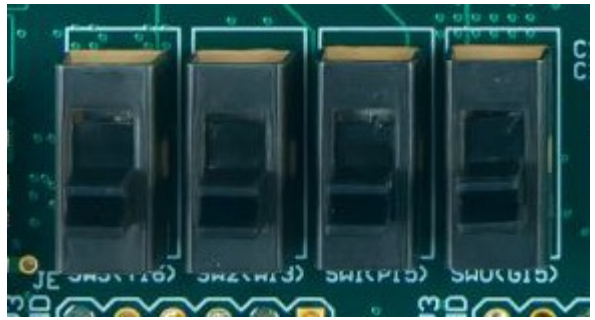


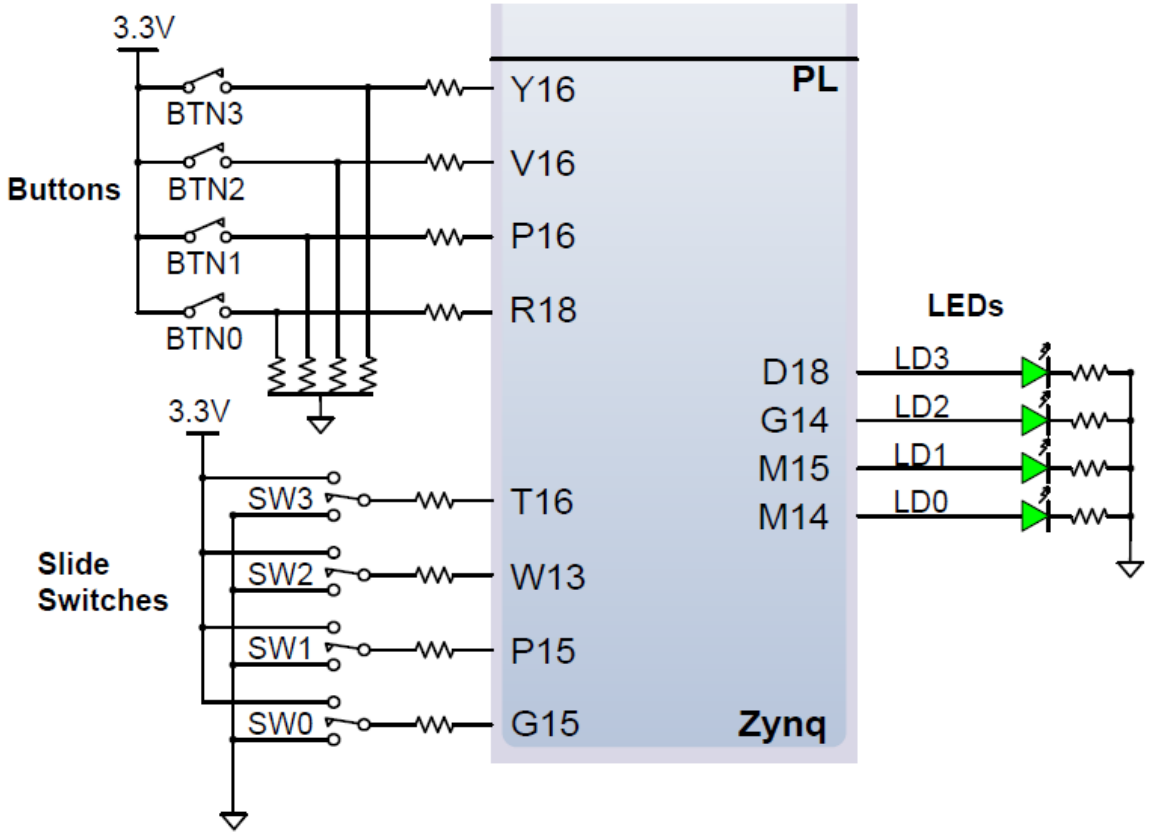
ZyBo Development Board

Push Buttons



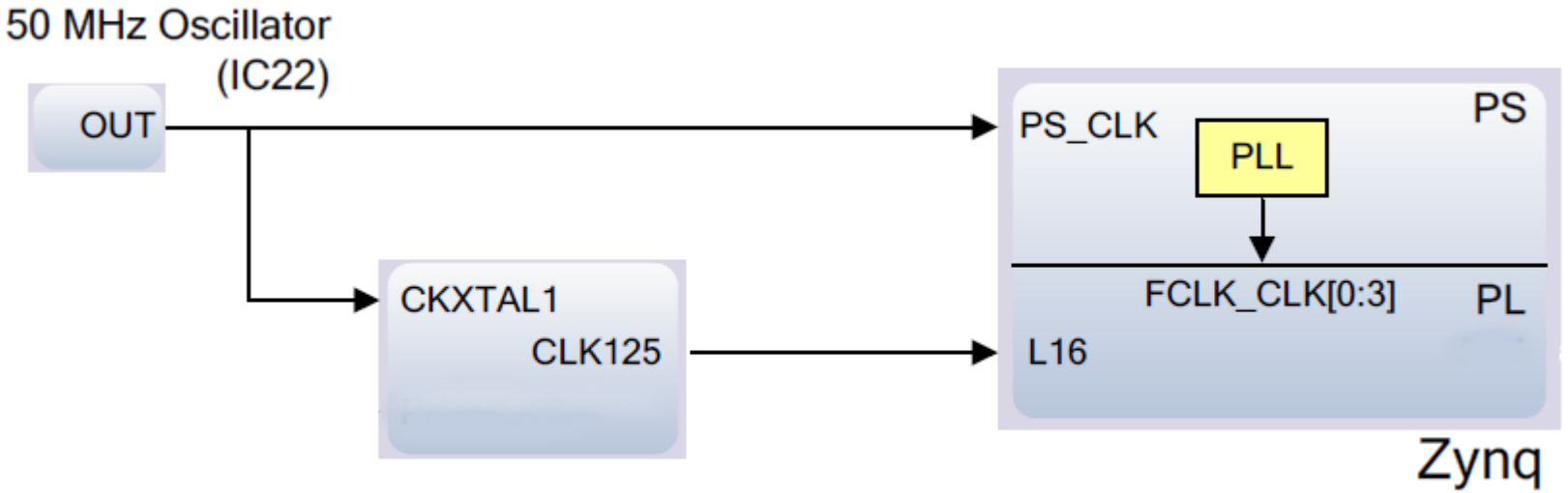
Switches





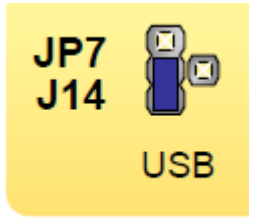
ZyBo Development Board

- The ZyBo provides a **125 MHz clock** to the PL (Programmable Logic) on L16 pin.

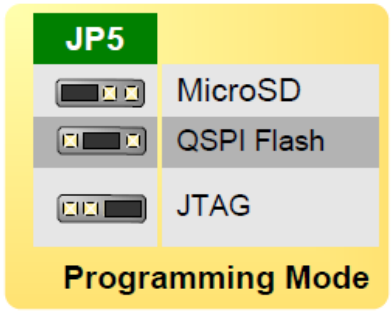


ZyBo Development Board

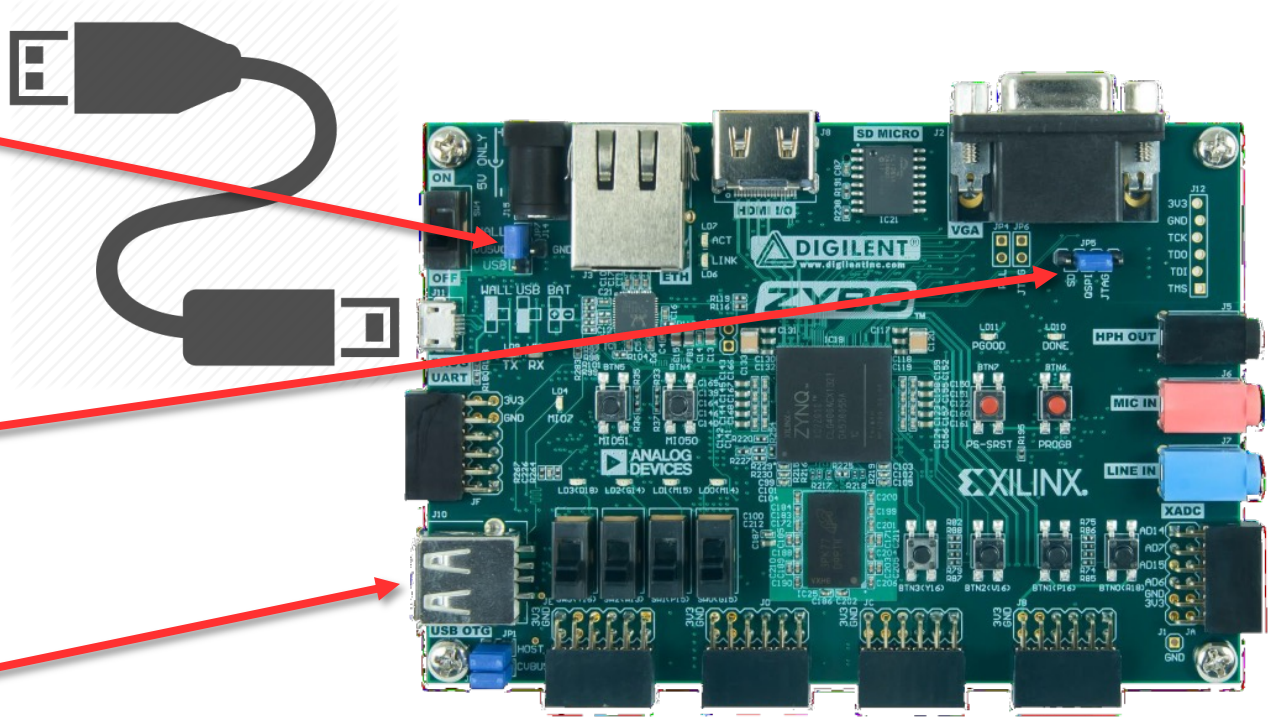
Supply by USB



Programming Mode QSPI



USB: host



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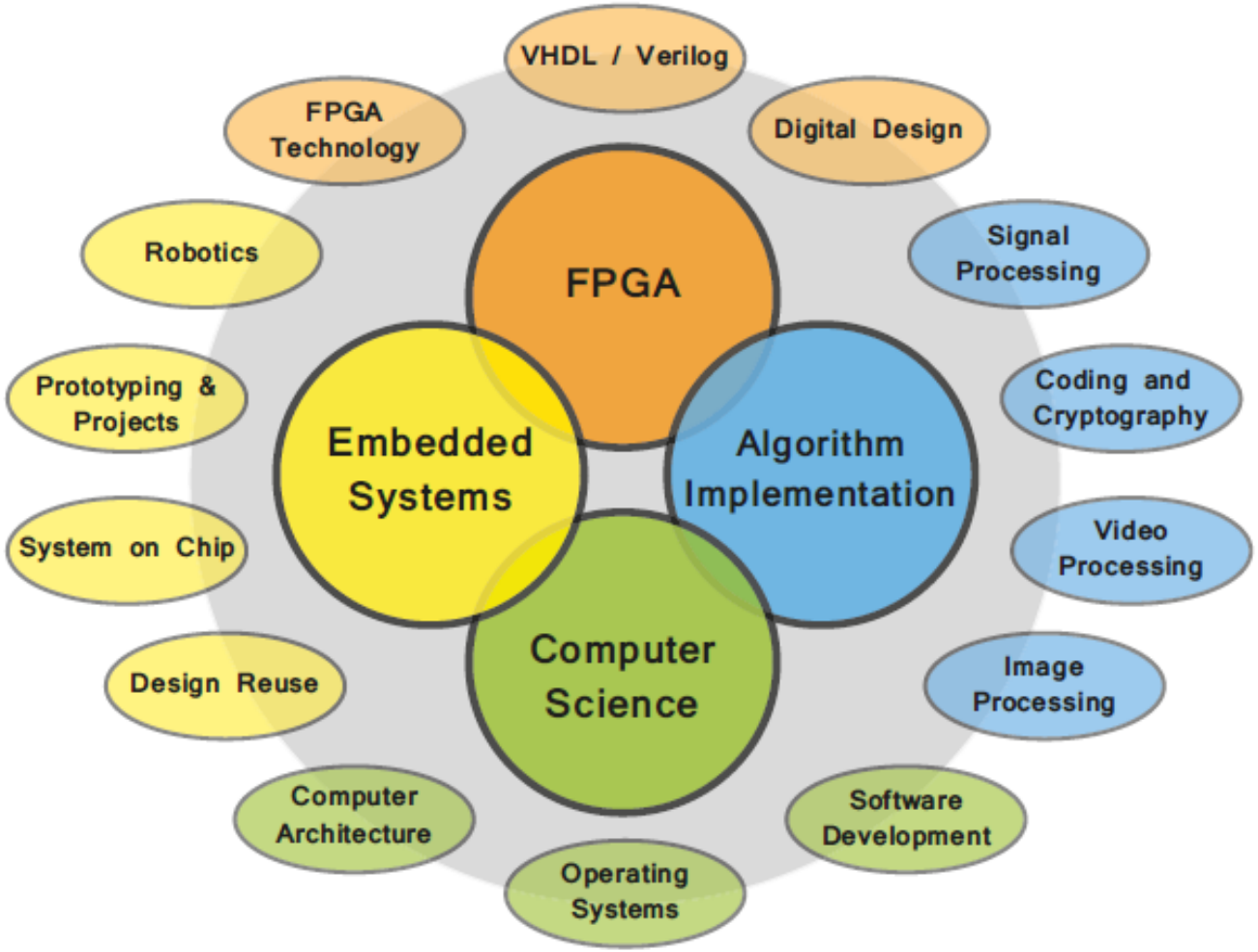
Zynq 7000 APSoC

Microelectronic Scopes:

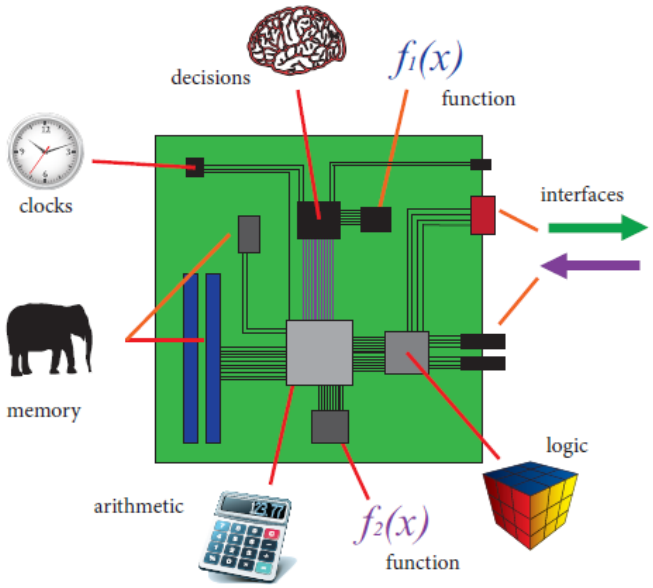
- Medical
- Military and Avionics
- Industrial
- Consumer
- Transport and Mobility
- Telecommunication
- Sensors Interface and IoT

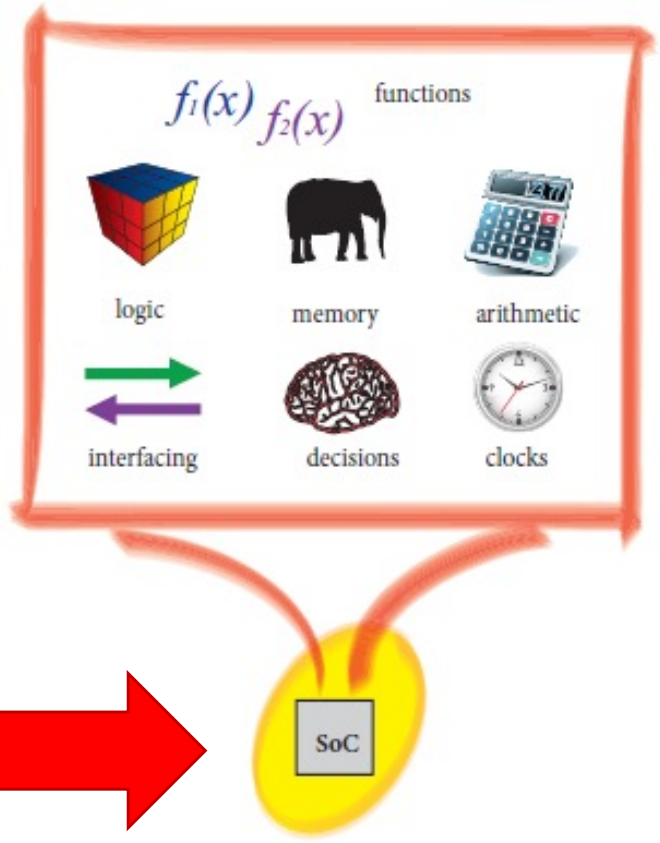


Zynq 7000 APSoC

SoC integrates in a single chip:

- Processor/s
- DSPs
- PLDs
- FPGAs
- Interfaces
- Memories
- IPs





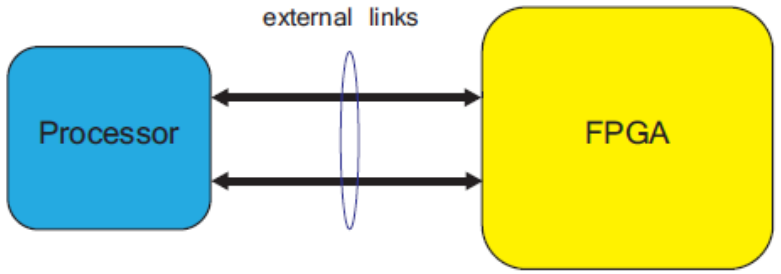
System on Board **System on Chip (SoC)**

Zynq 7000 APSoC

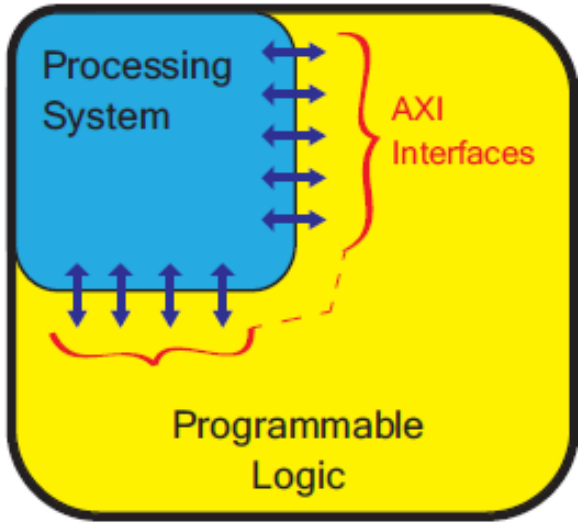
From discrete component to SoC

Xilinx APSoC (All Programmable SoC)

- Single chip as HW/SW design platform
  - PS: Processing System (2x ARM Cortex A-9)
  - PL: Programmable Logic (FPGA 7-series 28nm)

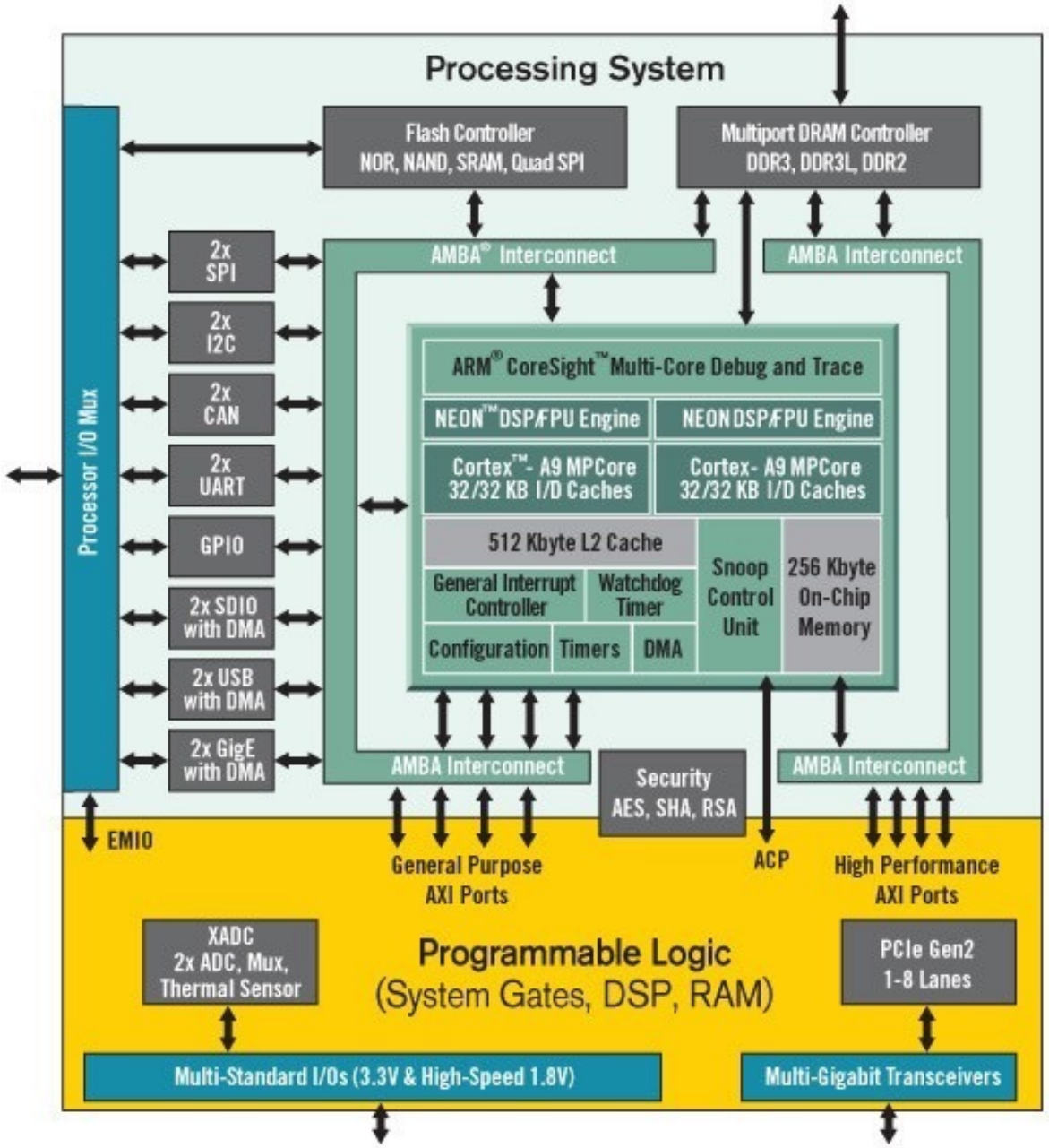


Discrete component Architecture



ZINQ APSoC Architecture

PS

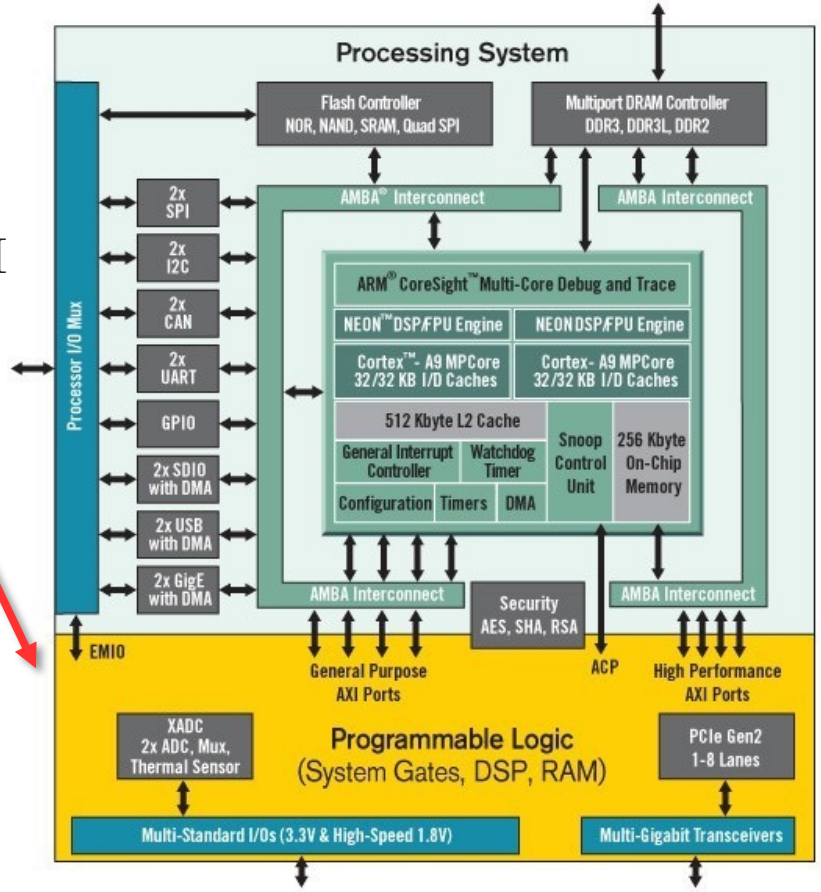

Processing System
Flash Controller
NOR, NAND, SRAM, Quad SPI
Multiport DRAM Controller
DDR3, DDR3L, DDR2
Processor I/O Mux
2x SPI
2x I2C
2x CAN
2x UART
GPIO
2x SDIO with DMA
2x USB with DMA
2x GigE with DMA
AMBA® Interconnect
AMBA Interconnect
ARM® CoreSight™ Multi-Core Debug and Trace
NEON™ DSP/FPU Engine
NEON DSP/FPU Engine
Cortex™- A9 MPCore 32/32 KB I/D Caches
Cortex- A9 MPCore 32/32 KB I/D Caches
512 Kbyte L2 Cache
General Interrupt Controller
Watchdog Timer
Configuration
Timers
DMA
Snoop Control Unit
256 Kbyte On-Chip Memory
AMBA Interconnect
AMBA Interconnect
Security AES, SHA, RSA
EMIO
General Purpose AXI Ports
ACP
High Performance AXI Ports
XADC 2x ADC, Mux, Thermal Sensor
Programmable Logic (System Gates, DSP, RAM)
PCIe Gen2 1-8 Lanes
Multi-Standard I/Os (3.3V & High-Speed 1.8V)
Multi-Gigabit Transceivers

PL

Zynq 7000 APSoC

ZYNQ XC7Z010-1CLG400C

- 650Mhz dual-core Cortex-A9 processor
- DDR3 memory controller with 8 DMA channels
- High-bandwidth peripheral controllers: 1G Eth, USB 2.0, SDI
- Low-bandwidth peripheral controller: SPI, UART, CAN, I2C
- **Reprogrammable logic equivalent to Artix-7 FPGA**
  - 4,400 logic slices, each with four 6-input LUTs and 8 flip-flops
  - 240 KB of fast block RAM
  - Two clock management tiles,
    - each with a phase-locked loop (PLL)
    - and mixed-mode clock manager (MMCM)
  - 80 DSP slices
  - Internal clock speeds exceeding 450MHz
  - On-chip analog-to-digital converter (XADC)

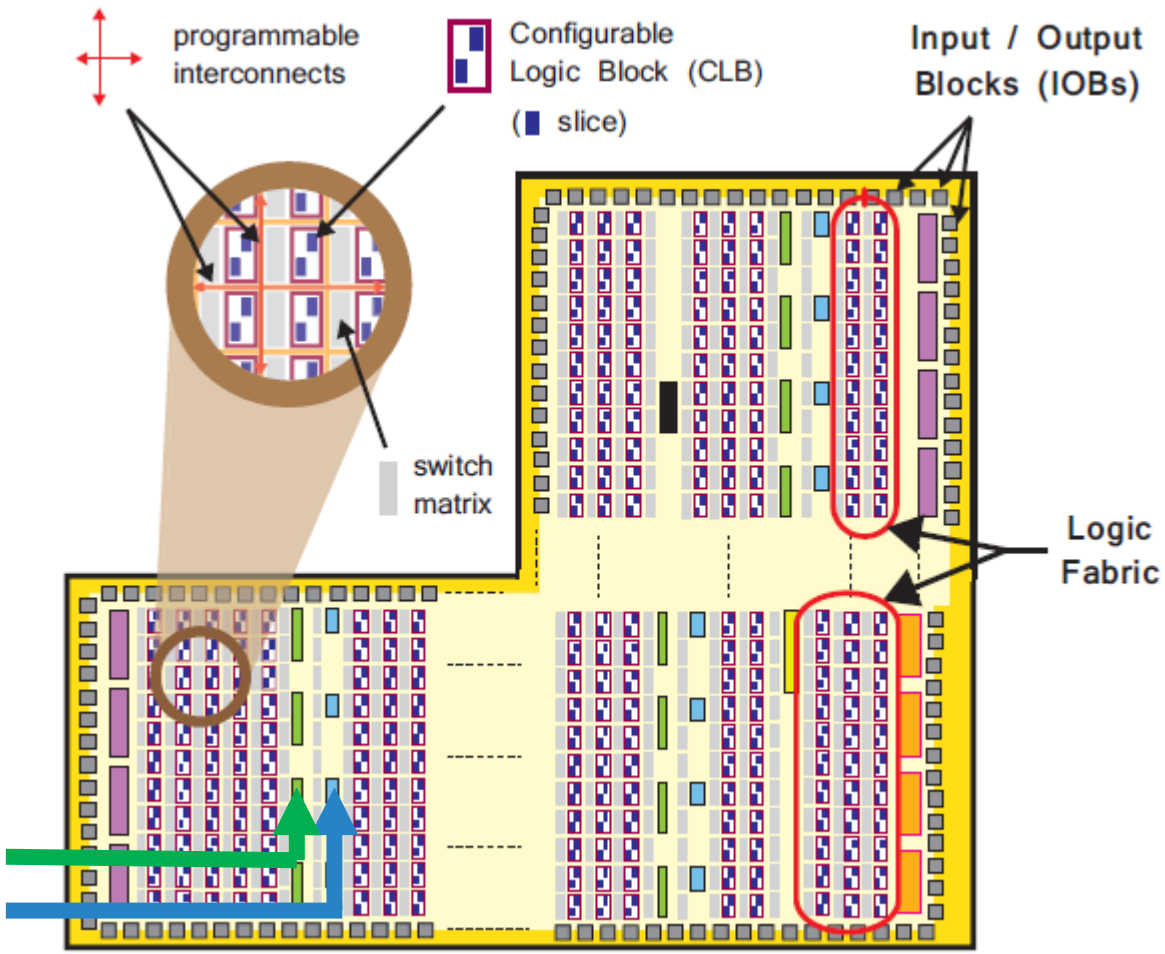


Zynq 7000 APSoC

PL resources:

- Configurable Logic Block (CLB)
  - Slice (x2)
    - LUT (x4)
    - FF (x8)
- Switch Matrix
- Carry Logic
- Input/Output Blocks (IOBs)

- Block RAM
- DSP48E1



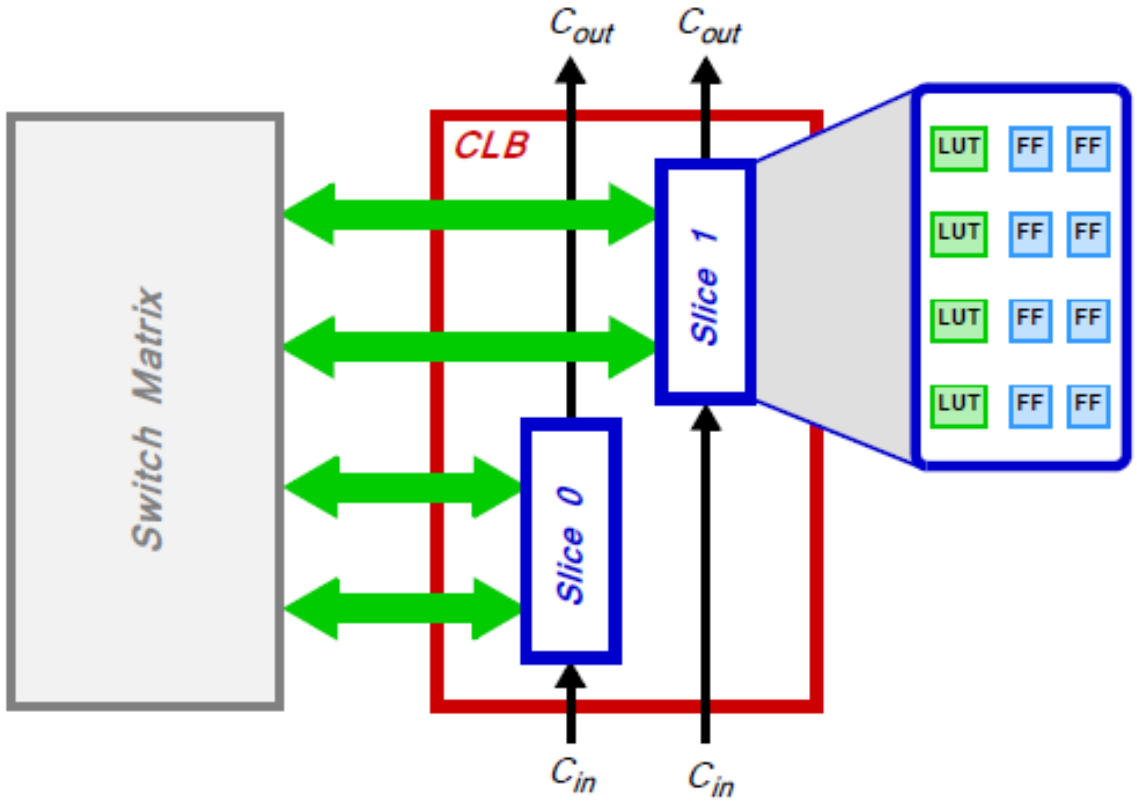
Column of Block RAMs
Column of DSP48E1s

Zynq 7000 APSoC

PL resources:

- **Configurable Logic Block (CLB)**
  - **Slice (x2)**
    - **LUT (x4)**
    - **FF (x8)**
- **Switch Matrix**
- **Carry Logic**
- Input/Output Blocks (IOBs)

- Block RAM
- DSP48E1



Zynq 7000 APSoC

PL resources:

- Configurable Logic Block (CLB)
  - **Slice (x2)**
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- Switch Matrix
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- Input/Output Blocks (IOBs)

- Block RAM
- DSP48E1

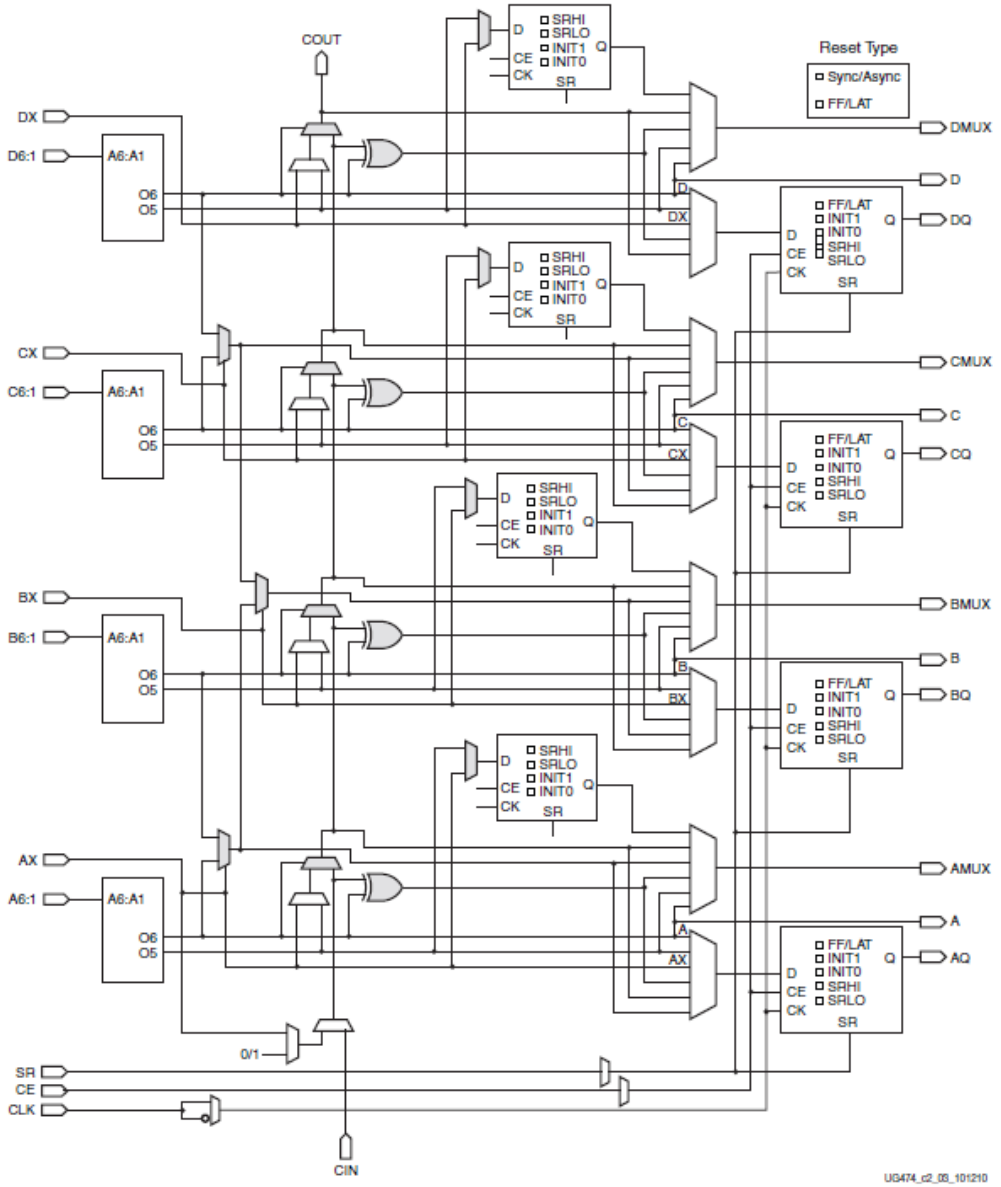


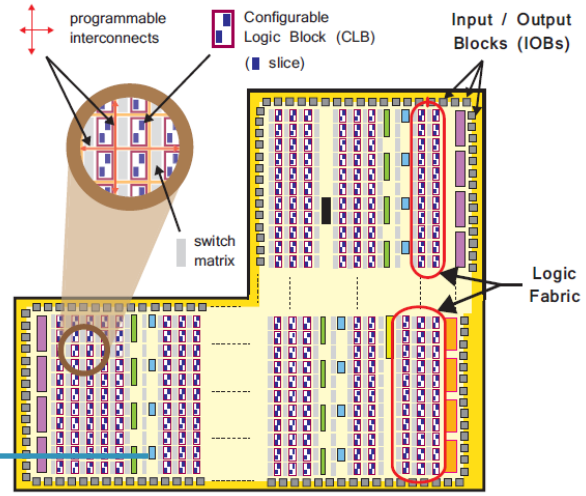
Figure 2-4: **Diagram of SLICEL**

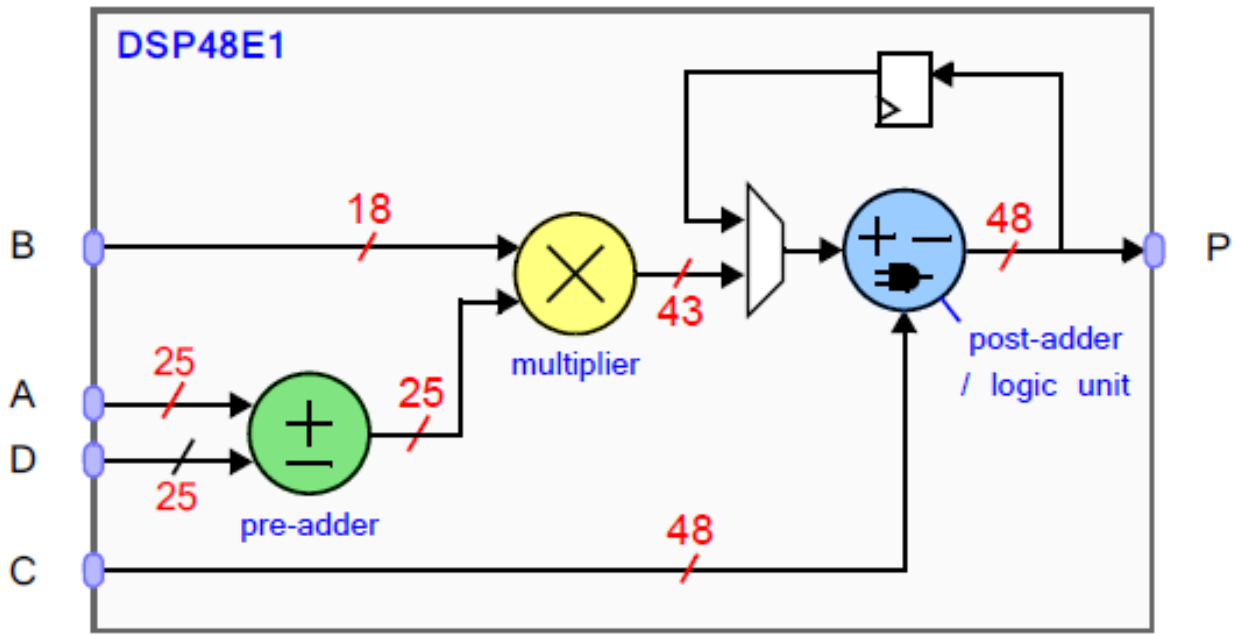
Zynq 7000 APSoC

PL resources:

- Configurable Logic Block (CLB)
  - Slice (x2)
    - LUT (x4)
    - FF (x8)
- Switch Matrix
- Carry Logic
- Input/Output Blocks (IOBs)

- Block RAM
- **DSP48E1**





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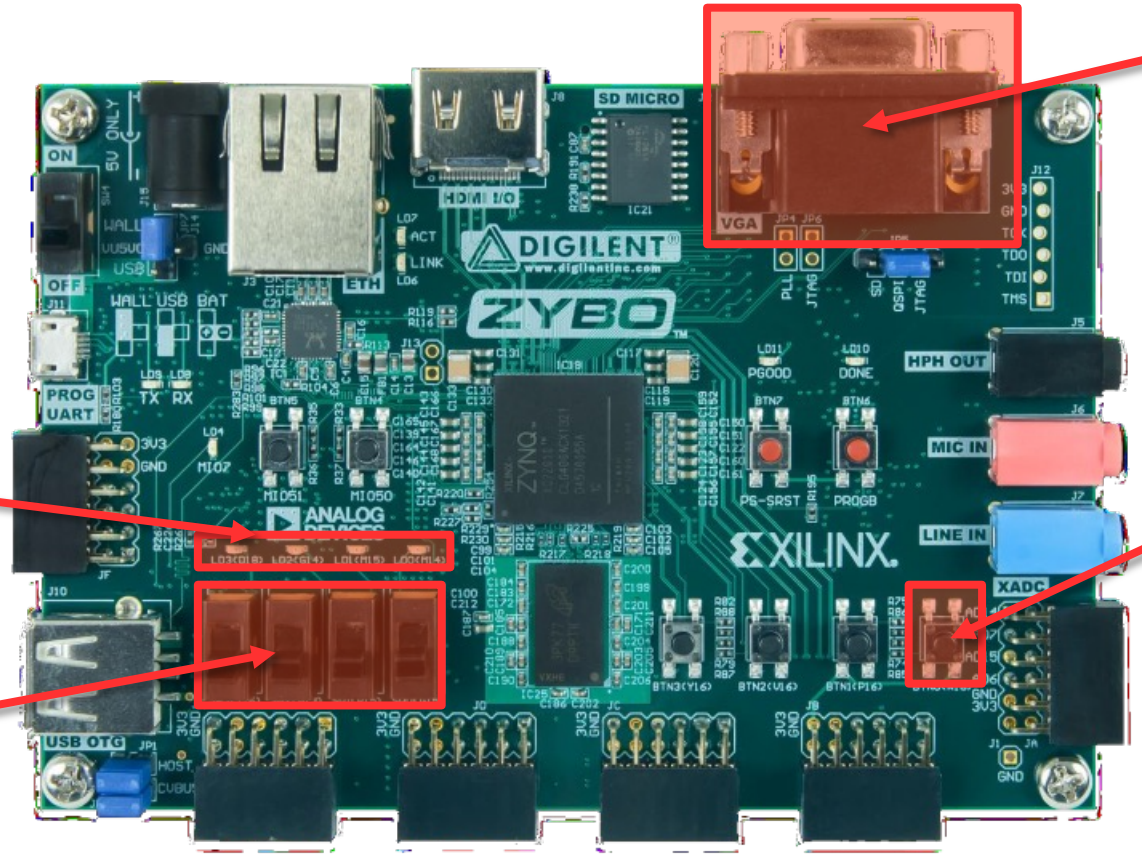
DDFS Wrapper for ZyBo

We need to remap our system into the I/O resources of ZyBo



yq[5:0] **to unsigned**.
On GRN channel

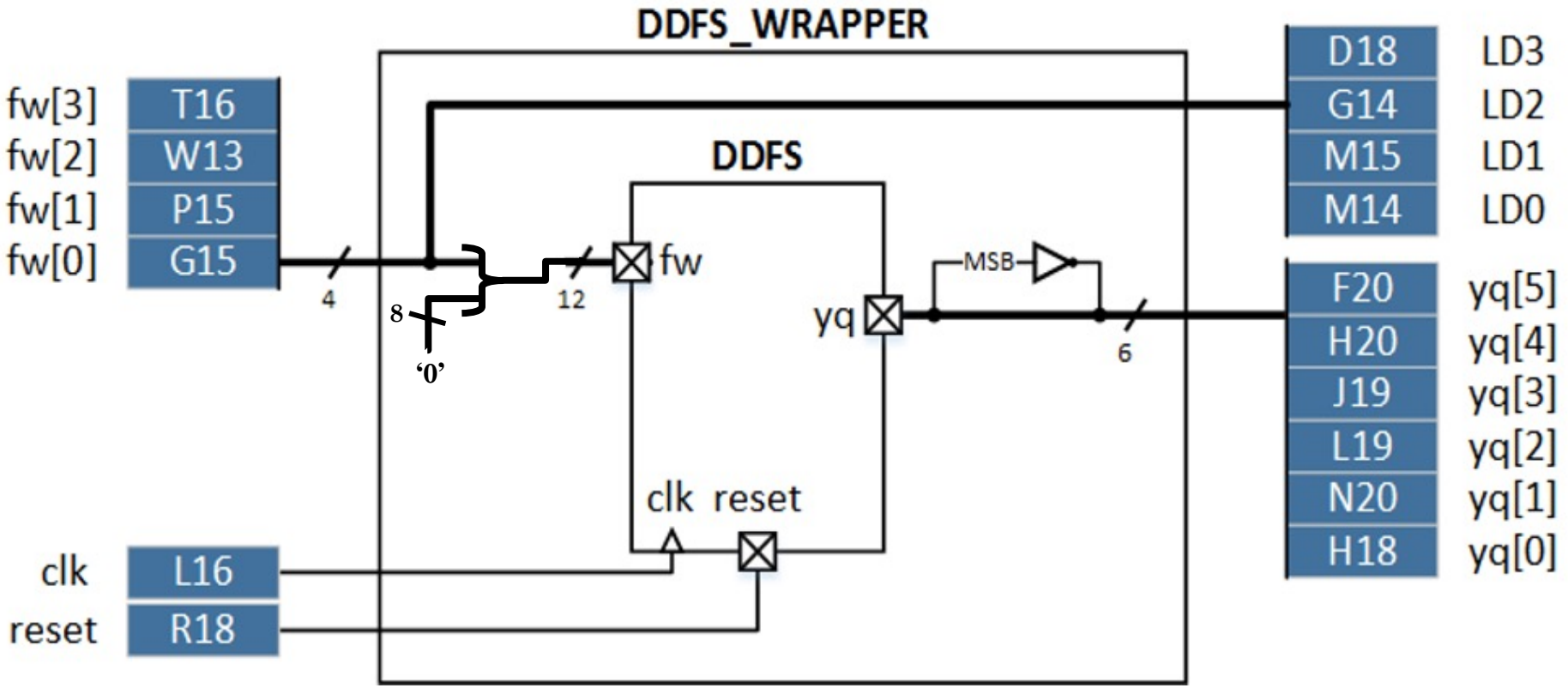
fw[3:0] led
feedback

reset (**active high**)

fw[3:0]

DDFS Wrapper for ZyBo

Write the wrapper for implementation

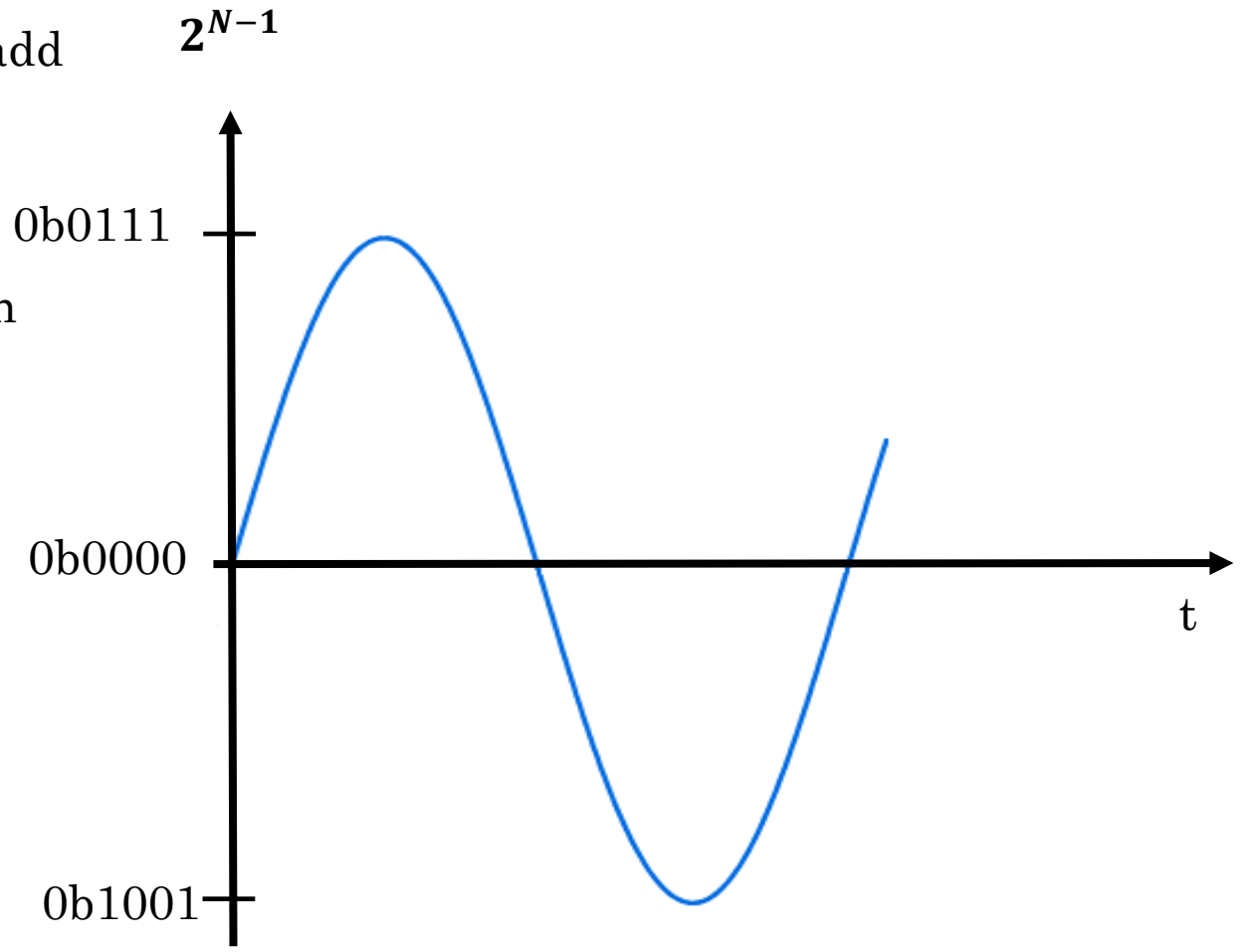


Negation of the MSB: motivation

The DAC converts only to positive values!

The negation of the MSB is equivalent to add

Let's suppose to represent *sin* amplitude in C2 using 4 bits



Negation of the MSB: motivation

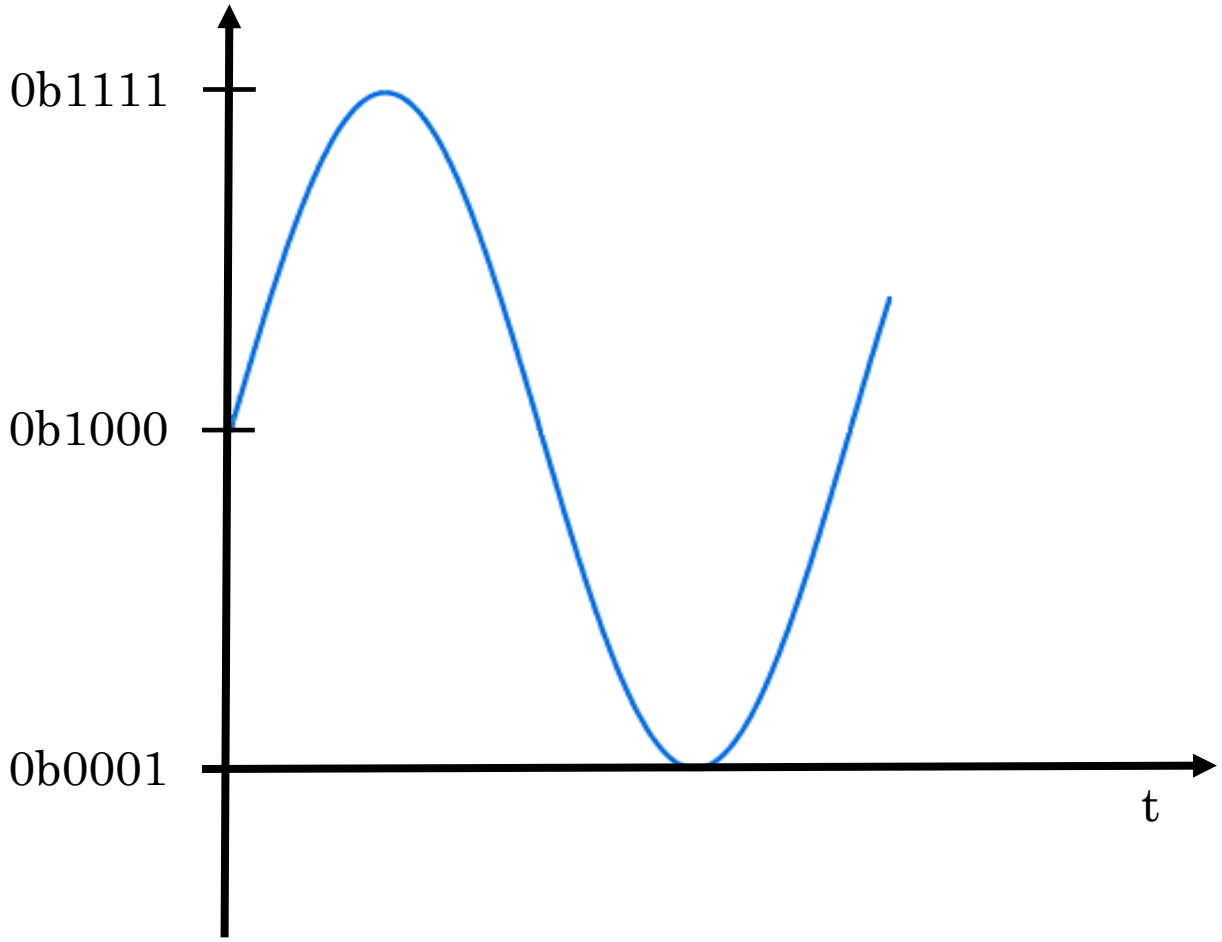
If N = 4, $\mathbf{2^{N-1}}$ is equivalent to **0b1000** (unsigned binary representation) and we have that:

- **0b0000 + 0b1000 = 0b1000**
- **0b0111 + 0b1000 = 0b1111**

Same consideration for negative values:

- **0b1001 + 0b1000 = 0b0001**

TRANSLATION!



Negation of the MSB: motivation

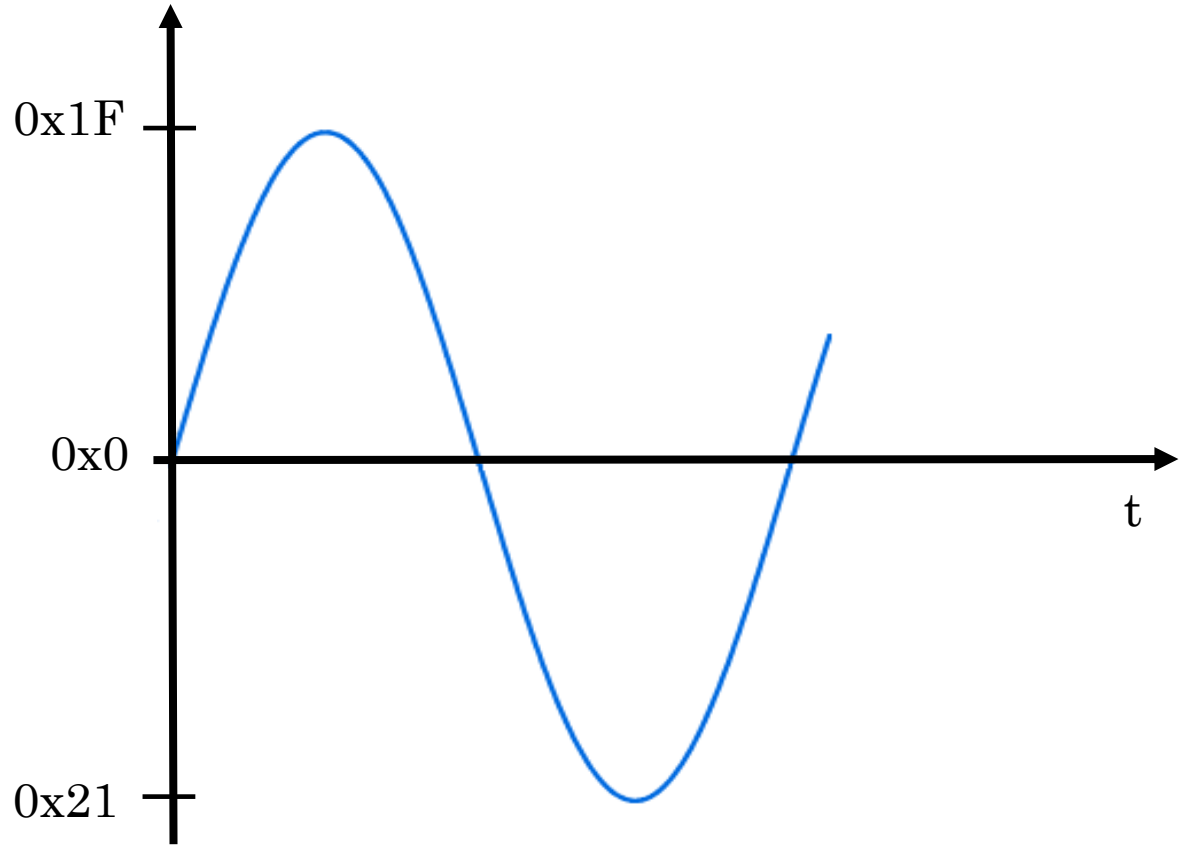
For the DDFS (6 bits):

- Max sample: 31 => 0x1F
- Min sample: -31 => 0x21

Remind: -31 in C2:

- Starting form 31: 0b011111
- Invert all bits: 0b100000
- Add 1: 0b100001

0x21



Negation of the MSB: motivation

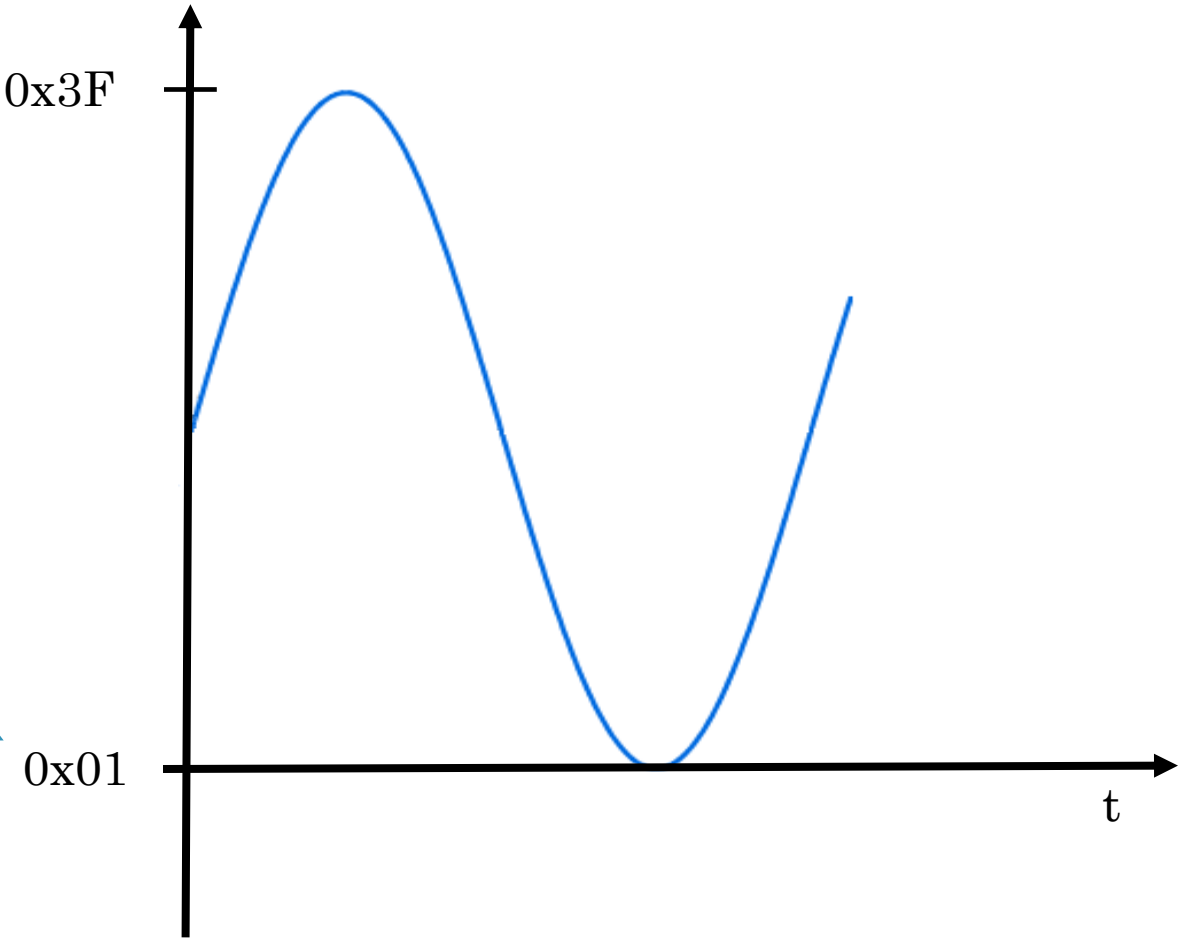
- For the DDFS: (N =6), $\mathbf{2^{N-1}}$ is equivalent to 0b100000 and we have:

Max sample:

- 0x1F => 0b011111
- **0b011111 + 0b100000 = 0b111111**

Min sample:

- 0x21 => 0b100001
- **0b100001 + 0b100000 = 0b000001**



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Xilinx VIVADO Design Suite

FPGA Design Flow

- VHDL
- Verilog
- SV

RTL elaboration
- Compiling
- Design Exploration
- RTL schematic

Synthesis
- Strategies
- Design Constraints
- I/O Pin assignment
- Reports Analysis

Implementation
- Strategies
- Design Constraints
- Timing Analysis
- Power Analysis
- Reports Analysis

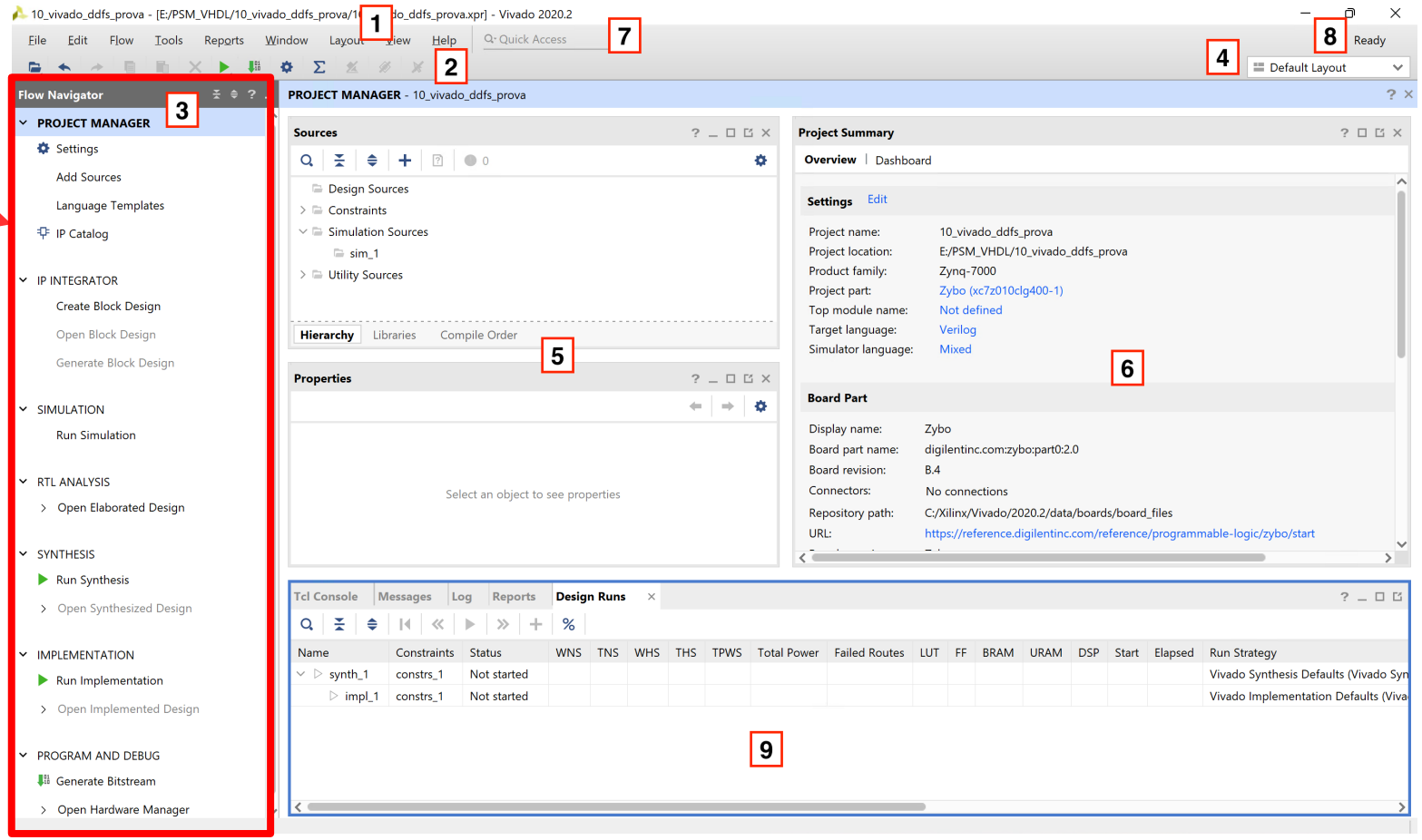
Generate Bitstream
- Programming the Device

Post-Synthesis Simulation

Post-P&R Timing Simulation

Xilinx VIVADO Design Suite

1. Menu Bar
2. Main Toolbar
3. Flow Navigator
4. Layout Selector
5. Data Windows Area
6. Workspace
7. Menu Command Search
8. Project Status Bar
9. Status Bar
10. Result Windows Area



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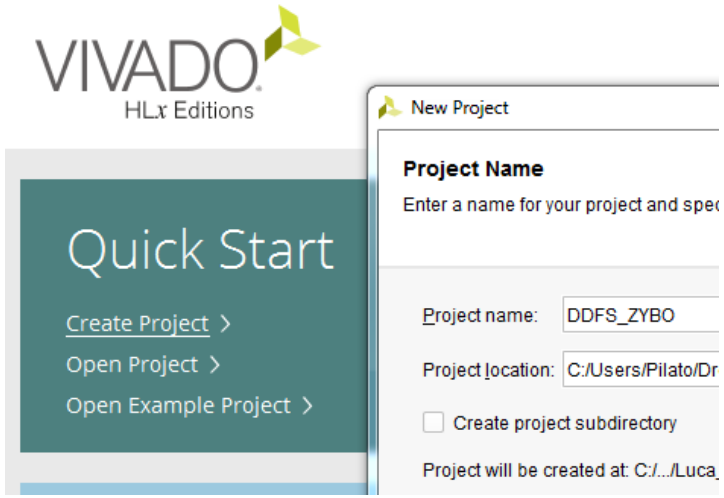
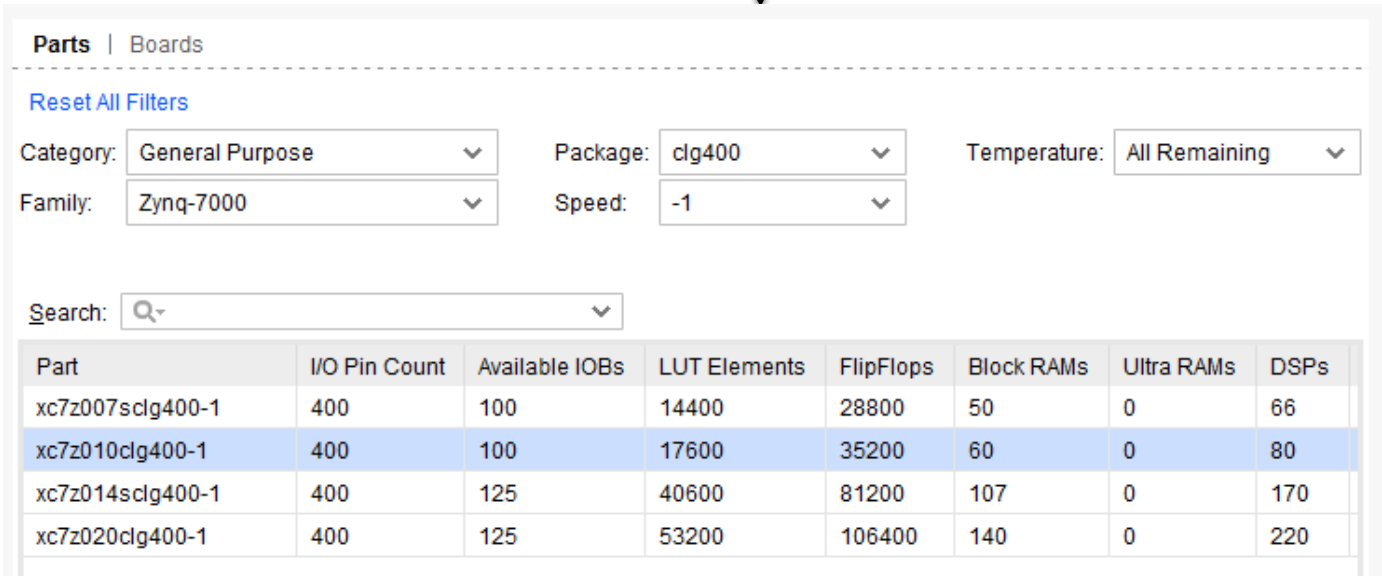
VIVADO Flow

RTL Elaboration → Synthesis → Implement. → Bitstream



RTL Project → Add all VHDL sources



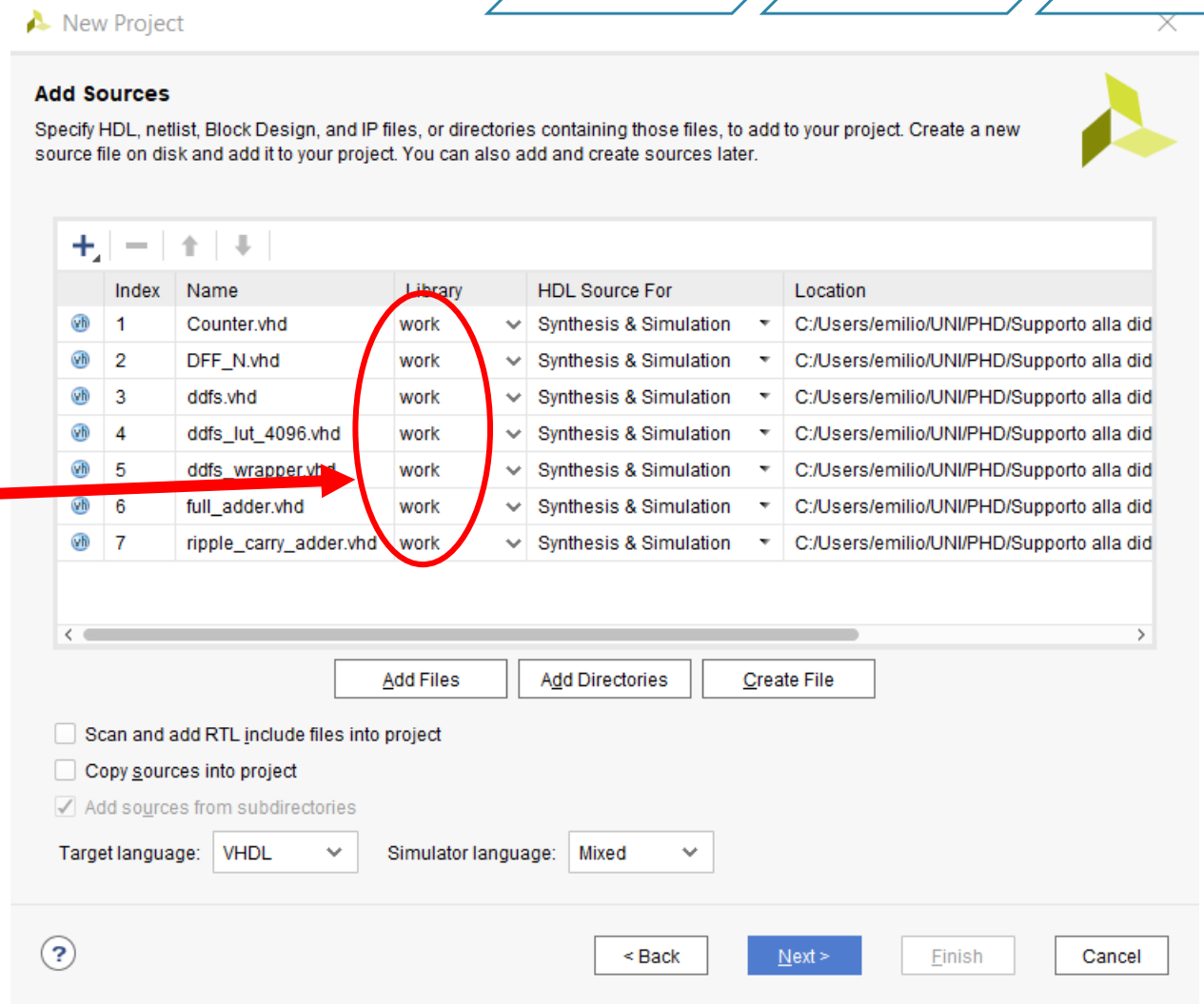
Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs
xc7z007sclg400-1	400	100	14400	28800	50	0	66
xc7z010clg400-1	400	100	17600	35200	60	0	80
xc7z014sclg400-1	400	125	40600	81200	107	0	170
xc7z020clg400-1	400	125	53200	106400	140	0	220

Device: xc7z010clg400-1

VIVADO Flow

RTL Elaboration → Synthesis → Implement. → Bitstream

When loading src files, select the «work» library if you have packages to include



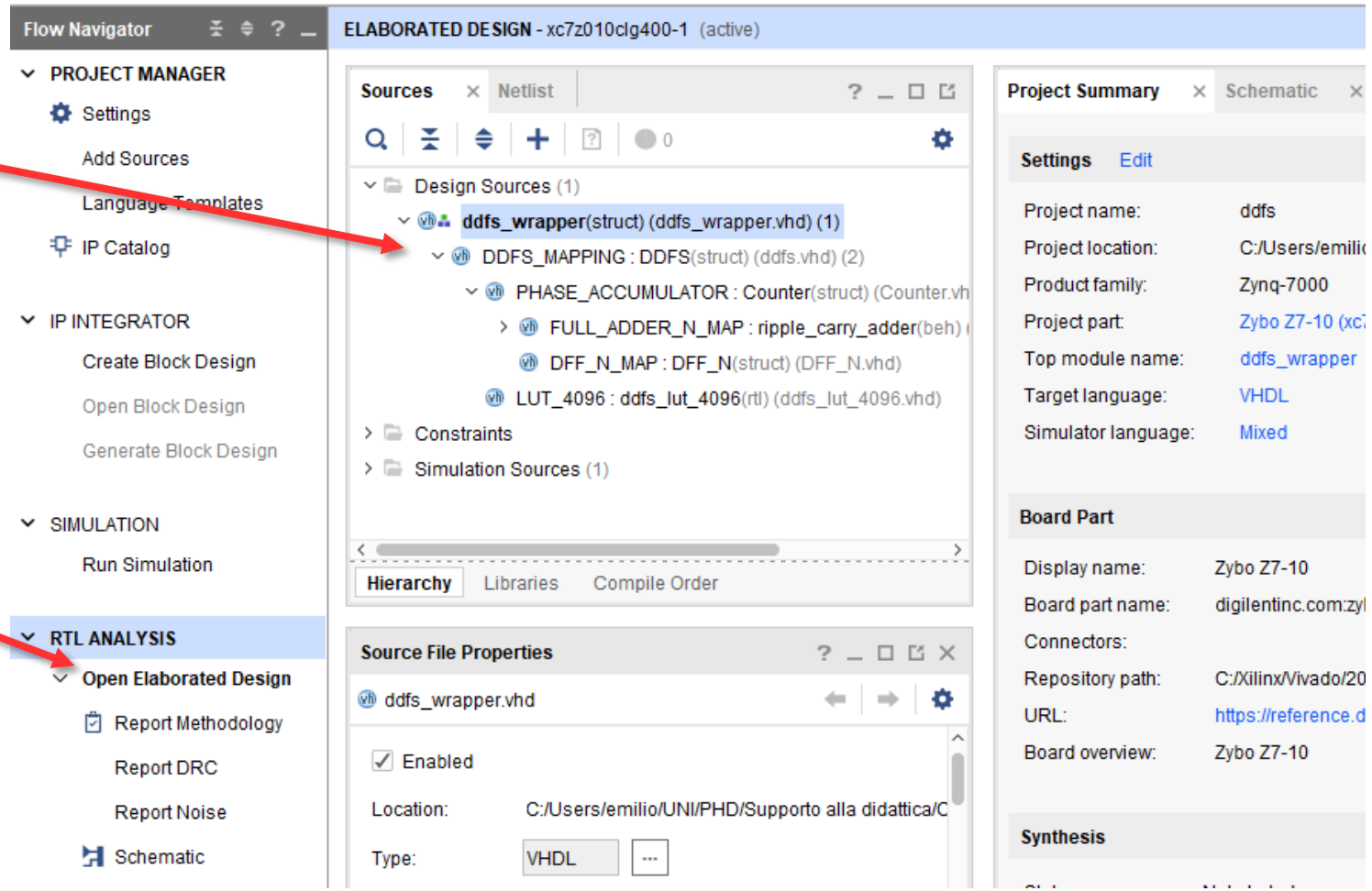
VIVADO Flow

RTL Elaboration → Synthesis → Implement. → Bitstream

Hierarchy is automatically resolved

Open Elaborated Design:

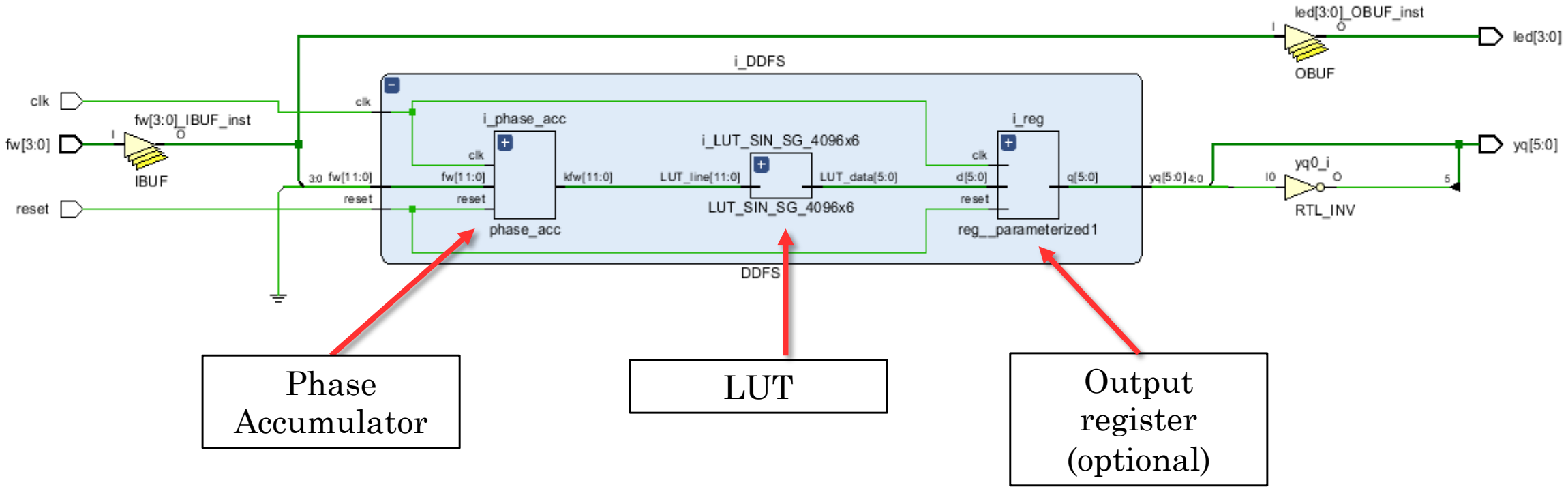
- Checks VHDL consistency
- Allows RTL analysis



VIVADO Flow

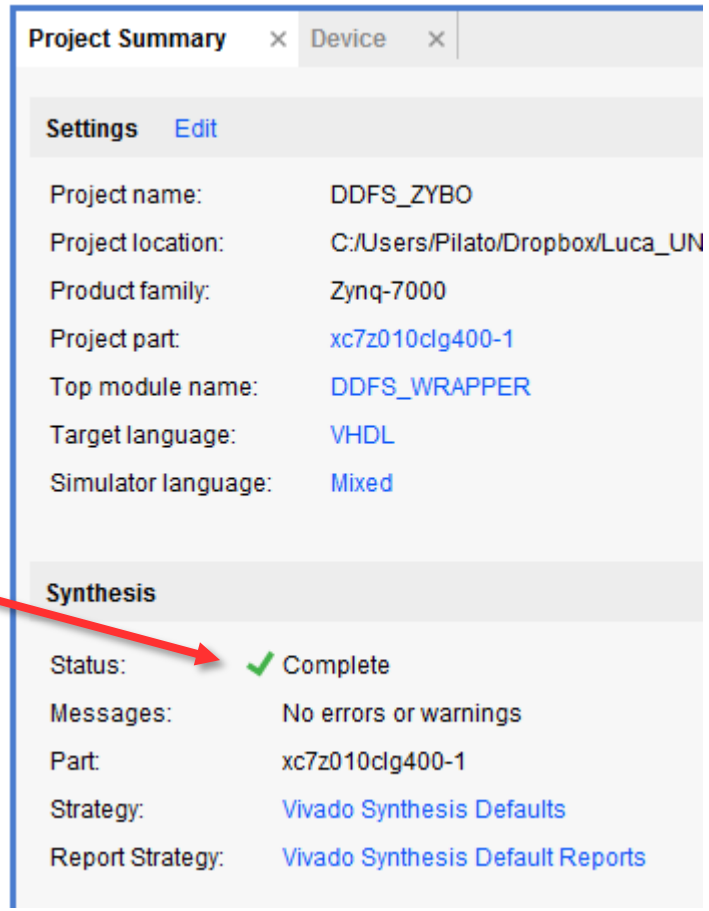
RTL Elaboration → Synthesis → Implement. → Bitstream

RTL ANALYSIS → Open Elaborated Design → Schematic



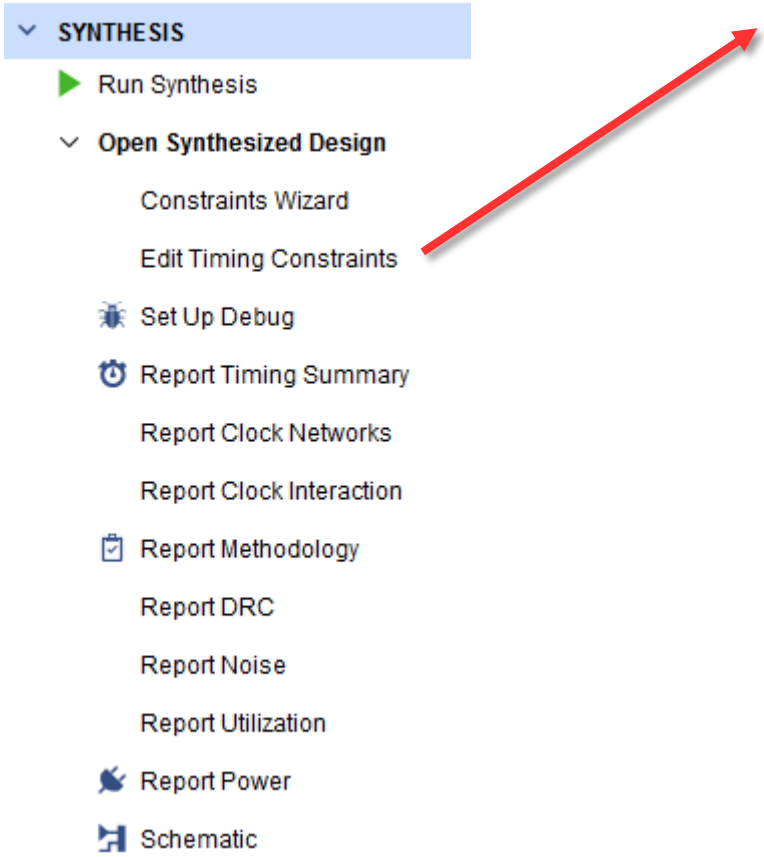
VIVADO Flow

- Close the Elaborated Design
- Run a first Synthesis (without constraints)
- …
- …
- At the end Open Synthesized Design
- Open Project Summary
- Check any messages

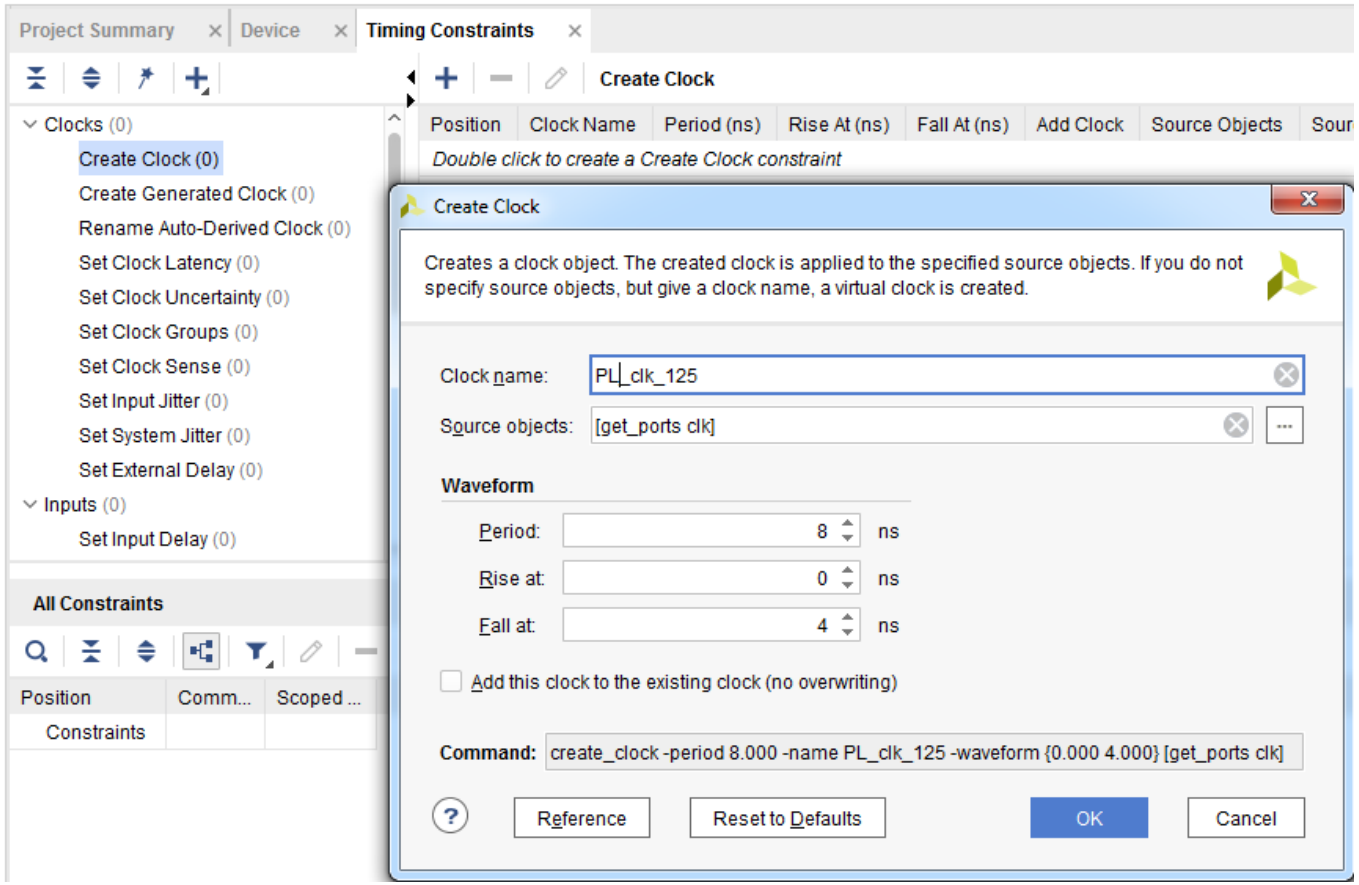


VIVADO Flow

RTL Elaboration → **Synthesis** → Implement. → Bitstream



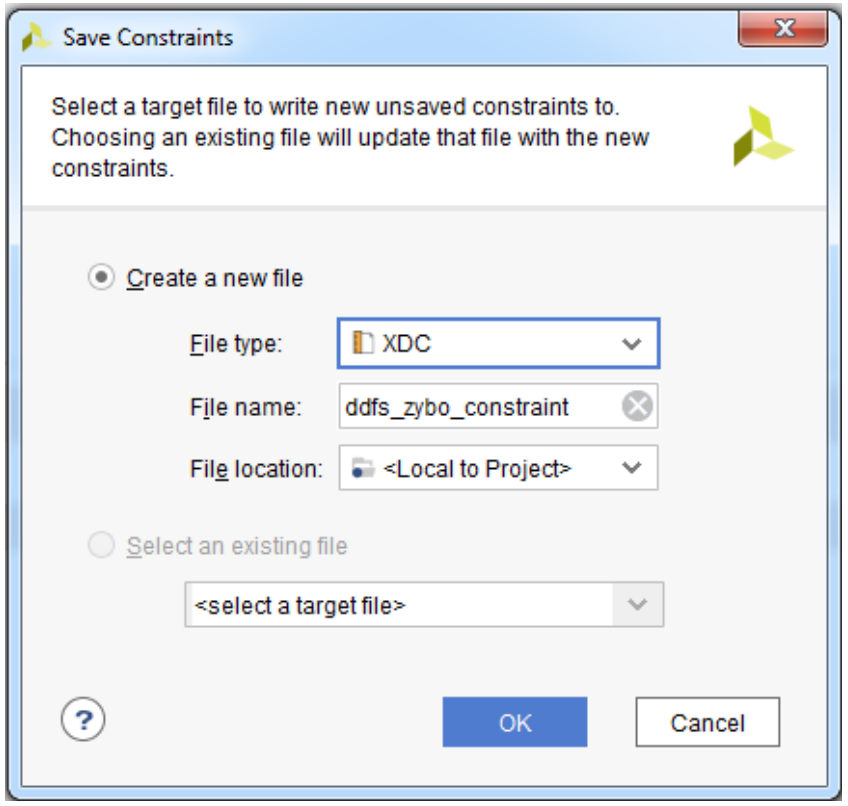
We need to specify clock constraints

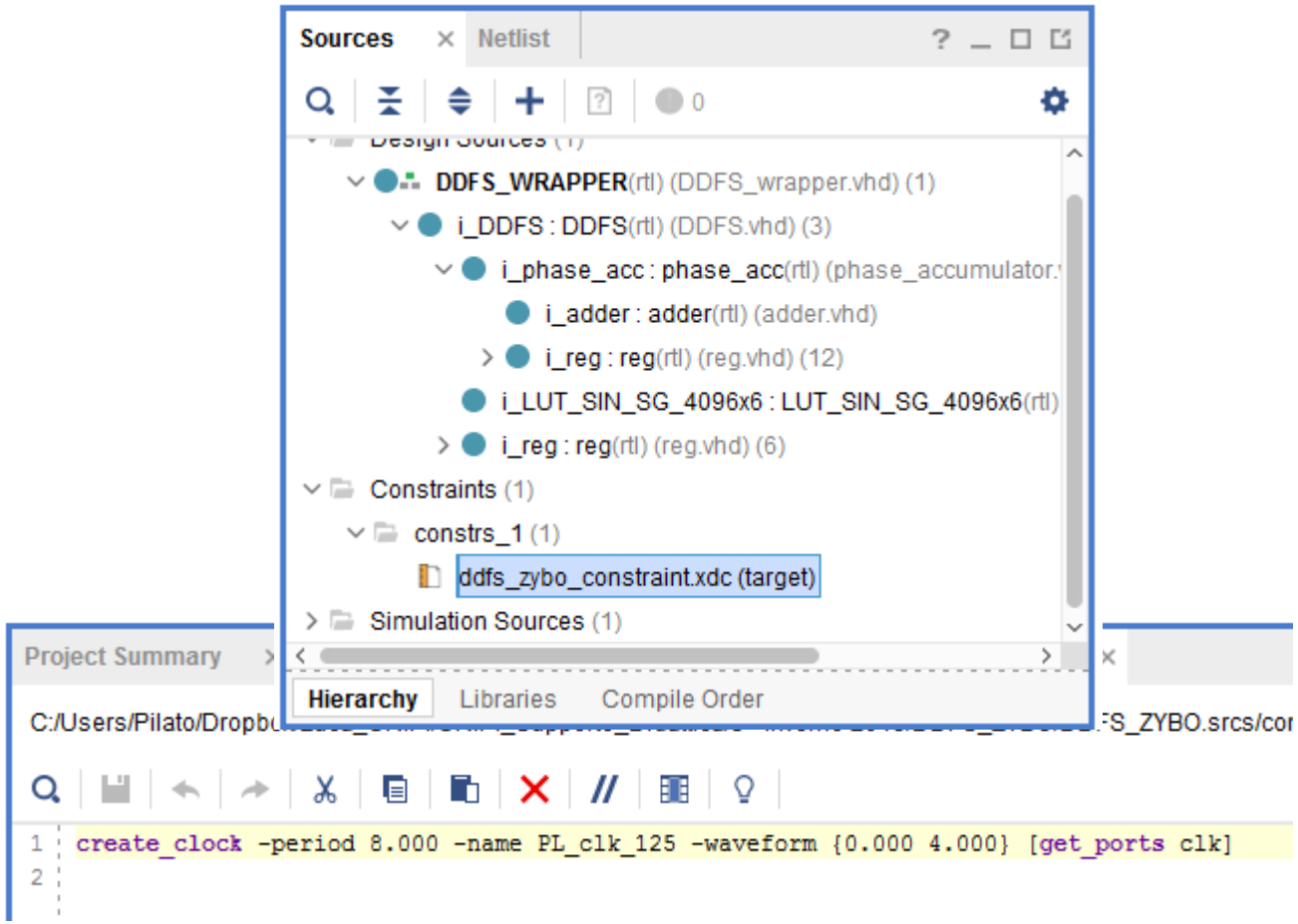


VIVADO Flow

RTL Elaboration → **Synthesis** → Implement. → Bitstream

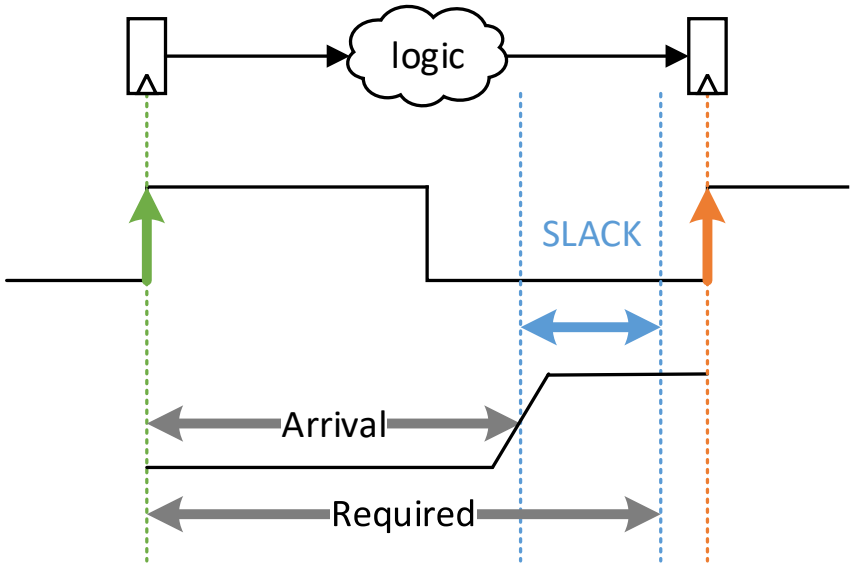
Save and look the xdc file





VIVADO Flow

- Re-Run the synthesis
- Check the Slack (Report Timing Summary)
  - Slack: "Arrival – Required" Time
  - Positive OK
  - Negative BAD



WNS: Worst Negative Slack (CRITICAL PATH)
TNS: Total Negative Slack (sum of negative slacks)

Design Timing Summary

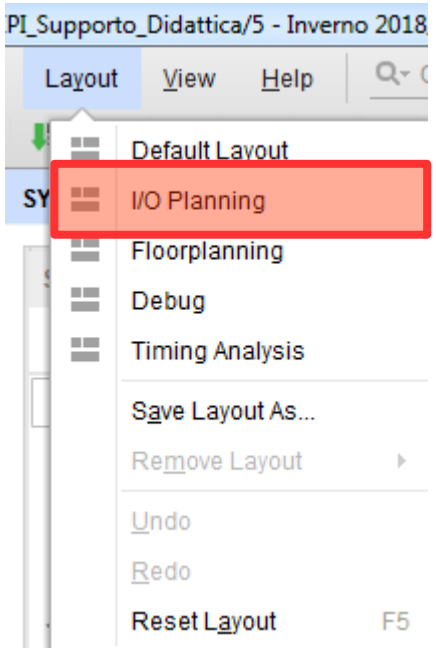
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3,196 ns	Worst Hold Slack (WHS):	0,170 ns	Worst Pulse Width Slack (WPWS):	3,500 ns
Total Negative Slack (TNS):	0,000 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	18	Total Number of Endpoints:	18	Total Number of Endpoints:	19

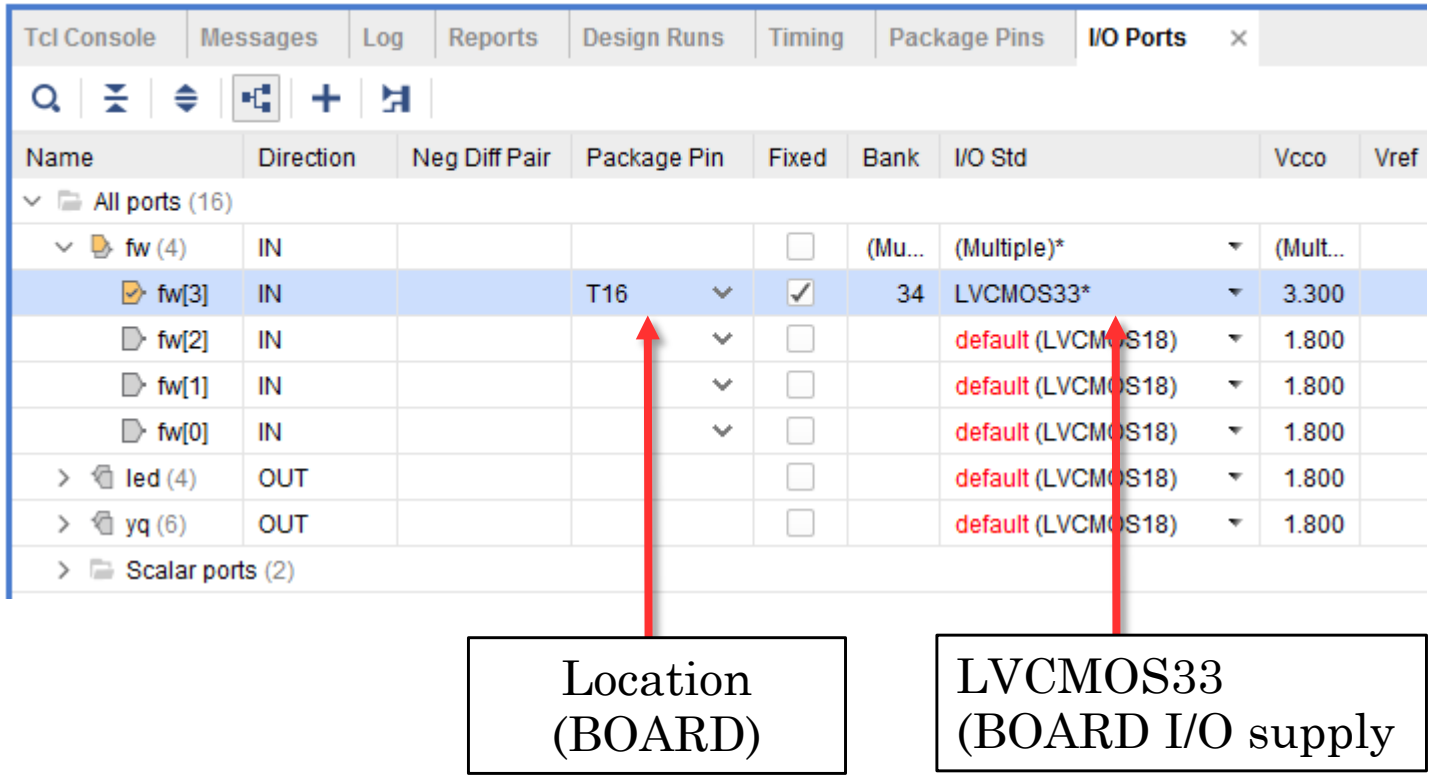
All user specified timing constraints are met.

VIVADO Flow

RTL Elaboration → **Synthesis** → Implement. → Bitstream

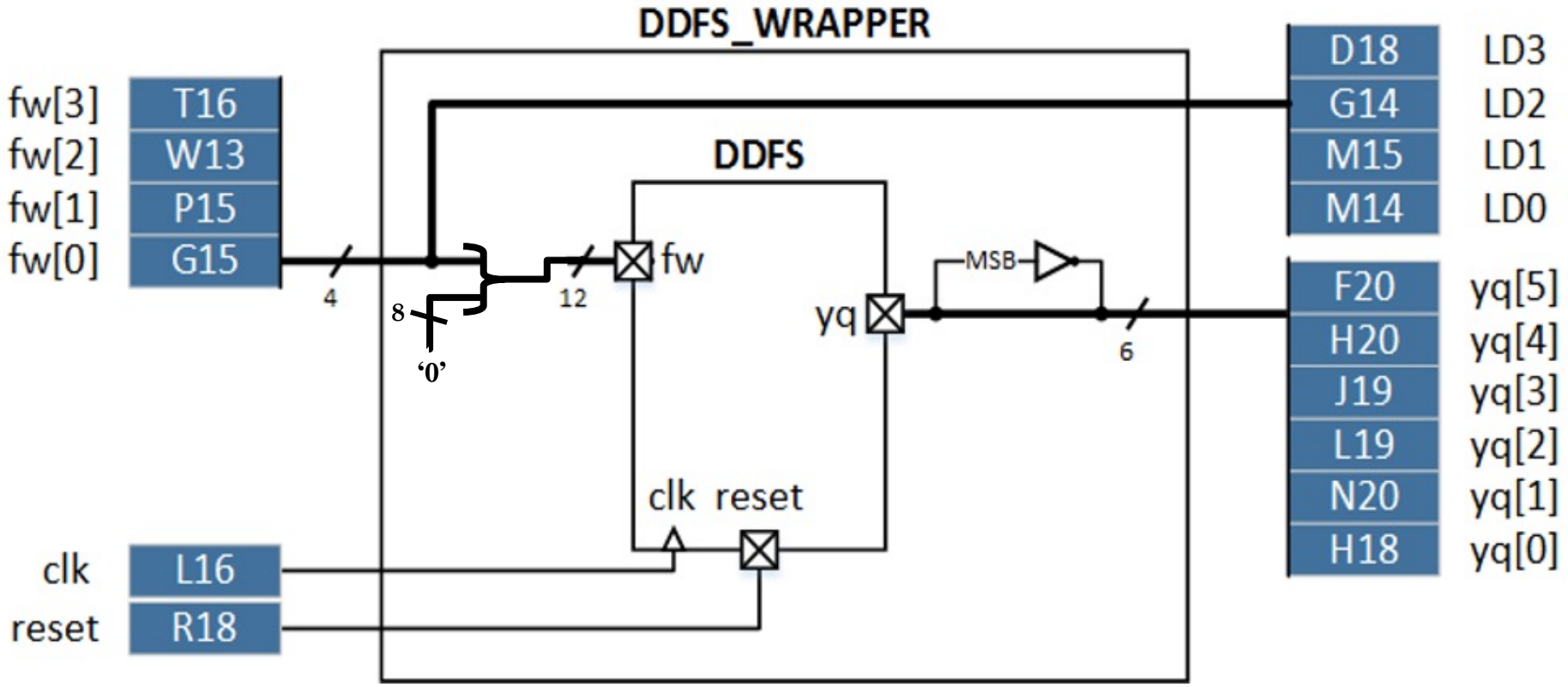
It is possible to assign I/O pin before Implementation. (Physical Constraints)





VIVADO Flow

It is possible to assign I/O pin before Implementation. (Physical Constraints)



VIVADO Flow

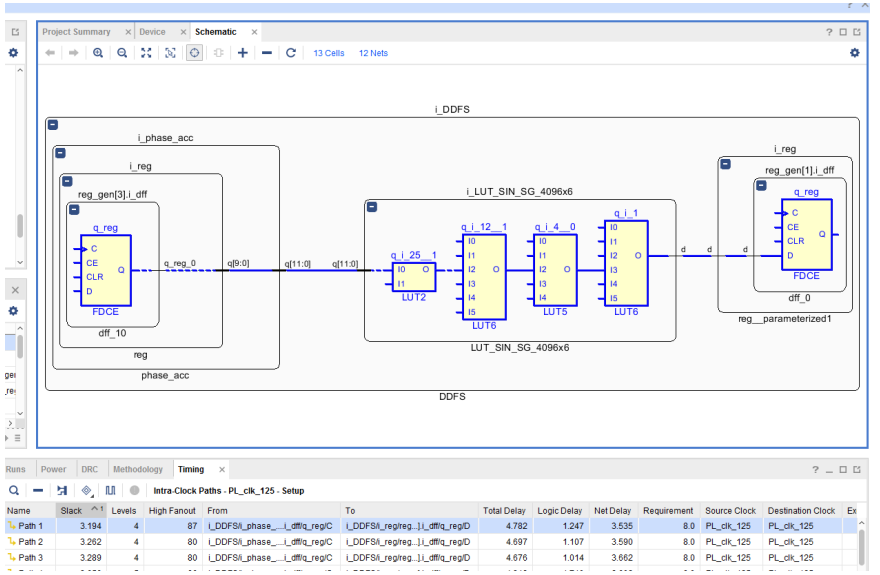
RTL Elaboration → Synthesis → **Implement.** → Bitstream

Run an Implementation (with constraints)

…

At the end Open Implemented Design:

- Project Summary
  - Check errors/warnings/messages
- Report timing
  - Check the slack



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3,194 ns	Worst Hold Slack (WHS):	0,228 ns	Worst Pulse Width Slack (WPWS):	3,500 ns
Total Negative Slack (TNS):	0,000 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	18	Total Number of Endpoints:	18	Total Number of Endpoints:	19

All user specified timing constraints are met.

VIVADO Flow

After implementation it is possible to check results in the Project Summary:

- Errors and warnings
- Resources Utilization (Graph or Table)
- Timing analysis
- Power consumption estimation

DRC Violations

Summary: 1 warning

Implemented DRC Report

Timing — **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	3.121 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	30

Implemented Timing Report

Utilization — Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	129	17600	0.73
FF	30	35200	0.09
IO	16	100	16.00
BUFG	1	32	3.13

Power — **Summary** | On-Chip

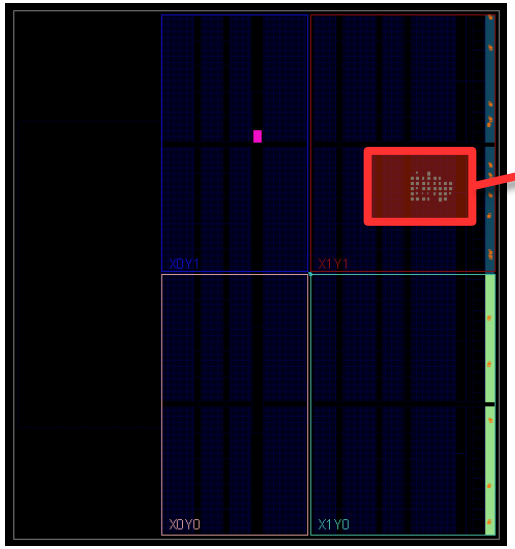
Total On-Chip Power:	**0.109 W**
Junction Temperature:	**26,3 °C**
Thermal Margin:	58,7 °C (5,0 W)
Effective ϑJA:	11,5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

VIVADO Flow

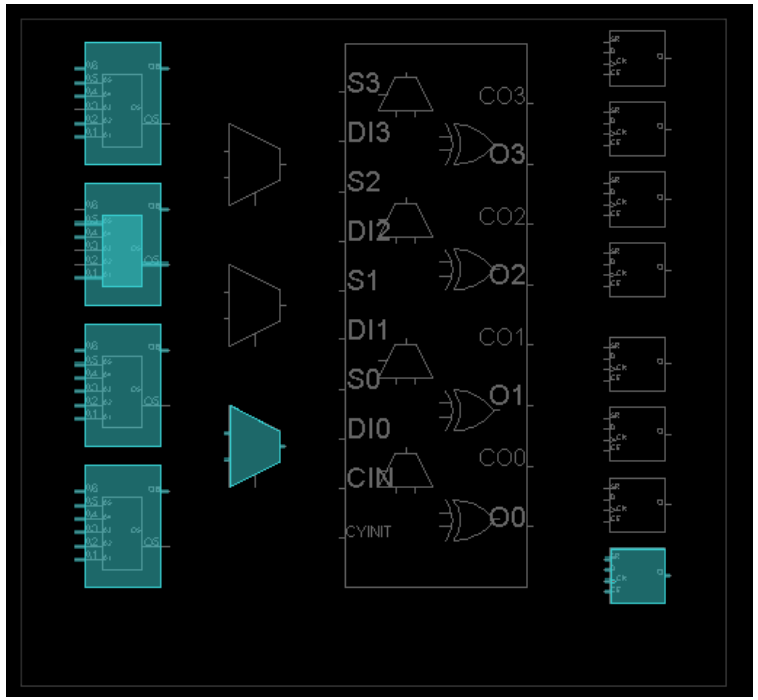
RTL Elaboration → Synthesis → **Implement.** → Bitstream

Open Implemented Design → «Device» window



Device

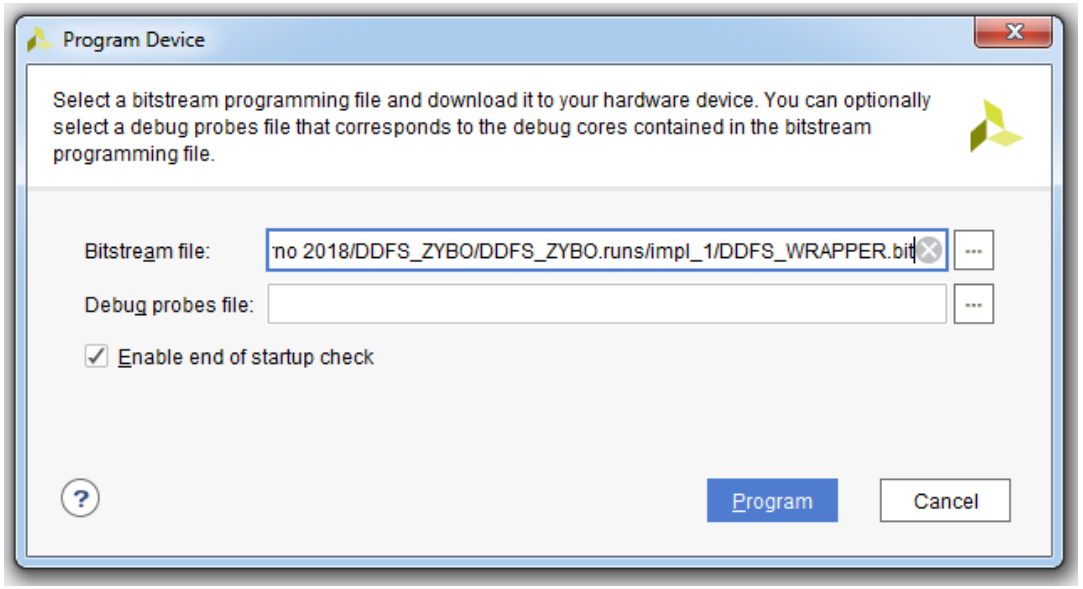
Fabric Logic

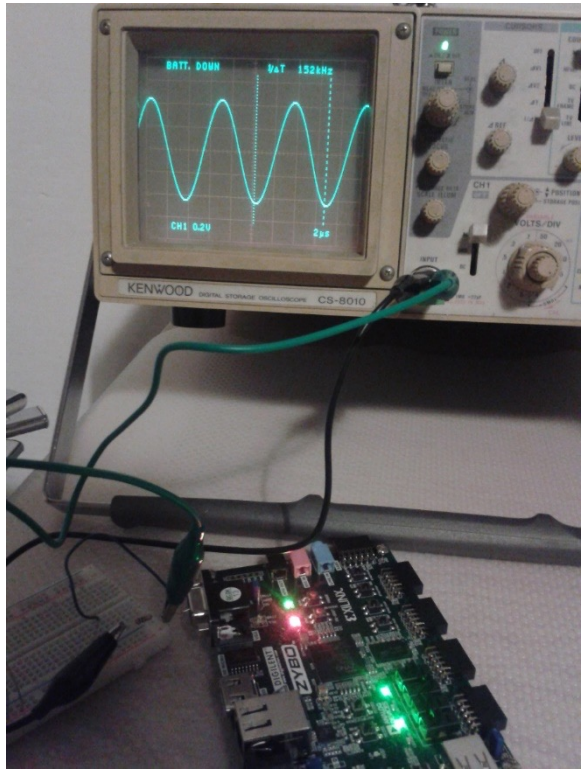


Slice

VIVADO Flow

- Generate the bitstream file (*.bit)
- Connect the Device (ZyBo Board)
- Open Hardware Manager
- Program the Device
- Evaluate your DDFS





End, Questions?

1) ZyBo Development Board
2) Zynq 7000 APSoC
3) DDFS Implementation on ZyBo
4) Xilinx VIVADO Design Suite
5) Vivado Design Flow