Electronics and Communication Systems
Electronics Systems

Master Degree in Computer Engineering

https://computer.ing.unipi.it/ce-lm

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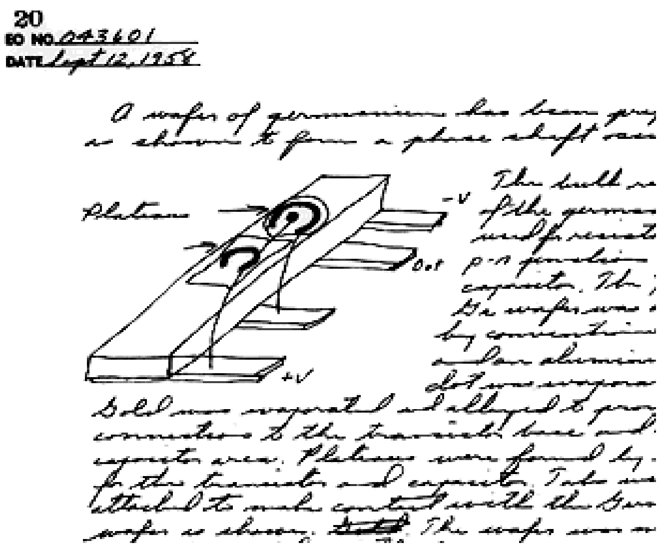
Outline

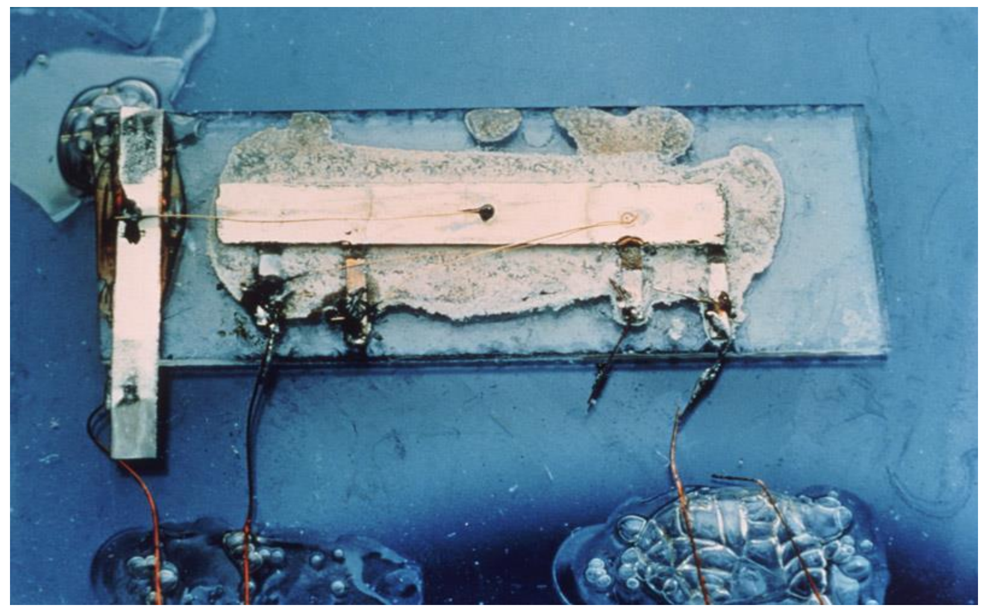
- What is an integrated circuit ?
- What is VLSI ?
- VLSI Technology Trends

What is an Integrated Circuit?

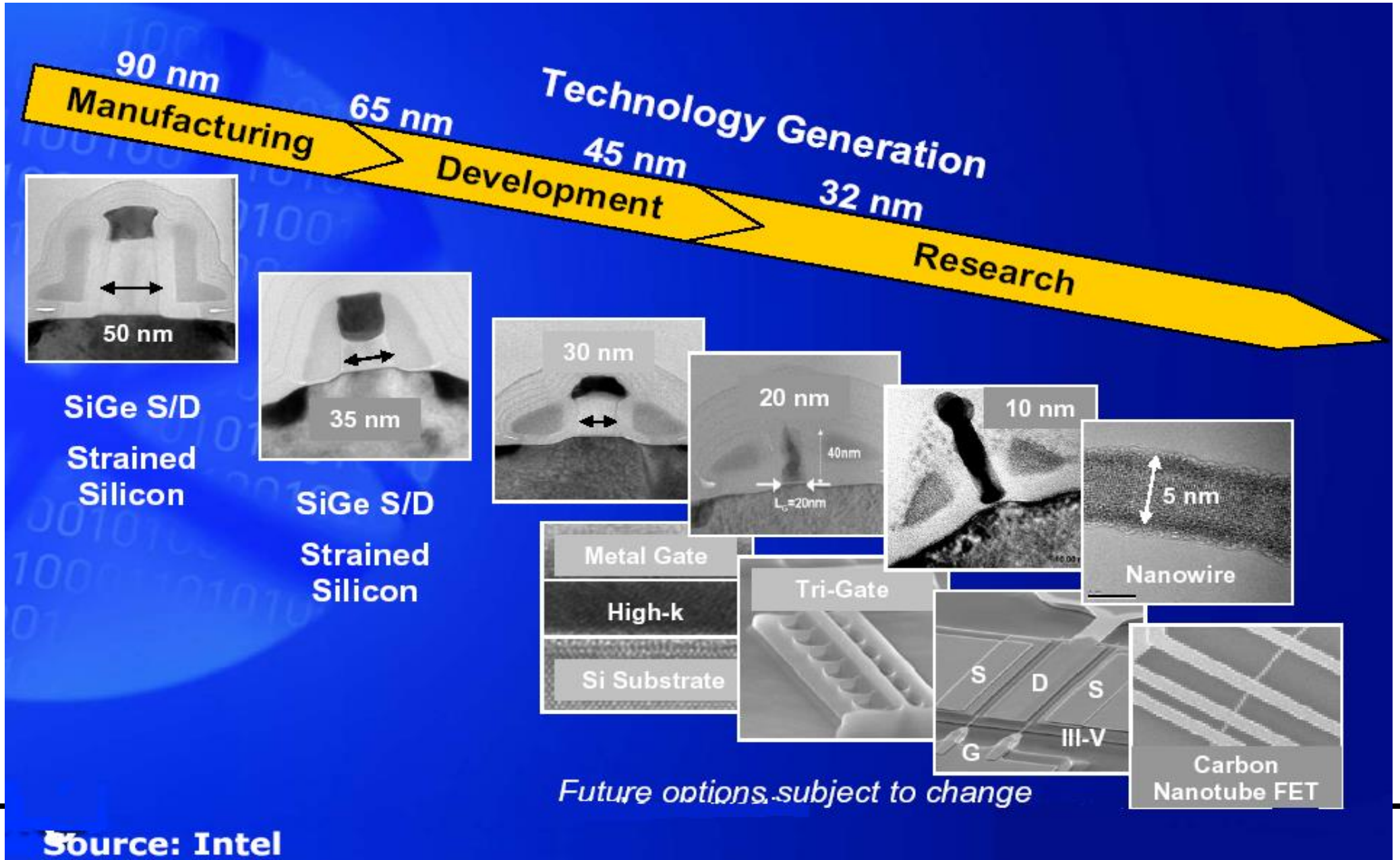
- A device having multiple electrical components and their interconnects manufactured on a single substrate.



US Patent # 3,138,743 filed Feb. 6, 1959

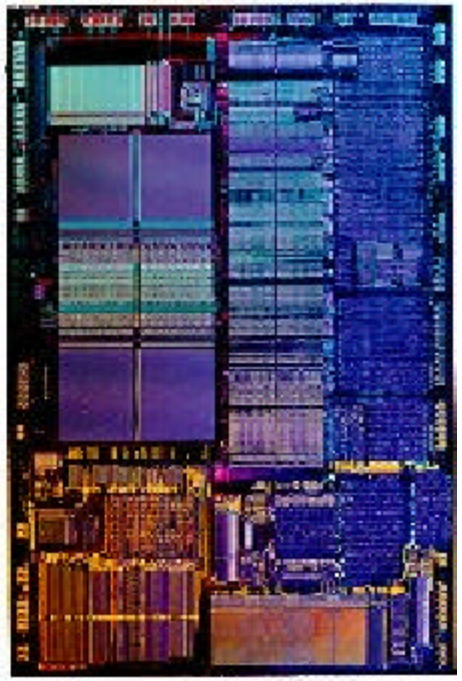


CMOS technology advances



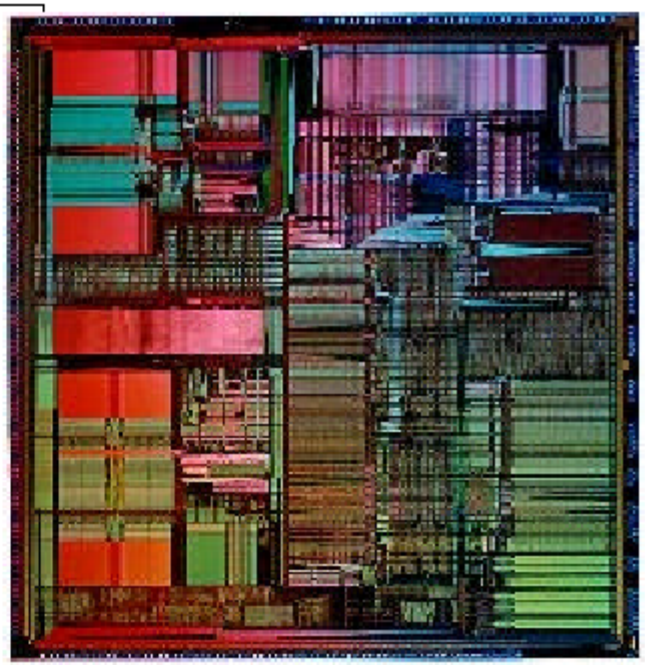
Intel 486™ DX CPU

- Design 1986 – 1989
- 25 MHz, 33 MHz
- 1.2 M transistors
- 1.0 micron
- 5 stage pipeline
- Unified 8 KByte code/data cache (write-through)
- First IA-32 processor capable of executing 1 instruction per clock cycle



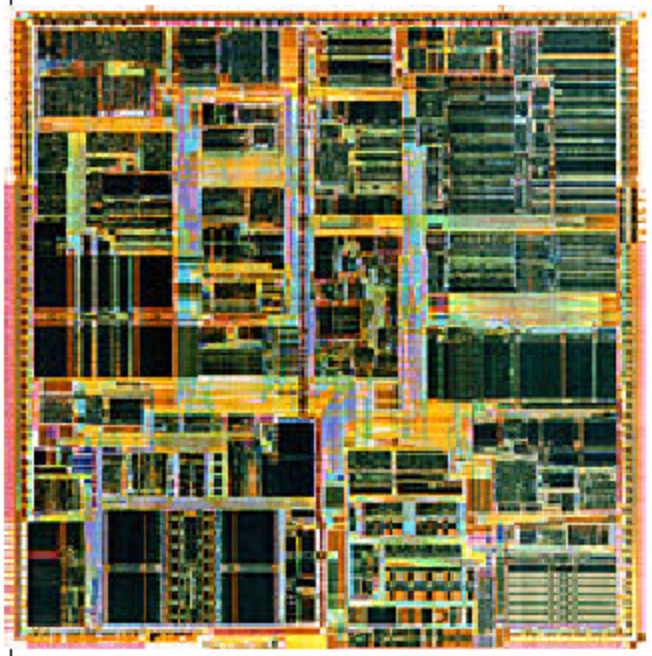
Pentium Processor

- Design 1989 – 1993
- 60 MHz, 66 MHz
- 3.1 M transistors
- 0.8 micron
- 5 stage pipeline
- 8 KByte instruction and 8 KByte data caches (writeback)
- Branch predictor
- Pipelined floating point
- First superscalar IA-32: capable of executing 2 instructions per clock



Pentium II Processor

- Design 1995 – 1997
- 233 MHz, 266 MHz, 300 MHz
- 7.5 M transistors
- 0.35 micron
- 16 KByte L1I, 16 KByte L1D, 512 KByte off-die L2
- First compaction of P6 microarchitecture



Pentium III Processor (Katmai)

- Introduced: 1999
- 450 MHz, 500 MHz, 533 MHz, 600MHz
- 9.5 M transistors
- 0.25 micron
- 16 KByte L1I, 16 KByte L1D, 512 KByte off-chip L2
- Addition of SSE instructions.

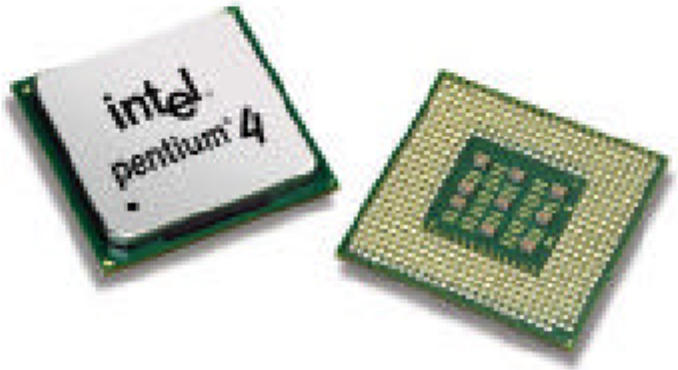
SSE: Intel Streaming SIMD Extensions to the x86 ISA

Pentium III Processor (Coppermine)

- Introduced: 1999
- 500MHz ... 1133MHz
- 28 M transistors
- 0.18 micron
- 16 KByte L1I, 16 KByte L1D, 256KByte on-chip L2
- Integrate L2 cache on chip, It topped out at 1GHz.

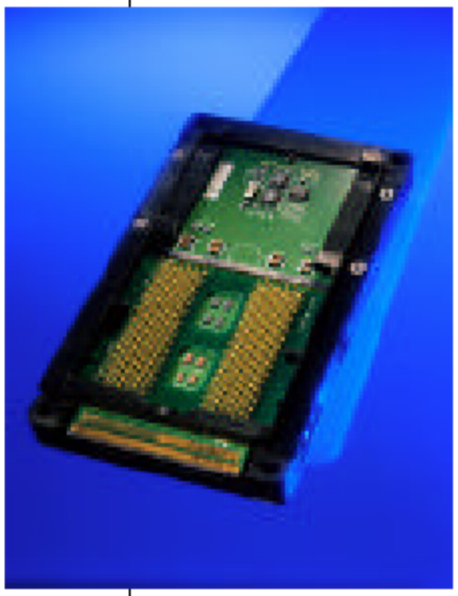
Pentium IV Processor

- Introduced: 2000
- 1.3GHz ... 2GHz ... 3.4GHz
- 42M ... 55M ... 125 M transistors
- 0.18 ... 0.13 ... 0.09 micron
- Latest one: 16 KByte L1I, 16 KByte L1D, 1M on-chip L2
- Very high clock speed and SSE performance



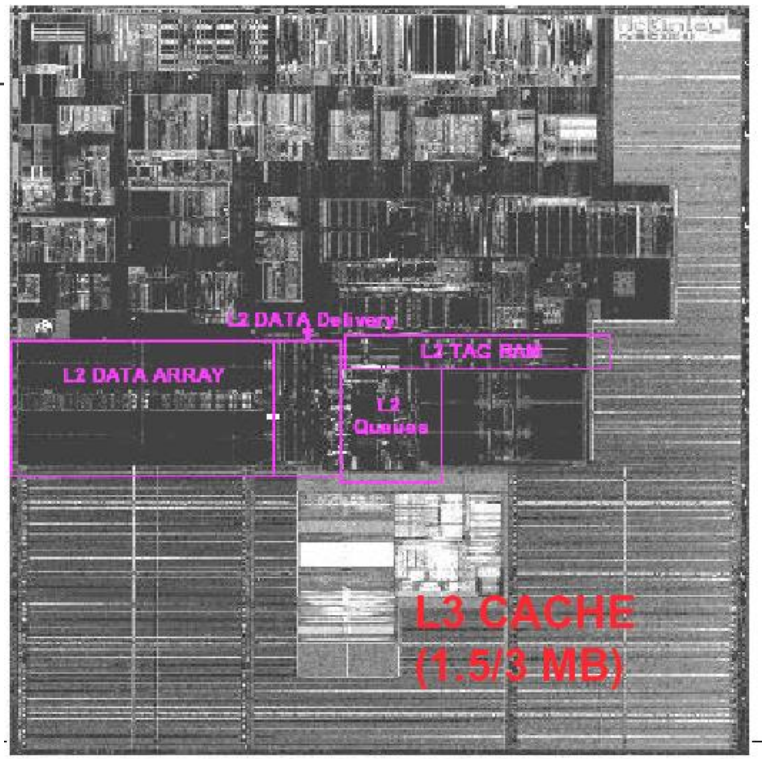
Intel Itanium Processor

- Design 1993 – 2000
- 733 MHz, 800 MHz
- 25 M transistors
- 0.18 micron
- 3 levels of cache
  - 16 KByte L1I, 16 KByte L1D
  - 96 KByte L2
  - 4 MByte off-die L3
- Superscalar degree 6, in-order machine
- ~~First implementation of 64-bit Itanium~~ architecture



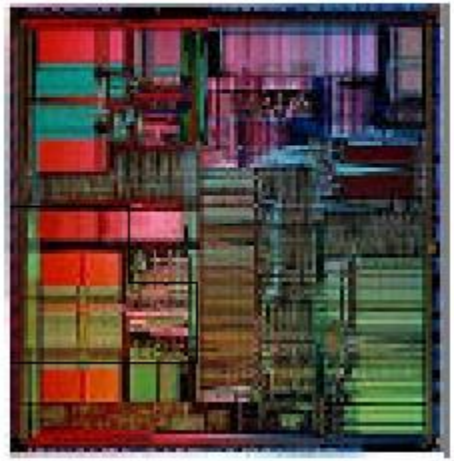
Intel Itanium 2 Processor

- Introduced: 2002
- 1GHz
- 221 M transistors
- 0.18 micron
- 3 levels of cache
  - 32 KByte I&D L1
  - 256 KByte L2
  - integrated 1.5MByte L3
- Based on EPIC architecture
- Enhanced Machine Check Architecture (MCA) with extensive Error Correcting Code (ECC)



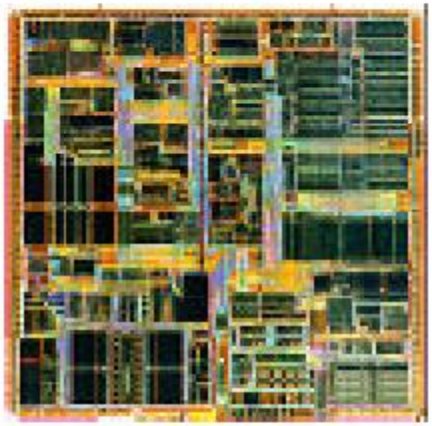
Cache size becoming larger and larger

1993: Pentium



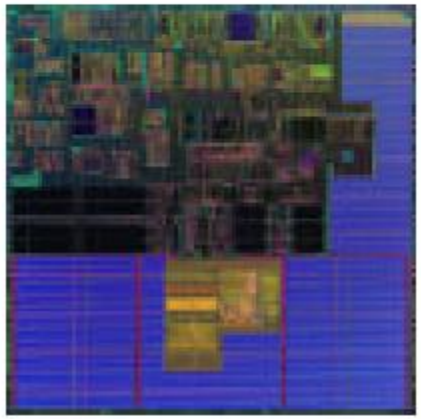
8 KByte I-cache and
8 KByte D-cache

1997: Pentium-II



- 16 KByte L1I, 16 KByte L1D
- 512 KByte off-die L2

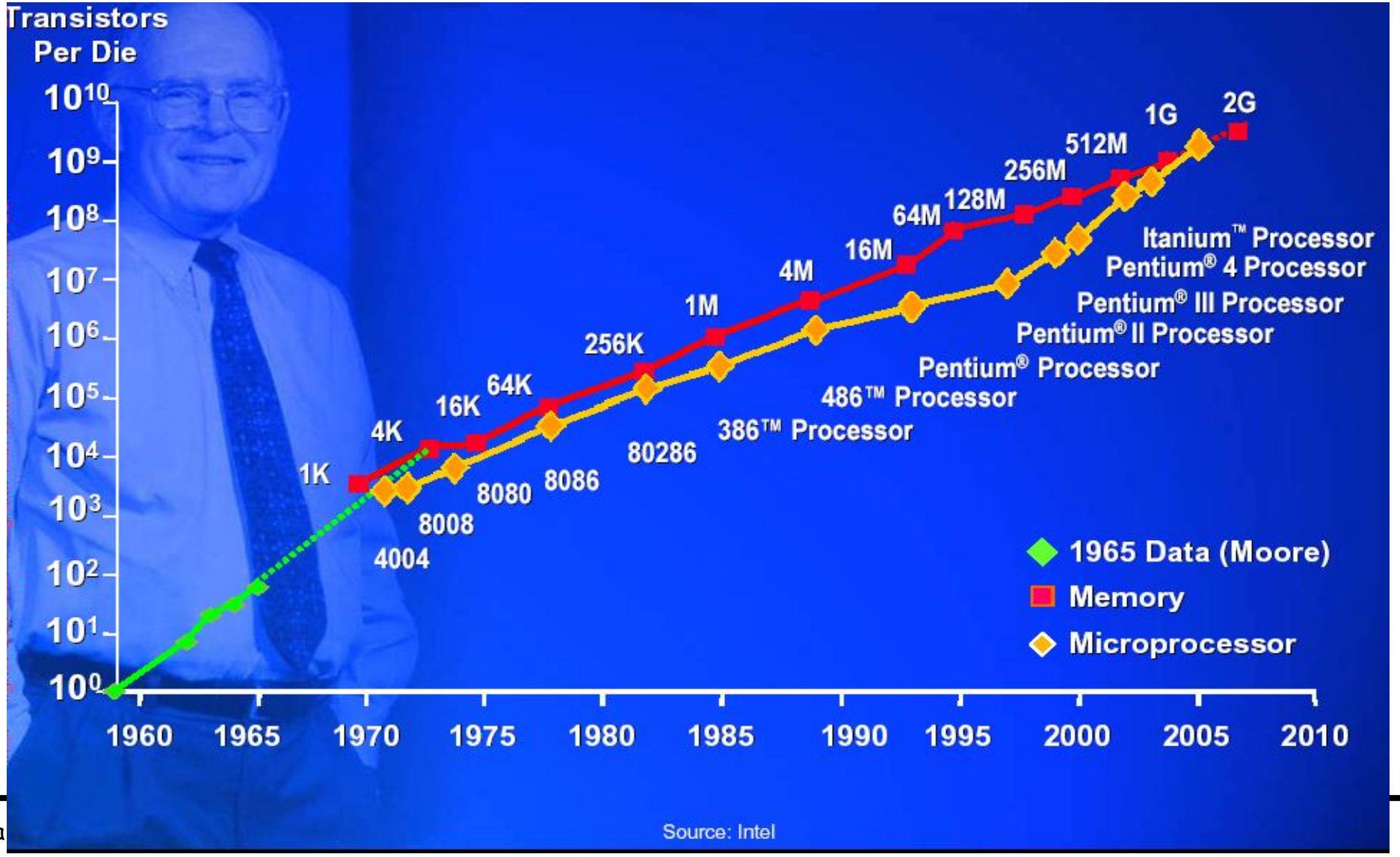
2002: Itanium-2



- Level 1: 16K KByte I-cache, 16 KByte D-cache
- Level 2: 256 KB
- Level 3: integrated 3 MB or 1.5 MB

Moore's Law

- Original "law": number of components on IC doubles every year
- Later modified to doubling every 18 months



Moore's Law

Cramming More Components onto Integrated Circuits

GORDON E. MOORE, LIFE FELLOW, IEEE

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65 000 components on a single silicon chip.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turnaround.

I. Present and Future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures, and semiconductor integrated circuits.

Reprinted from Gordon E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, pp. 114–117, April 19, 1965.
Publisher Item Identifier S 0018-9219(98)00753-1.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

Both approaches have worked well and are being used in equipment today.

II. The Establishment

Integrated electronics is established today. Its techniques are almost mandatory for new military systems, since the reliability, size, and weight required by some of them is achievable only with integration. Such programs as Apollo, for manned moon flight, have demonstrated the reliability of integrated electronics by showing that complete circuit functions are as free from failure as the best individual transistors.

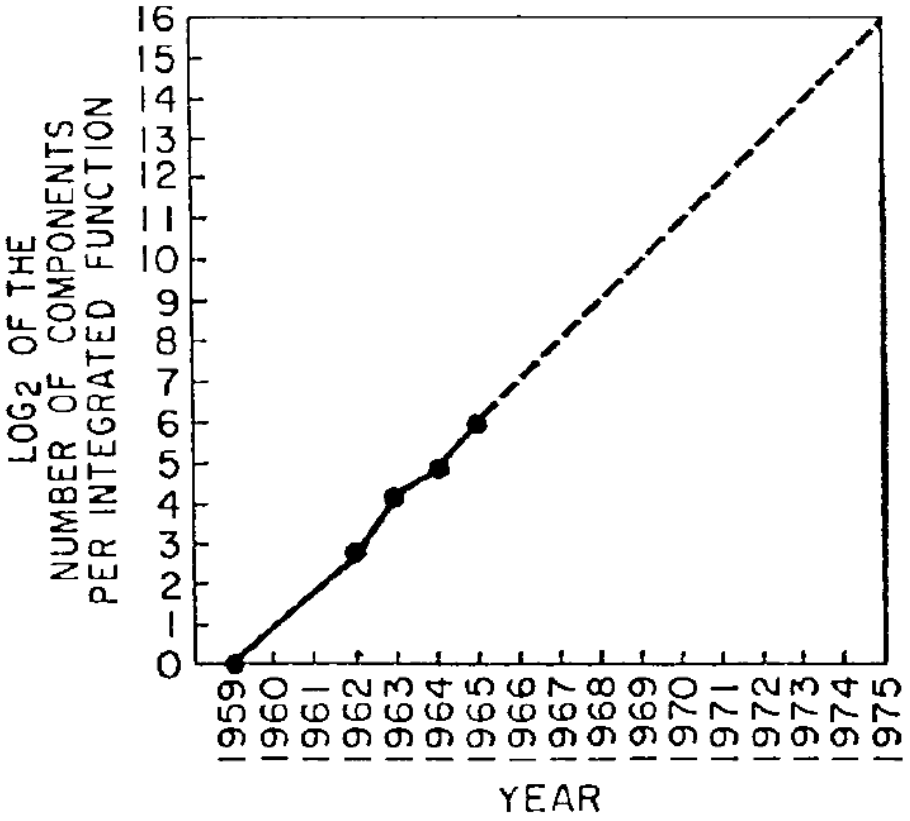
Most companies in the commercial computer field have machines in design or in early production employing integrated electronics. These machines cost less and perform better than those which use "conventional" electronics.

Instruments of various sorts, especially the rapidly increasing numbers employing digital techniques, are starting to use integration because it cuts costs of both manufacture and design.

The use of linear integrated circuitry is still restricted primarily to the military. Such integrated functions are expensive and not available in the variety required to satisfy a major fraction of linear electronics. But the first applications are beginning to appear in commercial electronics, particularly in equipment which needs low-frequency amplifiers of small size.

III. Reliability Counts

In almost every case, integrated electronics has demonstrated high reliability. Even at the present level of pro-



Dennard's Scaling

Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions

ROBERT H. DENNARD, MEMBER, IEEE, FRITZ H. GAENSSLEN, HWA-NIEN YU, MEMBER, IEEE, V. LEO RIDEOUT, MEMBER, IEEE, ERNEST BASSOUS, AND ANDRE R. LEBLANC, MEMBER, IEEE

Classic Paper

This paper considers the design, fabrication, and characterization of very small MOSFET switching devices suitable for digital integrated circuits using dimensions of the order of 1 μ. Scaling relationships are presented which show how a conventional MOSFET can be reduced in size. An improved small device structure is presented that uses ion implantation to provide shallow source and drain regions and a nonuniform substrate doping profile. One-dimensional models are used to predict the substrate doping profile and the corresponding threshold voltage versus source voltage characteristic. A two-dimensional current transport model is used to predict the relative degree of short-channel effects for different device parameter combinations. Polysilicon-gate MOSFET's with channel lengths as short as 0.5 μ were fabricated, and the device characteristics measured and compared with predicted values. The performance improvement expected from using these very small devices in highly miniaturized integrated circuits is projected.

I. List of Symbols

α	Inverse semilogarithmic slope of subthreshold characteristic.
D	Width of idealized step function profile for channel implant.
ΔW_f	Work function difference between gate and substrate.
$\epsilon_{Si}, \epsilon_{ox}$	Dielectric constants for silicon and silicon dioxide.
I_d	Drain current.
k	Boltzmann's constant.
κ	Unitless scaling constant.
L	MOSFET channel length.
μ_{eff}	Effective surface mobility.
n_i	Intrinsic carrier concentration.
N_a	Substrate acceptor concentration.
Ψ_s	Band bending in silicon at the onset of strong inversion for zero substrate voltage.
Ψ_b	Built-in junction potential.
q	Charge on the electron.
Q_{eff}	Effective oxide charge.
t_{ox}	Gate oxide thickness.
T	Absolute temperature.
V_d, V_s, V_g, V_{sub}	Drain, source, gate and substrate voltages.
V_{ds}	Drain voltage relative to source.
V_{s-sub}	Source voltage relative to sustrate.
V_t	Gate threshold voltage.
w_s, w_d	Source and drain depletion layer widths.
W	MOSFET channel width.

This paper is reprinted from IEEE Journal of Solid-State Circuits, vol. SC-9, no. 5, pp. 256–268, October 1974.
Publisher Item Identifier S 0018-9219(99)02196-9.

II. Introduction

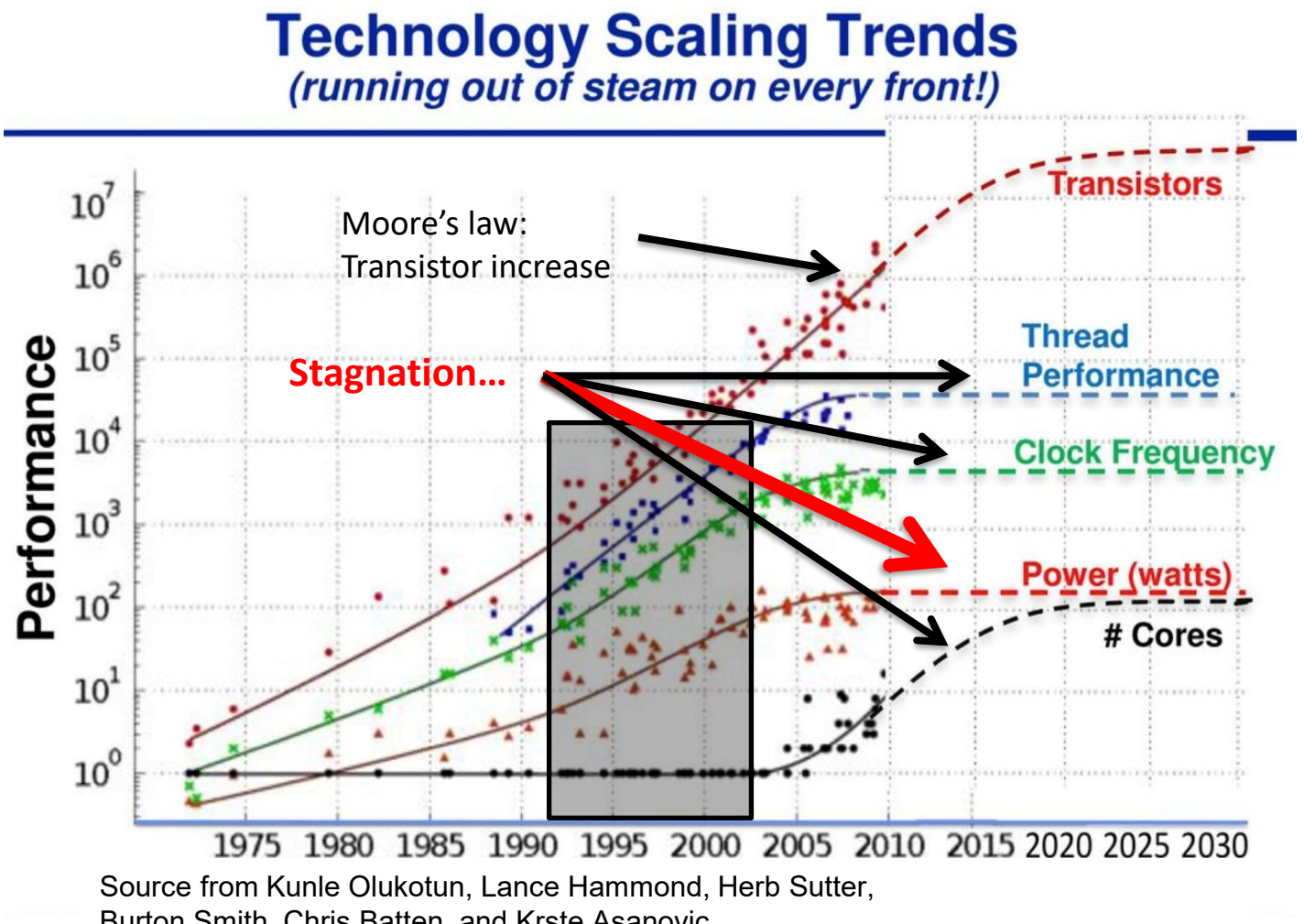
New high resolution lithographic techniques for forming semiconductor integrated circuit patterns offer a decrease in linewidth of five to ten times over the optical contact masking approach which is commonly used in the semiconductor industry today. Of the new techniques, electron beam pattern writing has been widely used for experimental device fabrication [1]–[4] while X-ray lithography [5] and optical projection printing [6] have also exhibited high-resolution capability. Full realization of the benefits of these new high-resolution lithographic techniques requires the development of new device designs, technologies, and structures which can be optimized for very small dimensions.

This paper concerns the design, fabrication, and characterization of very small MOSFET switching devices suitable for digital integrated circuits using dimensions of the order of 1 μ. It is known that reducing the source-to-drain spacing (i.e., the channel length) of an FET leads to undesirable changes in the device characteristics. These changes become significant when the depletion regions surrounding the source and drain extend over a large portion of the region in the silicon substrate under the gate electrode. For switching applications, the most undesirable "short-channel" effect is a reduction in the gate threshold voltage at which the device turns on, which is aggravated

Dennard scaling, states, roughly, that as transistors get smaller their power density stays constant, so that the power use stays in proportion with area: both voltage and current scale (downward) with length.

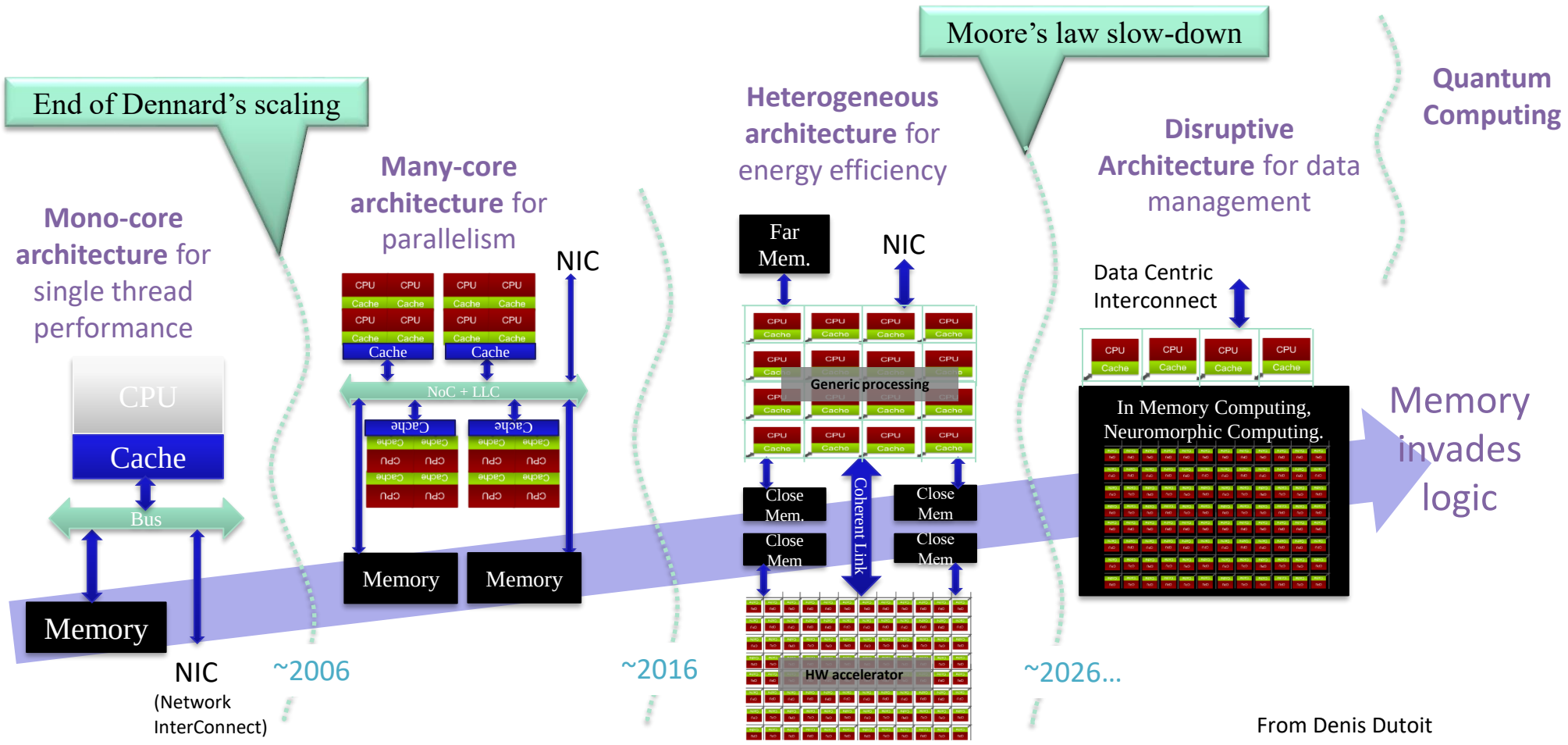
The breakdown of Dennard scaling and resulting inability to increase clock frequencies significantly has caused most CPU manufacturers to focus on multicore processors as an alternative way to improve performance.

Moore 's law and Dennard scaling



Source from Kunle Olukotun, Lance Hammond, Herb Sutter, Burton Smith, Chris Batten, and Krste Asanoviç

Processor architecture evolution



Silicon Roadmap

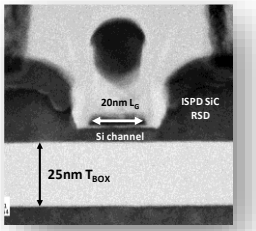
Silicon Quantum bits

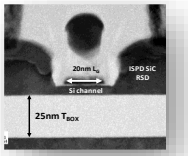
FDSOI

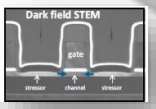
22FD

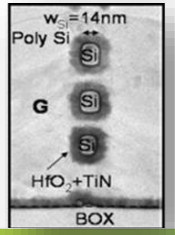
12FD

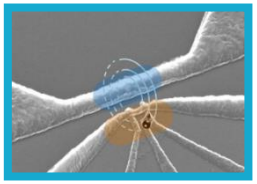
Next Gen











Non planar / trigate / stacked Nanowires

FinFET

28nm

14nm

10nm

2017

2019

7nm

5nm

Disruptive scaling

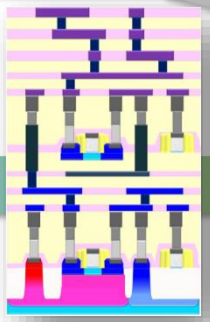
Alternative to scaling and diversification

Hybrid logic

Steep slope devices

Mechanical switches

Si Quantum bits

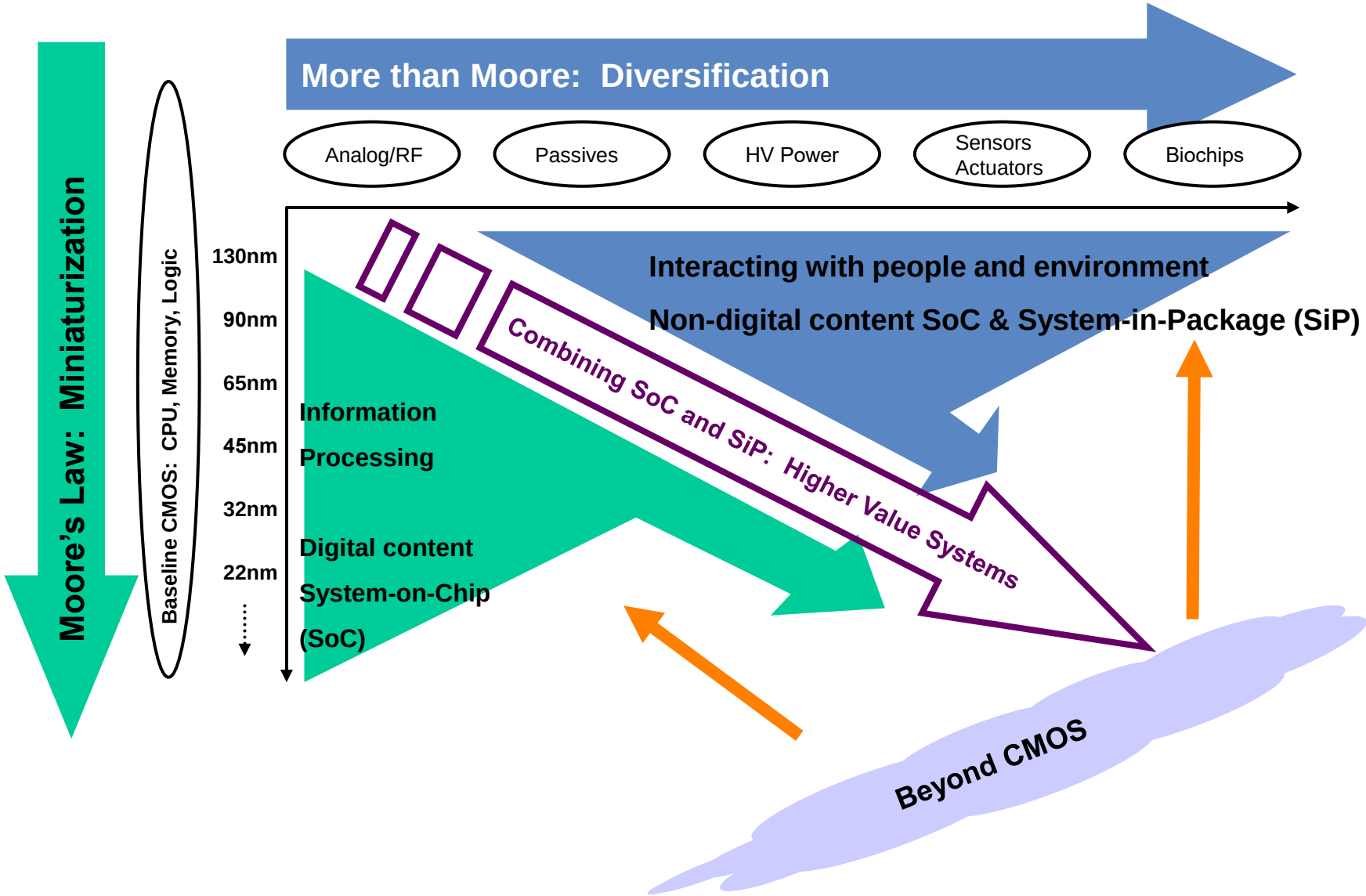


Monolithic 3D for 3D VLSI

Silicon Roadmap

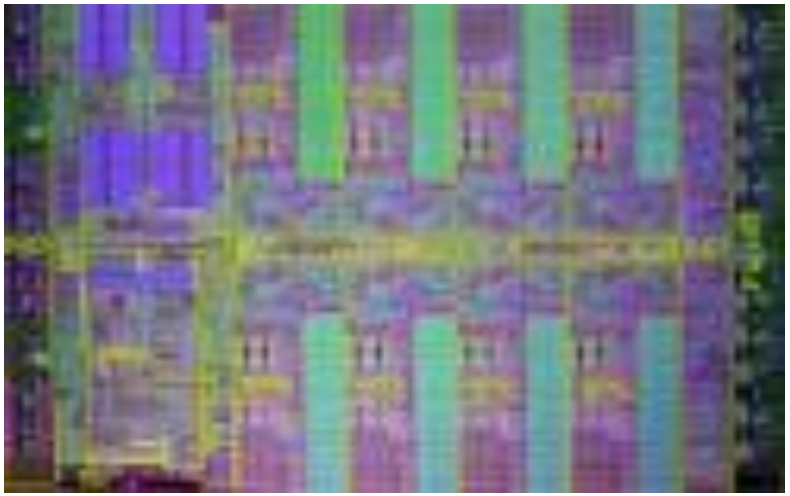
Nominal node		28nm	22nm	20nm	18nm	16nm	14nm	12nm	10nm	7nm	5nm (ITRS)
Intel	Lg		24				20		16	~12nm	10
	Fin Pitch		60 FinFET				FinFET 42		FinFET 34	FinFET	12
	CPP		90				70		54		32
	M1		80				52		36		16
	SRAM		HD 0.092µm2				0.0588µm2		0.0312µm2	0.027µm2	
	Year Publication		VLSI 2012				IEDM 2014		IEDM 2017/ISSCC2018	IEDM 2016	
	Risk Prod		2011				2014		1Q18		
Samsung	Lg	32		25	25		30		~20	~16	
	Fin Pitch	BULK		BULK	FDSOI		48 FinFET		Single Fin 42	Dual thin EUV 27	
	CPP	114		86	86		78		68	54/57	
	M1	90		64	64		64		51	36	
	SRAM	0.152µm2		0.084µm2			0.064/0.08µm2		0.04µm2	HD 6T SRAM 0.026µm2	
	Year Publication	ICSIST 2011		VLSI 2012			JSSC 2014		ISSCC/VLSI 2017	VLSI 2017/ISSCC2017-2018	
	Risk Prod	2011		2013			4Q-2015		1Q2017	2H-18	
TSMC	Lg	30	30	30		33		*25*	~20	~16	
	Fin Pitch	BULK	BULK	BULK		FinFET 45		*FinFET 45*	FinFET	FinFET 4th	
	CPP	118	105	90		90/80		*90/80*	64	57	
	M1	90	80	64		64		*64*	42	40	
	SRAM	0.155µm2	0.155µm2			0.07µm2			0.03µm2	0.027µm2	
	Year Publication	VLSI 2012	VLSI 2012	VLSI 2014		IEDM 2013		*6Track*	VLSI 2016	IEDM 2016	
	Risk Prod	2011	2018	2013		4Q-2015		*3Q2016*	4Q2016	3Q-17	
GF	Lg		28				30				
	Fin Pitch		FDSOI				48 Fin FET				
	CPP		90				78				
	M1		78				67				
	SRAM		0.110µm2				0.110µm2				
	Year Publication		IEDM 2016				IEDM 2016			C.Reita, C.Fenouillet-Beranger - CEA-LETI - 2018	
	Risk Prod		2016				2H-2016				

More Moore and More than Moore domains



Systems on Chip (SoC)

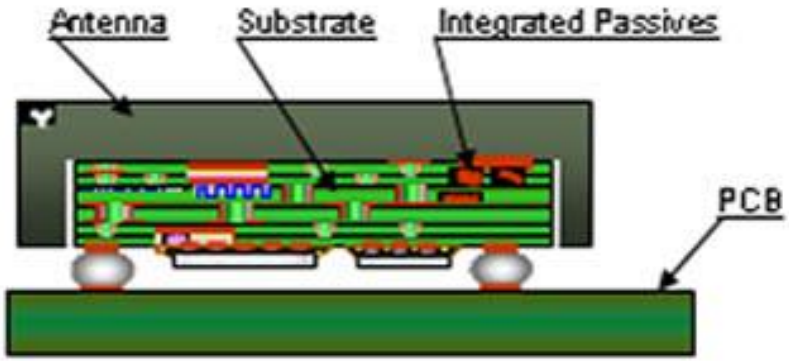
- Large-scale
  - Billion transistor chips
  - Multi-cores, multi-threaded sw
- Power-consumption limited
- Very expensive to design
  - Non recurring engineering costs
  - Migration toward software



IBM Cell Processor

Systems in Package (SiP)

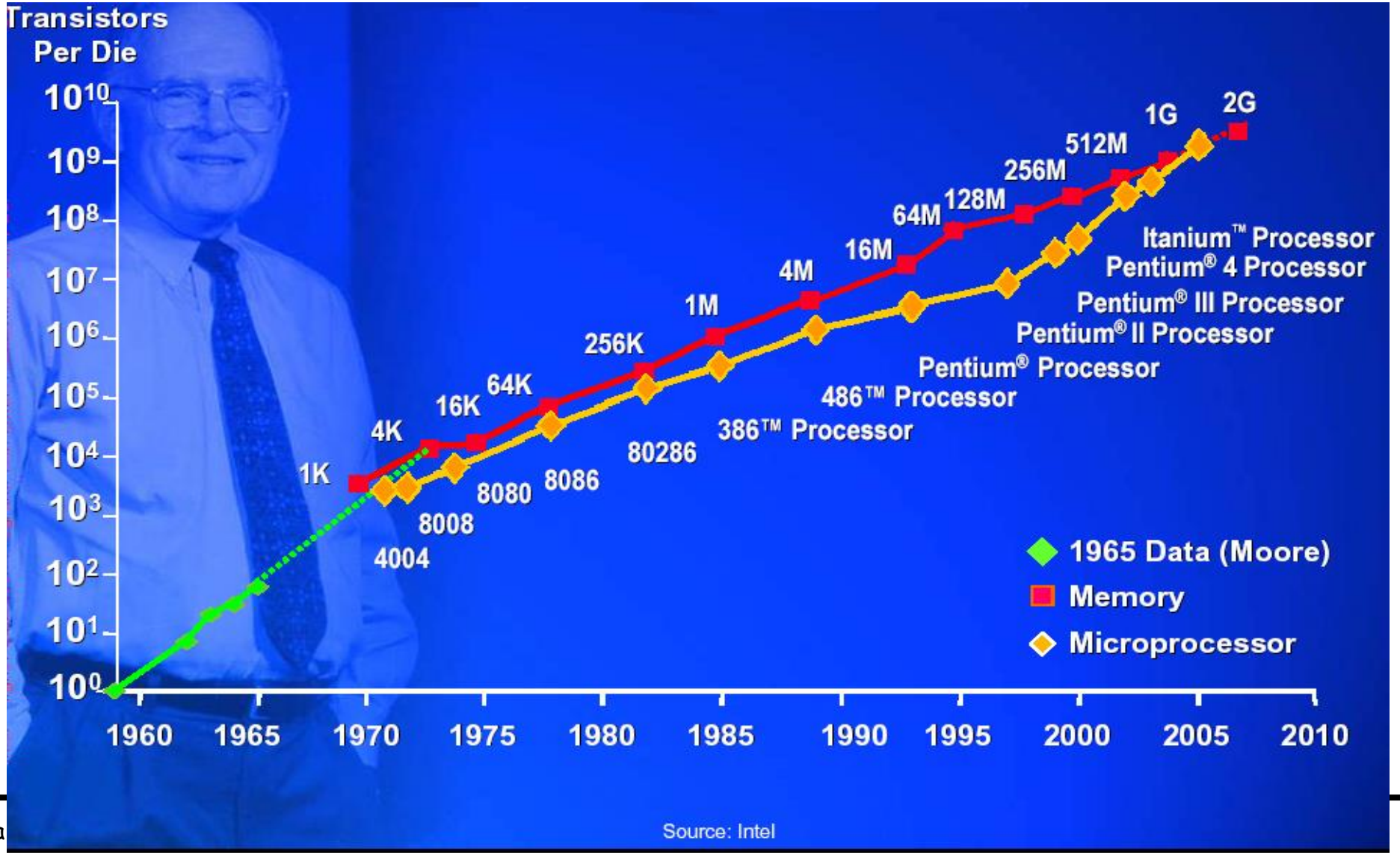
- There is a diminishing return in integrating everything on Si
  - Heterogeneous technologies
  - Multiple voltages
  - Thermal issues
- Packaging technology



Schematic diagram of RF-SIP

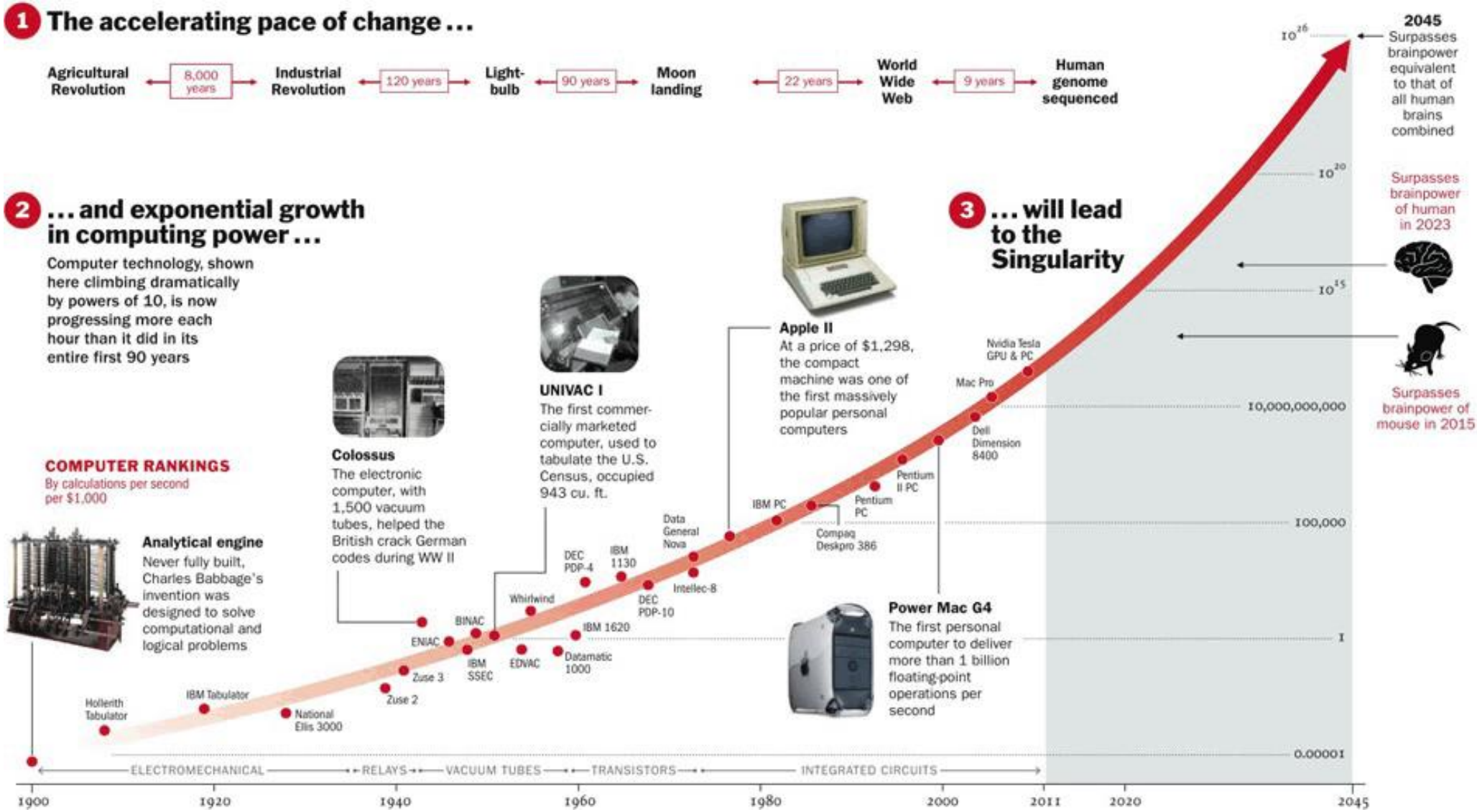
Moore's Law

- Original "law": number of components on IC doubles every year
- Later modified to doubling every 18 months




Home - Museo degli Strumenti p
https://www.msc.sma.unipi.it
Museo degli Strumenti per il Calcolo
Home
Visita
Museo
Educazione Museale
Eventi e news
Gallery
SISTEMA MUSEALE di ATENEO
UNIVERSITÀ DI PISA
MUSEO DEGLI STRUMENTI PER IL CALCOLO

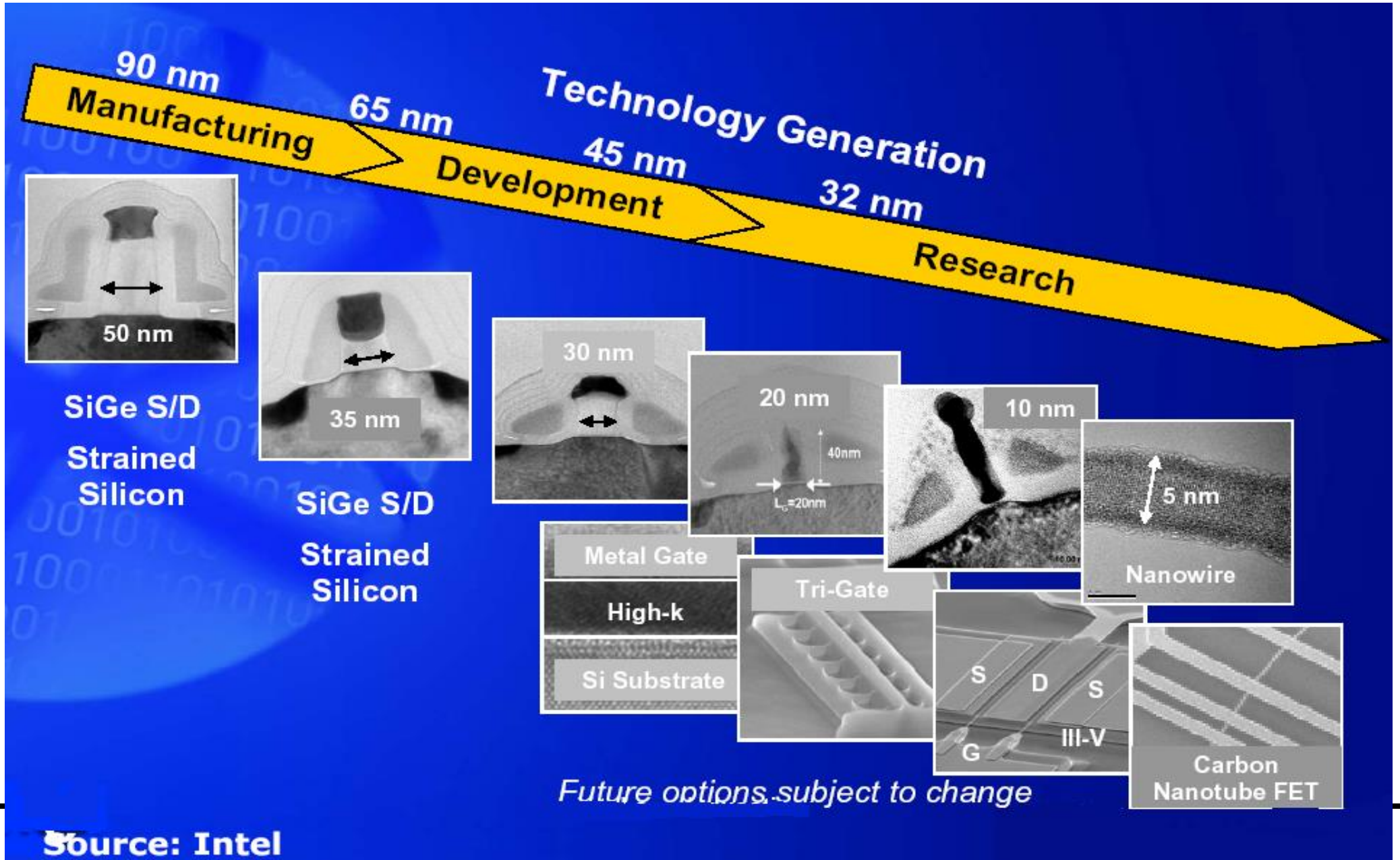
Perspective: In your Lifetime



What is VLSI ?

- Small Scale Integration – 10's of transistors
- Medium Scale Integration – 100's of transistors
- Large Scale Integration – 1000's of transistors
- Very Large Scale Integration 10,000's of transistors
- [Adjectives run out here]

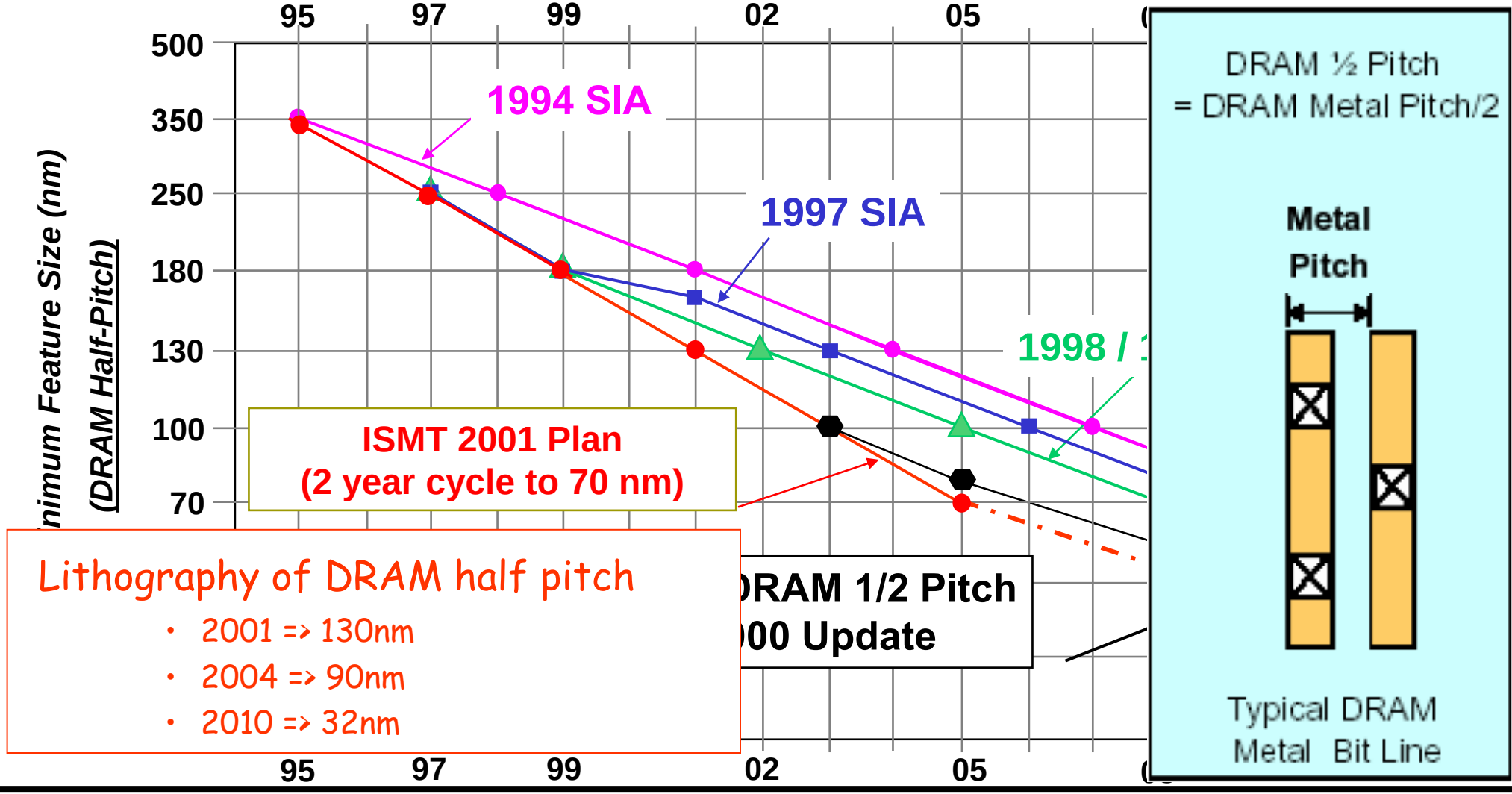
CMOS technology advances



Moore's Law Today

International Technology Roadmap for Semiconductors (ITRS) – 2001

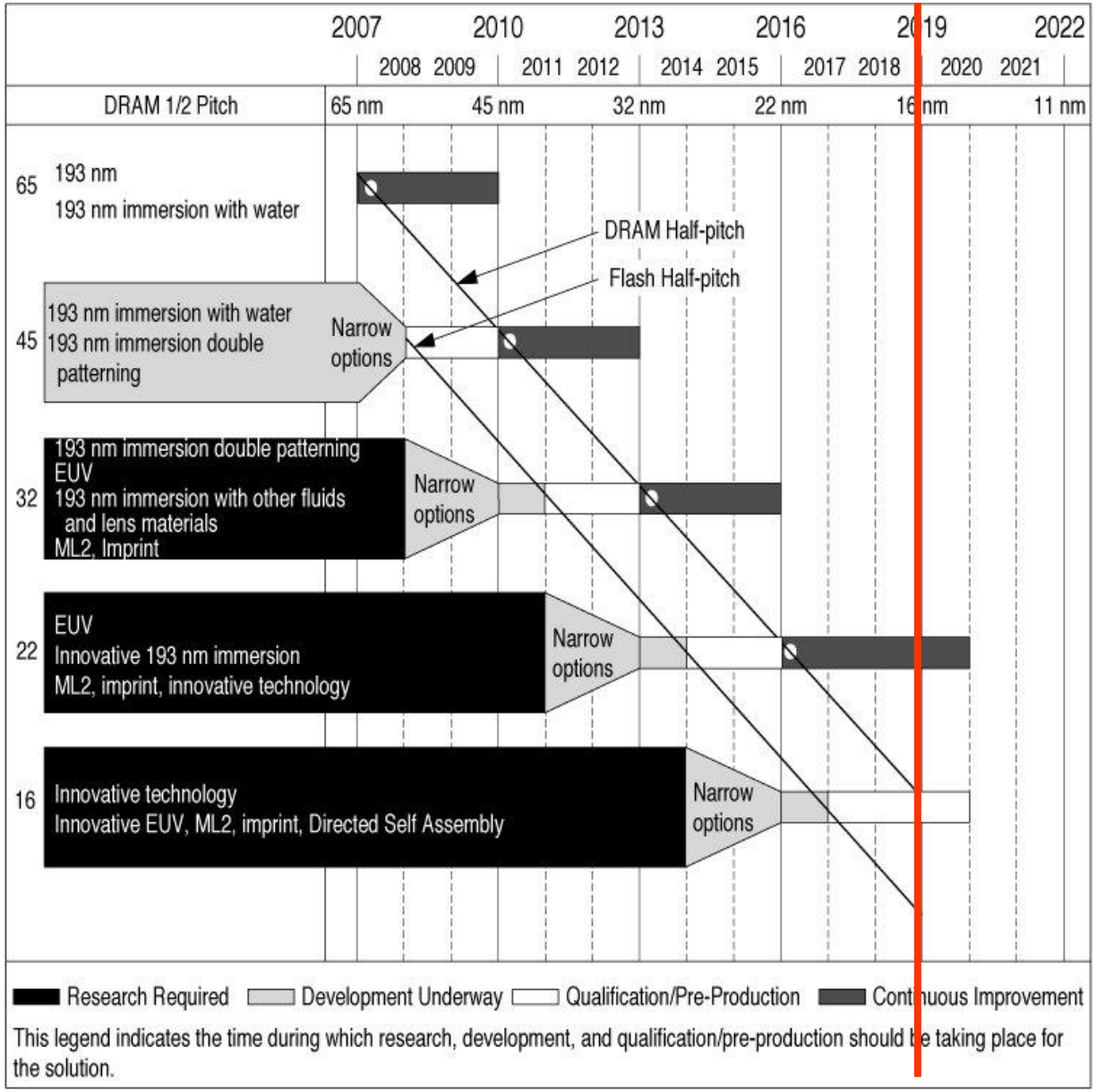
- Projects roadmap for coming years - Defined in terms of "Technology Nodes"

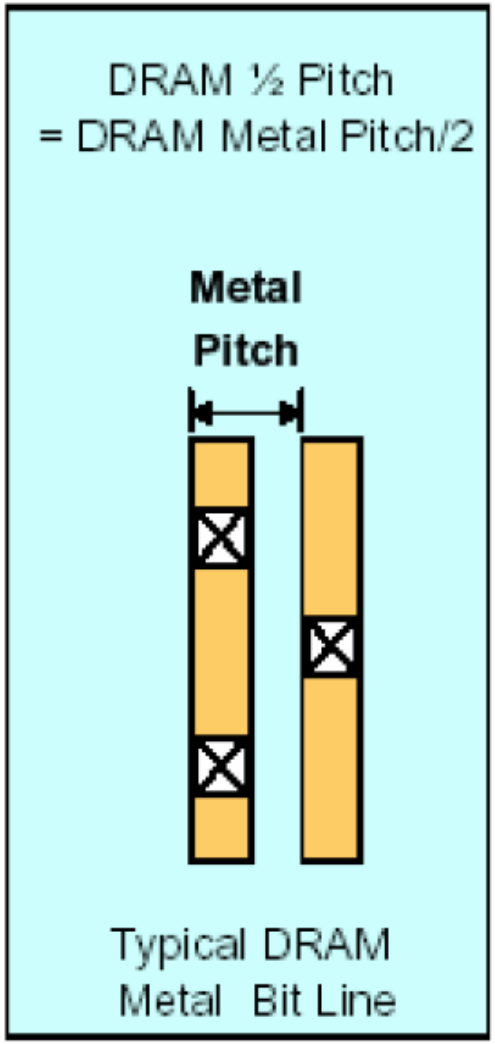


Lithography of DRAM half pitch

- 2001 => 130nm
- 2004 => 90nm
- 2010 => 32nm

ITRS Roadmap





How much could we put on a chip?

	2001	2013
Reticle size (mm)	25 x 32	22 x 26
Maximum die size (mm^2)	800	572
Feature size F/λ (μm)	0.13	0.032
Maximum die size (λ^2)	47,000,000,000	559,000,000,000
2-input NAND gates per die ($300\lambda^2$)	158,000,000	1,862,000,000
DRAM cells per die ($8F^2$)	6Gb	70Gb

- An incredible number of gates
- Caveat: these are upper bounds
  - Die this big don't yield well (if at all)
  - $300\lambda^2$ NAND-2 gate is minimum size
  - DRAM cell efficiency is only about 50%

- One 12 inch DRAM wafer in 2013 will contain about 4 trillion bits (!)

Perspective: In your Lifetime

- Cray-1: world's fastest computer 1976-1982
  - 64Mb memory (50ns cycle time)
  - 40Kb register (6ns cycle time)
  - ~1 million gates (4/5 input NAND)
  - 80MHz clock
  - 115kW
- In 0.13μ technology
  - 64Mb => 17mm^2
  - 1 million NAND-4 gates => 8.5mm^2

Good news, but…

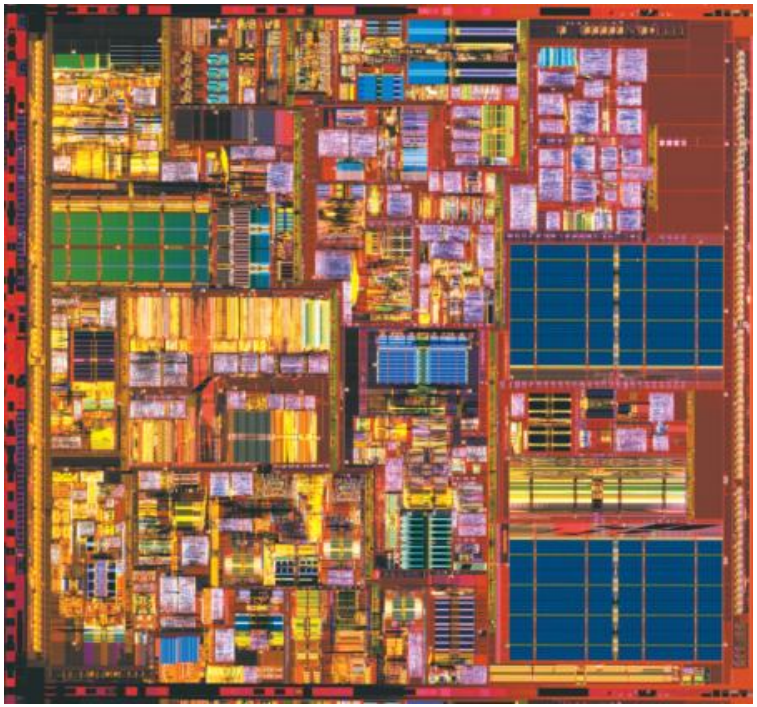
- Things getting worse with each generation:
  - Complexity
  - Power consumption
  - Power distribution
  - Signal integrity
  - Fabrication time
  - Capital costs for equipment
  - Fixed costs for masks
  - Variable costs for wafers
- How do we handle these for a device with 100M gates?

Three examples to cope with this complexity

- Standard Processor
- FPGA Approach
- Custom ASIC
- .....
- .....

One method of Coping: Use A Standard Processor

- Pros:
  - Intel and AMD have giant design teams – leverage them
  - Cost of large support infrastructure spread over huge user community
- Cons:
  - Fixed instruction set and datapath



Intel Pentium 4

0.13μ process

55 million transistors

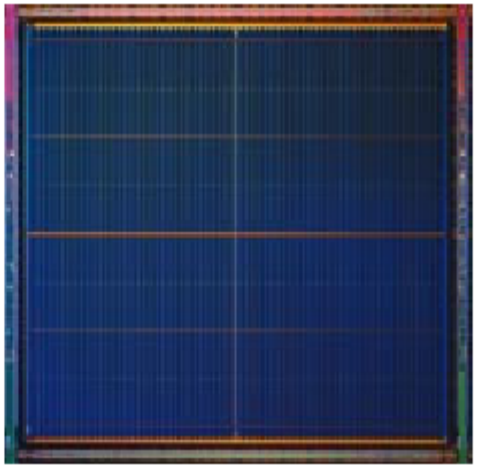
2.4GHz clock

145mm^2

source : Chipworks

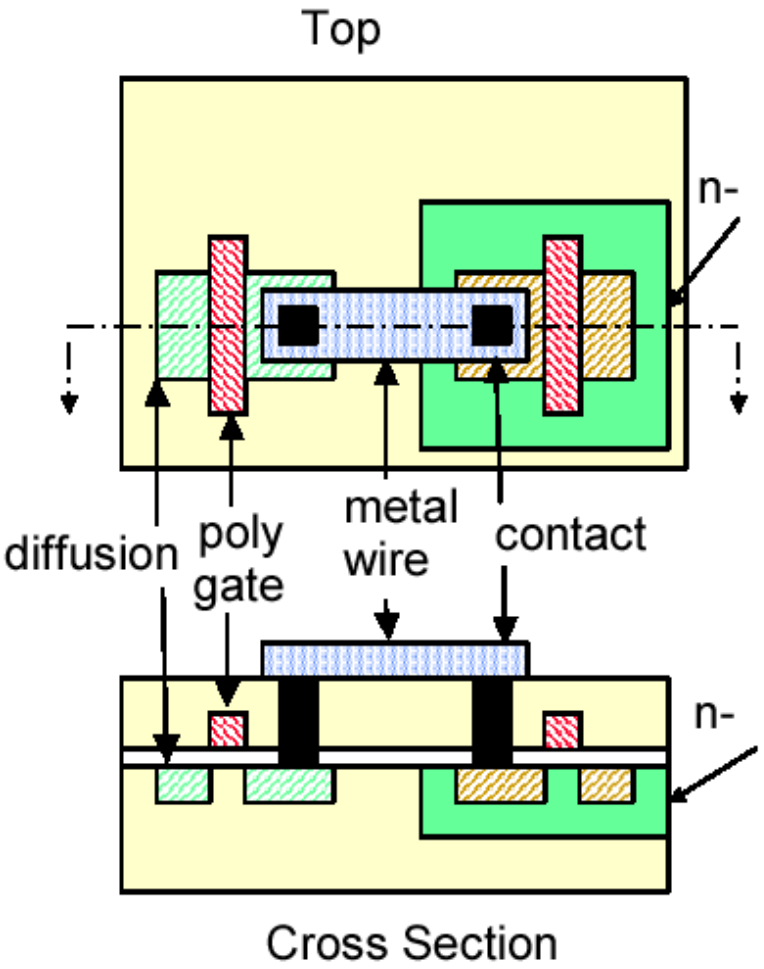
Another method of Coping: Using FPGA

- Logic pre-fabricated with reconfigurable interconnect
- Pros:
  - Very fast turnaround, easier to fix mistakes
  - Configurations for often used functions readily available
- Cons:
  - Practical number of usable gates is about 1 million at 0.13μ
    - Reaching a clock frequency of 150MHz is doing good
    - Power is typically 3x that of comparable Application Specific IC (ASIC)



Rolling Your Own ASIC

- Process is deceptively simple – Similar to printing or photography
- Choose a fabrication company ("fab")
- Produce a set of negatives ("masks") describing your chip
  - A set of four negatives for transistors
  - 2 negatives per layer of wiring
- Send negatives and $$$ to fab
- Wait 2-3 months for fabrication
- Package and test chips



The Hard Part

- The previous example had eight polygons and two transistors
- A real design will have at least 1 million polygons and 100K transistors
- Mistakes are really expensive
  - A full set of masks for 0.13μ is about $600,000
- Any single error in any of the polygons can ruin the chip
- No one person can really comprehend 1 million of anything
  - much less 1 billion
- Need to attack the problem with the standard engineering tools
  - Hierarchy and abstraction
  - Design reuse
  - Computer automation

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End, Questions ?

- What is an integrated circuit ?
- What is VLSI ?
- VLSI Technology Trends