RF_DFlipFlop

Created	@October 11, 2024 3:37 PM
Tags	
Status	Not started

Test Case	Clock (CLK)	Reset	D	Q (next state)	Description
1	Rising edge	1	X	0	Reset active, Q is reset to 0
2	Rising edge	0	X	Q (unchanged)	Reset deactivated, Q holds its value
3	Rising edge	0	1	1	D is set to 1, Q follows D
4	Rising edge	0	0	0	D is set to 0, Q follows D
5	Rising edge	0	1	1	D is set to 1, Q follows D
6	Rising edge	0	0	0	D is set to 0, Q follows D