CSU22022 Computer Architecture I

Prof. Michael Manzke

Full Processor Project 1ˢᵗ Instalment

Checklist

30ᵗʰ October 2024

Version 1.0

All files must be submitted to Blackboard as individual files, no zip files. Submit only entities that are working and are fully tested. You must follow the entity order on the checklist. You cannot skip entities.

The entities must be programmed and tested in the following order. Please confirm by ticking all the boxes next the items that all required files are available on Blackboard and that the entity is fully working.   You must print this checklist, tick the boxes, sign it, and submit it to Blackboard.

All files must be submitted in the checklist order:

> RF_Mux3_1Bit_XXXXXXXX.vhd
> RF_Mux3_1Bit_XXXXXXXX_TB.vhd
> RF_Mux3_1Bit_XXXXXXXX_SchematicXX.pdf
> RF_Mux3_1Bit_XXXXXXXX_TDXX.png
> RF_Mux3_1Bit_XXXXXXXX_Doc. txt (can be any file format)
> RF_Mux3_32Bit_XXXXXXXX.vhd
> RF_Mux3_32Bit_XXXXXXXX_TB.vhd
> RF_Mux3_32Bit_XXXXXXXX_SchematicXX.pdf
> RF_Mux3_32Bit_XXXXXXXX_TDXX.png
> RF_Mux3_32Bit_XXXXXXXX_Doc.txt (can be any file format)
>
> -
> -
> -

0	My submission complies with the "Instructions for the Blackboard Submission of the Assignment" (CSU22022 Full Processor Project 1st Instalment 2024-2025 Instruction V1.0.pdf)	y

1	RF_Mux3_1Bit_XXXXXXXX.vhd	y
	RF_Mux3_1Bit_XXXXXXXX_TB.vhd	y
	RF_Mux3_1Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux3_1Bit_XXXXXXXX_TDXX.png	y
	RF_Mux3_1Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

2	RF_Mux3_32Bit_XXXXXXXX.vhd	y
	RF_Mux3_32Bit_XXXXXXXX_TB.vhd	y
	RF_Mux3_32Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux3_32Bit_XXXXXXXX_TDXX.png	y
	RF_Mux3_32Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

3	RF_Mux16_1Bit_XXXXXXXX.vhd	y
	RF_Mux16_1Bit_XXXXXXXX_TB.vhd	y
	RF_Mux16_1Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux16_1Bit_XXXXXXXX_TDXX.png	y
	RF_Mux16_1Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

4	RF_Mux16_32Bit_XXXXXXXX.vhd	y
	RF_Mux16_32Bit_XXXXXXXX_TB.vhd	y
	RF_Mux16_32Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux16_32Bit_XXXXXXXX_TDXX.png	y
	RF_Mux16_32Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

5	RF_Mux32_1Bit_XXXXXXXX.vhd	y
	RF_Mux32_1Bit_XXXXXXXX_TB.vhd	y
	RF_Mux32_1Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux32_1Bit_XXXXXXXX_TDXX.png	y
	RF_Mux32_1Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

6	RF_Mux32_32Bit_XXXXXXXX.vhd	y
	RF_Mux32_32Bit_XXXXXXXX_TB.vhd	y
	RF_Mux32_32Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux32_32Bit_XXXXXXXX_TDXX.png	y
	RF_Mux32_32Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

7	RF_DFlipFlop_XXXXXXXX.vhd	y
	RF_DFlipFlop_XXXXXXXX_TB.vhd	y
	RF_DFlipFlop_XXXXXXXX_SchematicXX.pdf	y
	RF_DFlipFlop_XXXXXXXX_TDXX.png	y
	RF_DFlipFlop_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

8	RF_Register32Bit_XXXXXXXX.vhd	y
	RF_Register32Bit_XXXXXXXX_TB.vhd	y
	RF_Register32Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Register32Bit_XXXXXXXX_TDXX.png	y
	RF_Register32Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

9	RF_DestReg_Decoder_XXXXXXXX.vhd	y
	RF_DestReg_Decoder_XXXXXXXX_TB.vhd	y
	RF_DestReg_Decoder_XXXXXXXX_SchematicXX.pdf	y
	RF_DestReg_Decoder_XXXXXXXX_TDXX.png	y
	RF_DestReg_Decoder_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

10	RF_TempDestReg_Decoder_XXXXXXXX.vhd	y
	RF_TempDestReg_Decoder_XXXXXXXX_TB.vhd	y
	RF_TempDestReg_Decoder_XXXXXXXX_SchematicXX.pdf	y
	RF_TempDestReg_Decoder_XXXXXXXX_TDXX.png	y
	RF_TempDestReg_Decoder_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

11	RF_RegisterFile_32_15_XXXXXXXX.vhd	y
	RF_RegisterFile_32_15_XXXXXXXX_TB.vhd	y
	RF_RegisterFile_32_15_XXXXXXXX_SchematicXX.pdf	y
	RF_RegisterFile_32_15_XXXXXXXX_TDXX.png	y
	RF_RegisterFile_32_15_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

12	RF_Test_RegisterFile_32_15_XXXXXXXX.vhd	y
	RF_Test_RegisterFile_32_15_XXXXXXXX_TB.vhd	y
	RF_Test_RegisterFile_32_15_XXXXXXXX_SchematicXX.pdf	y
	RF_Test_RegisterFile_32_15_XXXXXXXX_TDXX.png	y
	RF_Test_RegisterFile_32_15_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

| 13 | Processor_XXXXXXXX.srcs (including all subdirectories and files) | y |
| | Processor_XXXXXXXX.xpr | y |

Student Name: Emma Burgess

Student ID: 22336157

29/11/24   Emma Burgess

Date   Signature