Register File

Created	@October 15, 2024 11:29 AM
Tags	
Status	Not started

Test Case	RW	DR	D	SA	SB	TD	Reset	A (Expected)	B (Expected)
0	0	00000	00000001010101001101001010011101	00001	00001	0000	0	00000001010101001101001010011101	00000001010101001101001
1	0	00001	00000001010101001101001010011110	00001	00001	0000	0	00000001010101001101001010011110	00000001010101001101001
2	0	00010	00000001010101001101001010011111	00010	00010	0000	0	00000001010101001101001010011111	00000001010101001101001
3	0	00011	00000001010101001101001010100000	00011	00011	0000	0	00000001010101001101001010100000	00000001010101001101001
4	0	00100	00000001010101001101001010100001	00100	00100	0000	0	00000001010101001101001010100001	00000001010101001101001
...	..	..	..	..	..	..	..	..	..
31	0	11111	00000001010101001101001010111100	11111	11111	0000	0	00000001010101001101001010111100	00000001010101001101001
32	0	00000	00000001010101001101001010111110	00000	00000	0001	0	00000001010101001101001010111110	00000001010101001101001
33	0	00000	00000001010101001101001010111111	00000	00000	0010	0	00000001010101001101001010111111	00000001010101001101001
...	..	..	..	..	..	..	..	..	..

1. Each test case corresponds to a write operation to a specific register followed by a read operation.
2. The table can be expanded for all 38 test cases, adding one to the binary DR, SA&SB / TD
3. The reset value resets all register outputs to 0, so when **Reset** is asserted (active low), all register outputs should be zeros until the next write operation is performed.
4. The clock signal is not shown in the table but is necessary for synchronising the operations.