CSU22022 Computer Architecture I

Prof. Michael Manzke

Full Processor Project 1st Instalment

Checklist

4th November 2024

Version 2.0

Checklist for the submission of the Full Processor Project 2nd Instalment. Please don't submit these files but confirm that all entities from the 1st Instalment are tested and working.

1	RF_Mux3_1Bit_XXXXXXXX.vhd	y
	RF_Mux3_1Bit_XXXXXXXX_TB.vhd	y
	RF_Mux3_1Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux3_1Bit_XXXXXXXX_TDXX.png	y
	RF_Mux3_1Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

2	RF_Mux3_32Bit_XXXXXXXX.vhd	y
	RF_Mux3_32Bit_XXXXXXXX_TB.vhd	y
	RF_Mux3_32Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux3_32Bit_XXXXXXXX_TDXX.png	y
	RF_Mux3_32Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

3	RF_Mux16_1Bit_XXXXXXXX.vhd	y
	RF_Mux16_1Bit_XXXXXXXX_TB.vhd	y
	RF_Mux16_1Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux16_1Bit_XXXXXXXX_TDXX.png	y
	RF_Mux16_1Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

4	RF_Mux16_32Bit_XXXXXXXX.vhd	y
	RF_Mux16_32Bit_XXXXXXXX_TB.vhd	y
	RF_Mux16_32Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux16_32Bit_XXXXXXXX_TDXX.png	y
	RF_Mux16_32Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

5	RF_Mux32_1Bit_XXXXXXXX.vhd	y
	RF_Mux32_1Bit_XXXXXXXX_TB.vhd	y
	RF_Mux32_1Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux32_1Bit_XXXXXXXX_TDXX.png	y
	RF_Mux32_1Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

6	RF_Mux32_32Bit_XXXXXXXX.vhd	y
	RF_Mux32_32Bit_XXXXXXXX_TB.vhd	y
	RF_Mux32_32Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Mux32_32Bit_XXXXXXXX_TDXX.png	y
	RF_Mux32_32Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

7	RF_DFlipFlop_XXXXXXXX.vhd	y
	RF_DFlipFlop_XXXXXXXX_TB.vhd	y
	RF_DFlipFlop_XXXXXXXX_SchematicXX.pdf	y
	RF_DFlipFlop_XXXXXXXX_TDXX.png	y
	RF_DFlipFlop_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

8	RF_Register32Bit_XXXXXXXX.vhd	y
	RF_Register32Bit_XXXXXXXX_TB.vhd	y
	RF_Register32Bit_XXXXXXXX_SchematicXX.pdf	y
	RF_Register32Bit_XXXXXXXX_TDXX.png	y
	RF_Register32Bit_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

9	RF_DestReg_Decoder_XXXXXXXX.vhd	y
	RF_DestReg_Decoder_XXXXXXXX_TB.vhd	y
	RF_DestReg_Decoder_XXXXXXXX_SchematicXX.pdf	y
	RF_DestReg_Decoder_XXXXXXXX_TDXX.png	y
	RF_DestReg_Decoder_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

10	RF_TempDestReg_Decoder_XXXXXXXX.vhd	y
	RF_TempDestReg_Decoder_XXXXXXXX_TB.vhd	y
	RF_TempDestReg_Decoder_XXXXXXXX_SchematicXX.pdf	y
	RF_TempDestReg_Decoder_XXXXXXXX_TDXX.png	y
	RF_TempDestReg_Decoder_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

11	RF_RegisterFile_32_15_XXXXXXXX.vhd	y
	RF_RegisterFile_32_15_XXXXXXXX_TB.vhd	y
	RF_RegisterFile_32_15_XXXXXXXX_SchematicXX.pdf	y
	RF_RegisterFile_32_15_XXXXXXXX_TDXX.png	y
	RF_RegisterFile_32_15_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

12	RF_Test_RegisterFile_32_15_XXXXXXXX.vhd	y
	RF_Test_RegisterFile_32_15_XXXXXXXX_TB.vhd	y
	RF_Test_RegisterFile_32_15_XXXXXXXX_SchematicXX.pdf	y
	RF_Test_RegisterFile_32_15_XXXXXXXX_TDXX.png	y
	RF_Test_RegisterFile_32_15_XXXXXXXX_Doc.tex (can be any file format)	y
	Is working	y

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Date Signature