CA Project **2** Report, Team 25

Members

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Team Work

We coded together by a collaborative online editor, HackMD, Each of us implemented a part of d_cache_top.v, then connected the modules with wires in CPU.v synchronously. While debugging, 賴楷宗 looked for differences between our outputs("output.txt" and "cache.txt") and TA's, then checked the state by gtkwave; After discussing about the error, 林日能 and 邱綜樹 were responsible for correcting the code.

Implementation

In order to be in coordinate with the pipelined CPU in our last project (which pipeline was shifted at negative edges of clock), several modules need to change their response condition. Our dcache_top.v, dcache_data_sram.v, dcache_tag_sram.v and DataMemory.v also update their values at negative edge. But DataMemory.v still writes at positive edge.

Cache Controller in detail
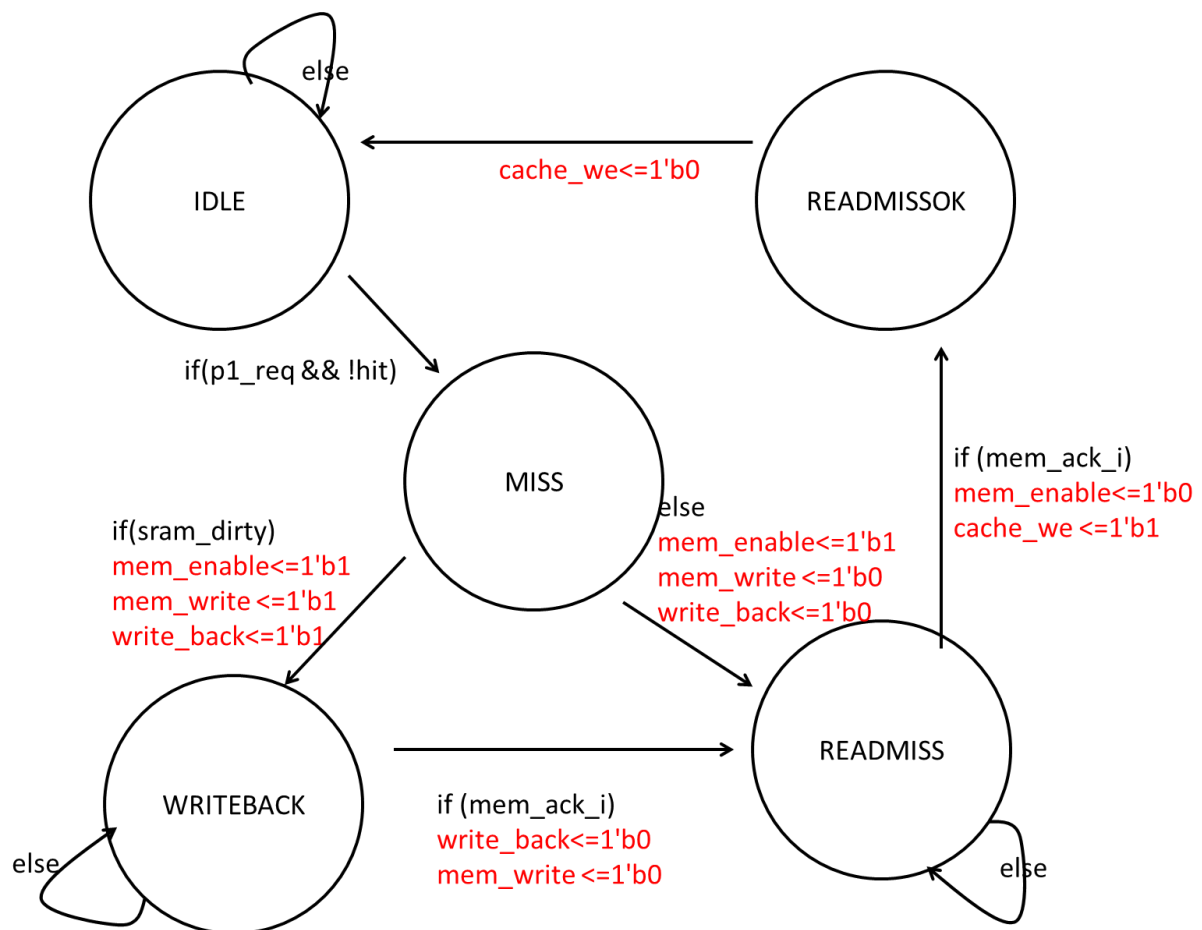
Problems and solution of this project

1. **Problem :** If I connect A module's output to B module's input directly, there is some value lost (e.g. A's output = 10, but B's input = x)
    Solution : create a wire between A & B. (Even though I am not use this solution at somewhere, there aren't any value lost at that point. So it's a bit weird…)

2. **Problem:** There is no "Write Miss" and "Read Miss" occurred in our cache.txt.
    Solution: We found that it is because our dcache updates values at positive edge (which is the TA's implementation), so we change it to be in coordinate with our last project (update values at negative edge). Then all the incoordination between our output and TA's vanished.

3. **Problem:** We tried to use a for loop, but the loop is endless.
    Solution: For Example - for(a = start ; a >= end ; a = a - 1) { ... }But our start & end are not integer, they are 8-bit wire(or reg (?)). As a result, when comparing a with end, there are weird bugs s.t. continuous decreasing occurred. Finally, we assign raw result of start & end to two integers, then add to respective place in for-loop AND SOLVE THE ISSUE!!!