**MSoC Self-paced 2: PP4FPGA FIR**

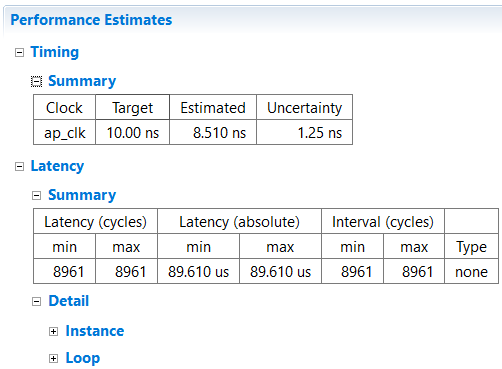
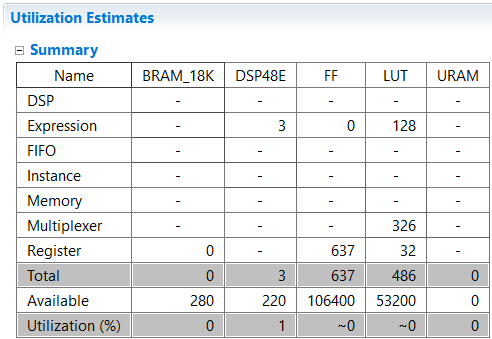
**R08943011 黃文璁**

* **[v] HLS C-sim/synthesis/cosim**
* **[v] System bring-up (zedboard)**
* **[v] Improvement (latency, area)**
* **[v] Github:** [**https://github.com/b04901060/MSoC-Application-Acceleration-with-High-Level-Synthesis**](https://github.com/b04901060/MSoC-Application-Acceleration-with-High-Level-Synthesis)

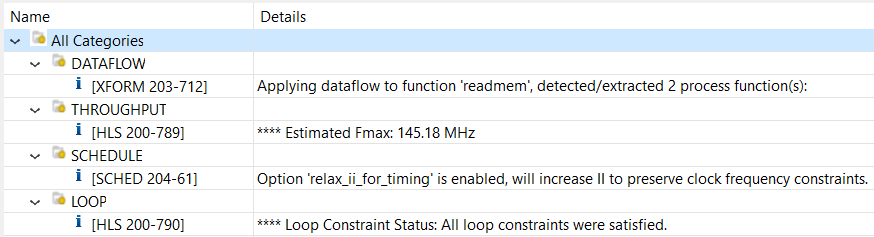
1. **Introduction**

本example實作有限脈衝響應 (finite impulse response) 濾波器，輸入訊號和對應的 tap 參數相乘後累加得到輸出。

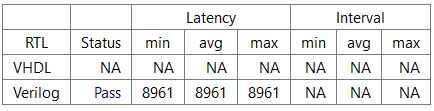
1. **C Synthesis and cosim**

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另外可以注意到合成結果沒有warning：



**Cosim:**

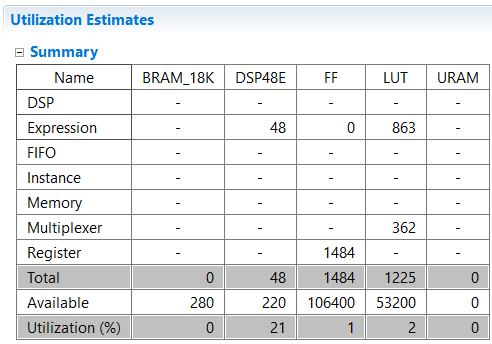
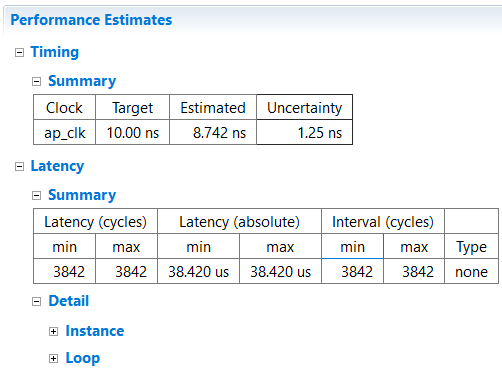


**-> Verilog pass**

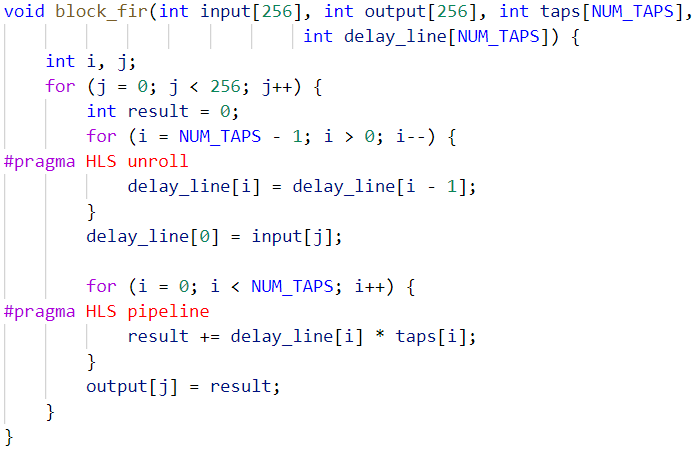
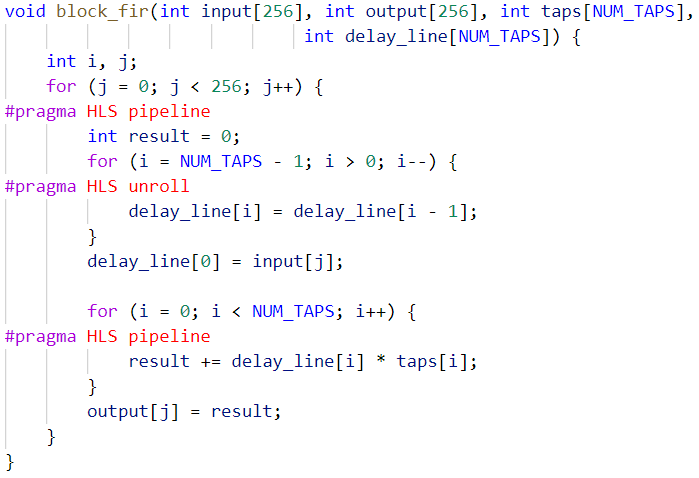
1. **Optimization**

在原版中的雙層迴圈只在最內層的迴圈加上 PIPELINE pragma，我的版本中再於外圈loop加上PIPELINE指令，以達到更低的latency，但便需要更多FPGA resource，在area和performance間做tradeoff。

* + **Latency optimized synthesis result**

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* + **Latency**: 8961 -> 3842 (**-57%**)
  + **FF**: 637 -> 1484 (**+133%**)
  + **LUT**: 486 -> 1225 (**+152%**)

**Before After**

1. **Block Diagram**