LAB05_312651057

吳鴻明

實驗目的

使single port memory 完成 dual port memory 的事情，諸如讀取與寫入，而本實驗需完成同時讀取與寫入的功能。

實驗程式碼

RAM_bg.v A

RAM_bg.v

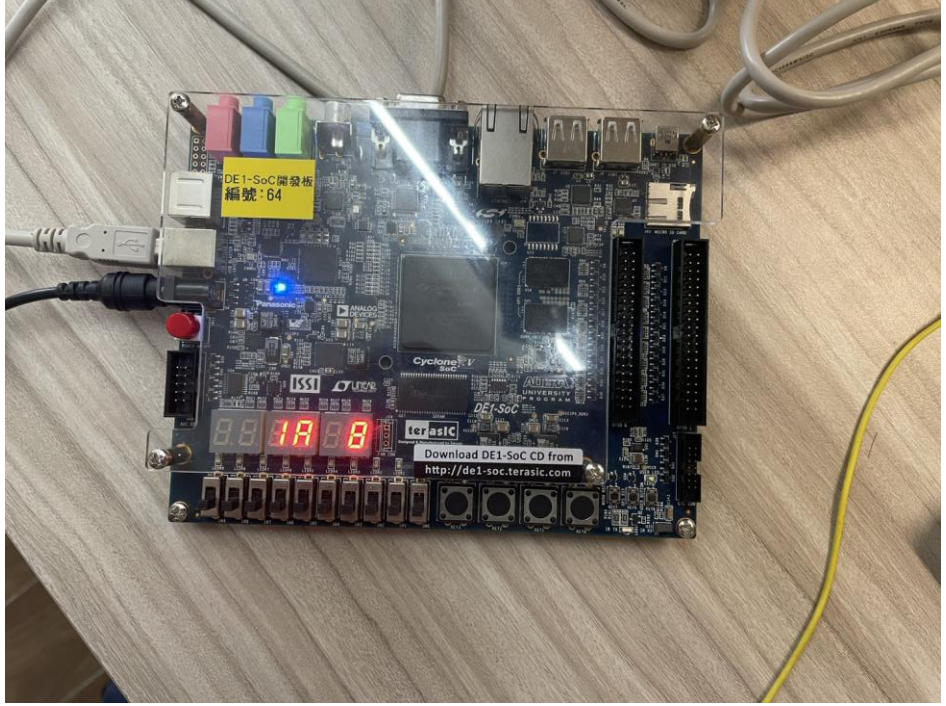
```
1  module RAM(input CLOCK_50,
2             input [9:0] SW,
3             output  [9:0]LEDR,
4             output reg [6:0]HEX0,HEX2,HEX3);
5
6
7  reg clk_slow;
8  reg[26:0]sys_cnt;
9  reg[4:0]addr;
10 reg [3:0]data_tmp[31:0];
11
12 wire [3:0]data;
13
14 ram_test u1 (
15     .address(SW[4:0]),
16     .clock(CLOCK_50),
17     .data(SW[8:5]),
18     .wren(SW[9]),
19     .q(data));
20
21 assign LEDR[0] = (SW[9])?1'b1:1'b0;
22
23
24
25
26 always@(posedge CLOCK_50)begin
27     if(sys_cnt <50000000)begin
28         sys_cnt <= sys_cnt + 26'b1;
29         clk_slow <= 1'b0;
30         if (SW[9]) begin
31             data_tmp[SW[4:0]] <= data;
32         end
33     end
34     else begin
35         sys_cnt <= 26'b0;
36         clk_slow <= ~clk_slow;
37     end
38 end
39
40 always@(posedge clk_slow)begin
41     addr <= (addr == 5'd31)? 5'd0 : addr + 5'd1;
42 end
43
44
45 always@(*)begin
46     case(addr[3:0])
47         5'd1: HEX2 = 7'b1111001;
48         5'd2: HEX2 = 7'b0100100;
```

RAM_bg.v A

RAM_bg.v

```
45  always@(*)begin
46      case(addr[3:0])
51          5'd5: HEX2 = 7'b0010010;
52          5'd6: HEX2 = 7'b0000010;
53          5'd7: HEX2 = 7'b1011000;
54          5'd8: HEX2 = 7'b0000000;
55          5'd9: HEX2 = 7'b0011000;
56          5'd10: HEX2 = 7'b0001000;
57          5'd11: HEX2 = 7'b0000011;
58          5'd12: HEX2 = 7'b1000110;
59          5'd13: HEX2 = 7'b0100001;
60          5'd14: HEX2 = 7'b0000110;
61          5'd15: HEX2 = 7'b0001110;
62          default: HEX2 = 7'b1000000;
63      endcase
64  end
65
66  always@(*)begin
67      case(addr[4])
68          1'b0: HEX3 = 7'b1000000;
69          1'b1: HEX3 = 7'b1111001;
70          default: HEX3 = 7'b1000000;
71      endcase
72  end
73
74  always@(*)begin
75      case(data_tmp[addr])
76          5'd1: HEX0 = 7'b1111001;
77          5'd2: HEX0 = 7'b0100100;
78          5'd3: HEX0 = 7'b0110000;
79          5'd4: HEX0 = 7'b0011001;
80          5'd5: HEX0 = 7'b0010010;
81          5'd6: HEX0 = 7'b0000010;
82          5'd7: HEX0 = 7'b1011000;
83          5'd8: HEX0 = 7'b0000000;
84          5'd9: HEX0 = 7'b0011000;
85          5'd10: HEX0 = 7'b0001000;
86          5'd11: HEX0 = 7'b0000011;
87          5'd12: HEX0 = 7'b1000110;
88          5'd13: HEX0 = 7'b0100001;
89          5'd14: HEX0 = 7'b0000110;
90          5'd15: HEX0 = 7'b0001110;
91          default: HEX0 = 7'b1000000;
92      endcase
93  end
94
95
```

實驗結果照片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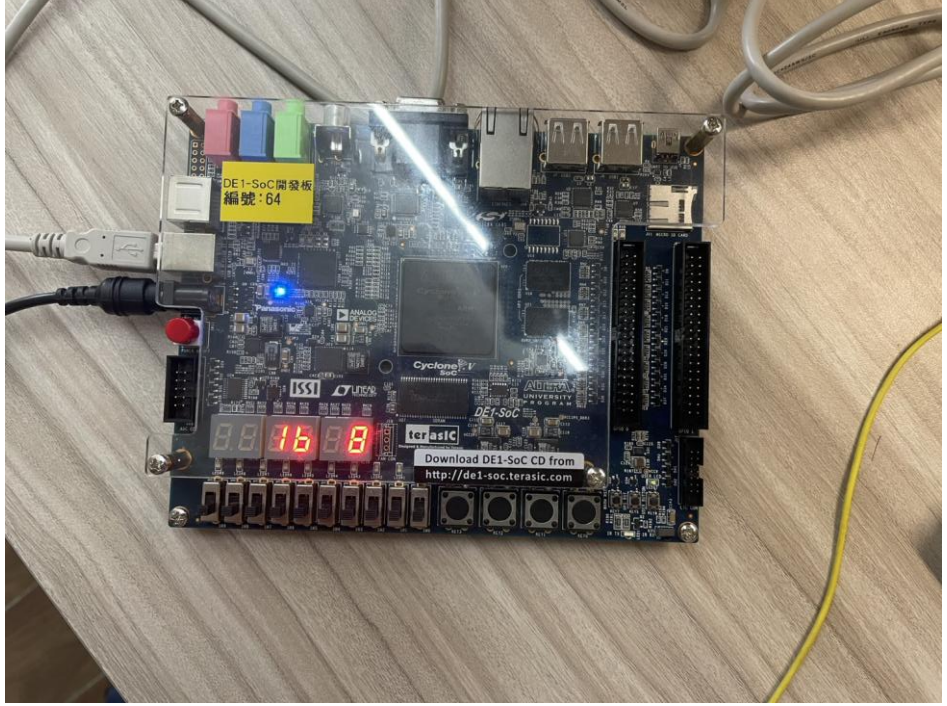
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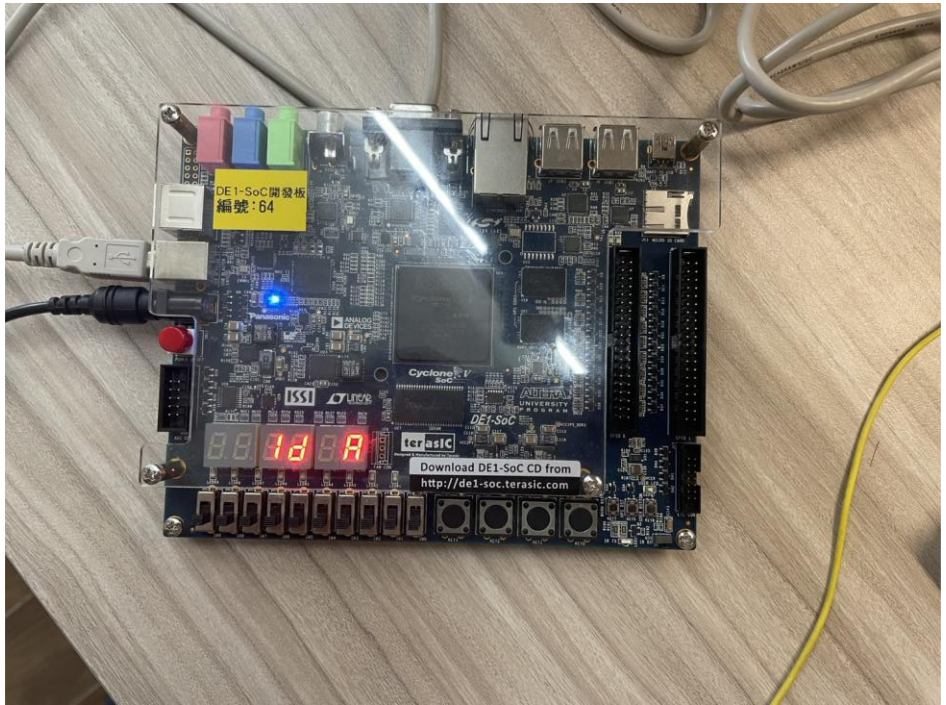
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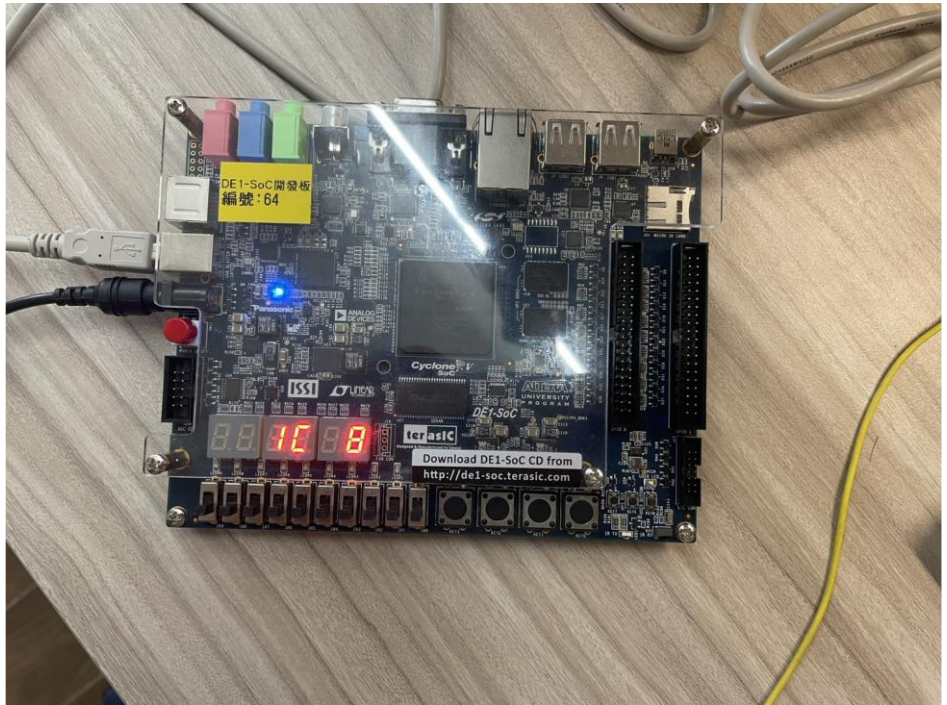
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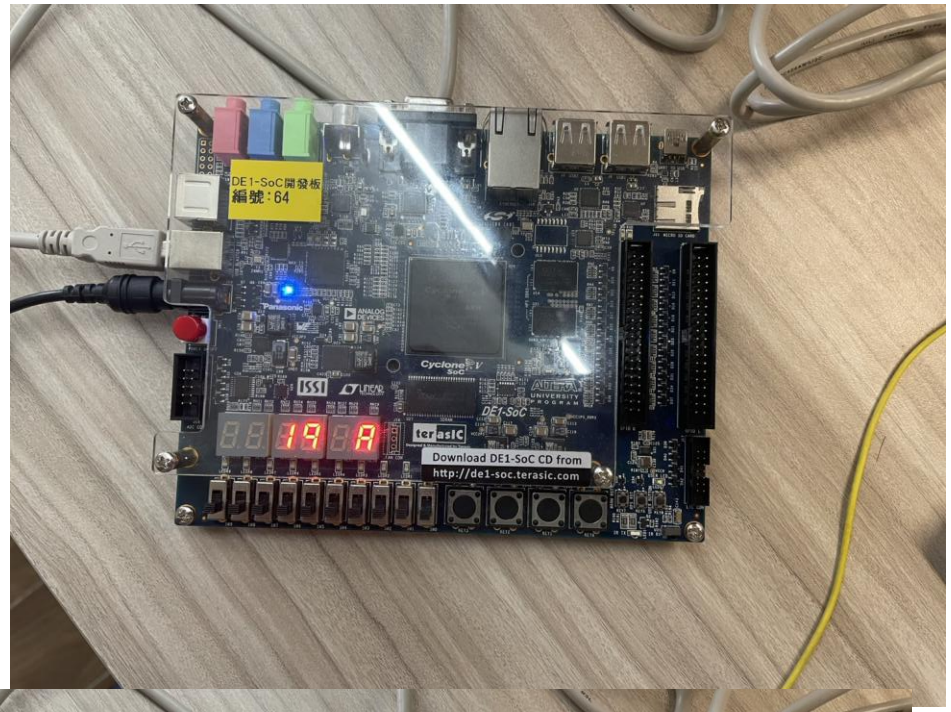
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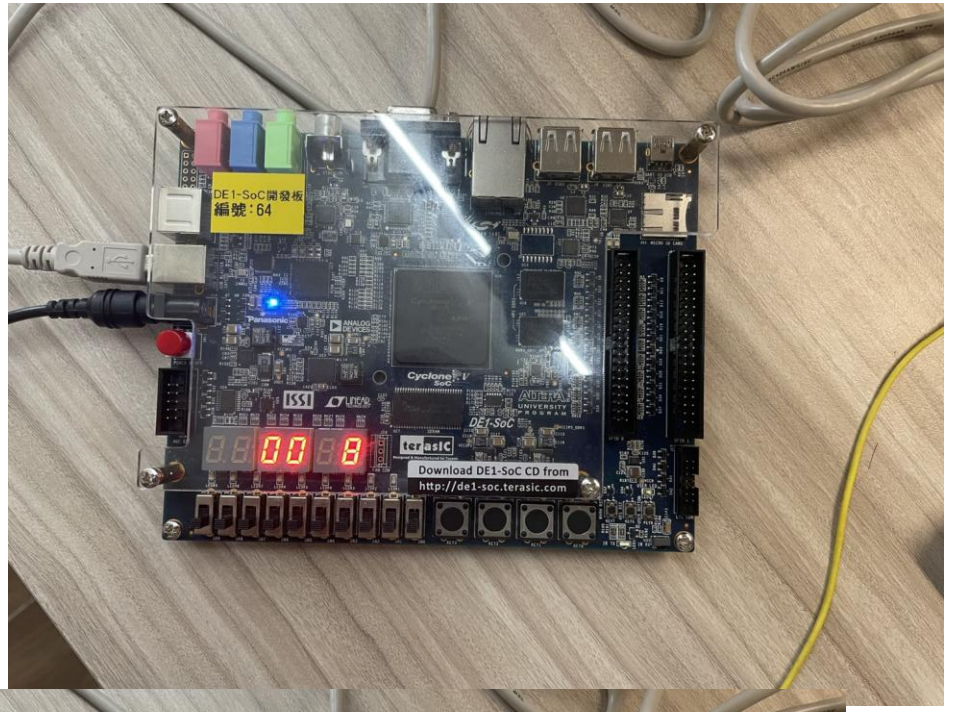
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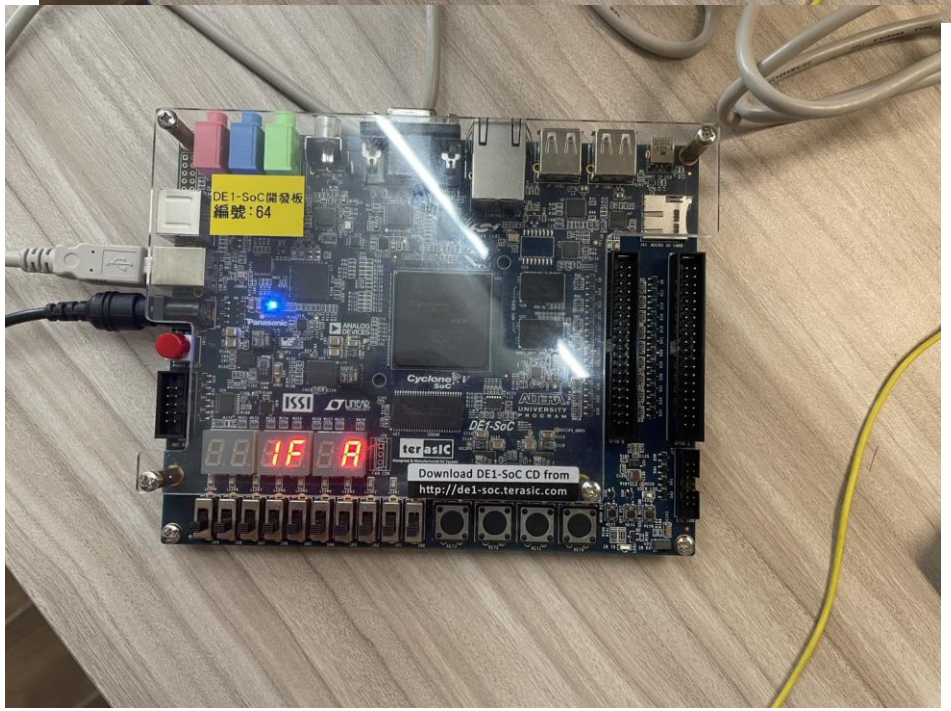
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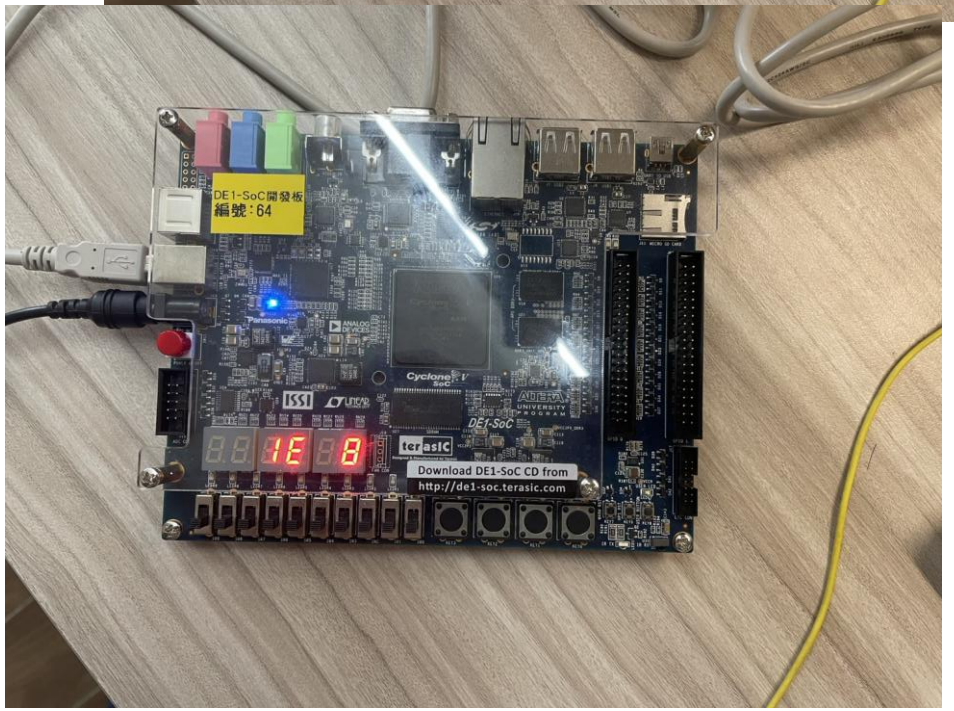
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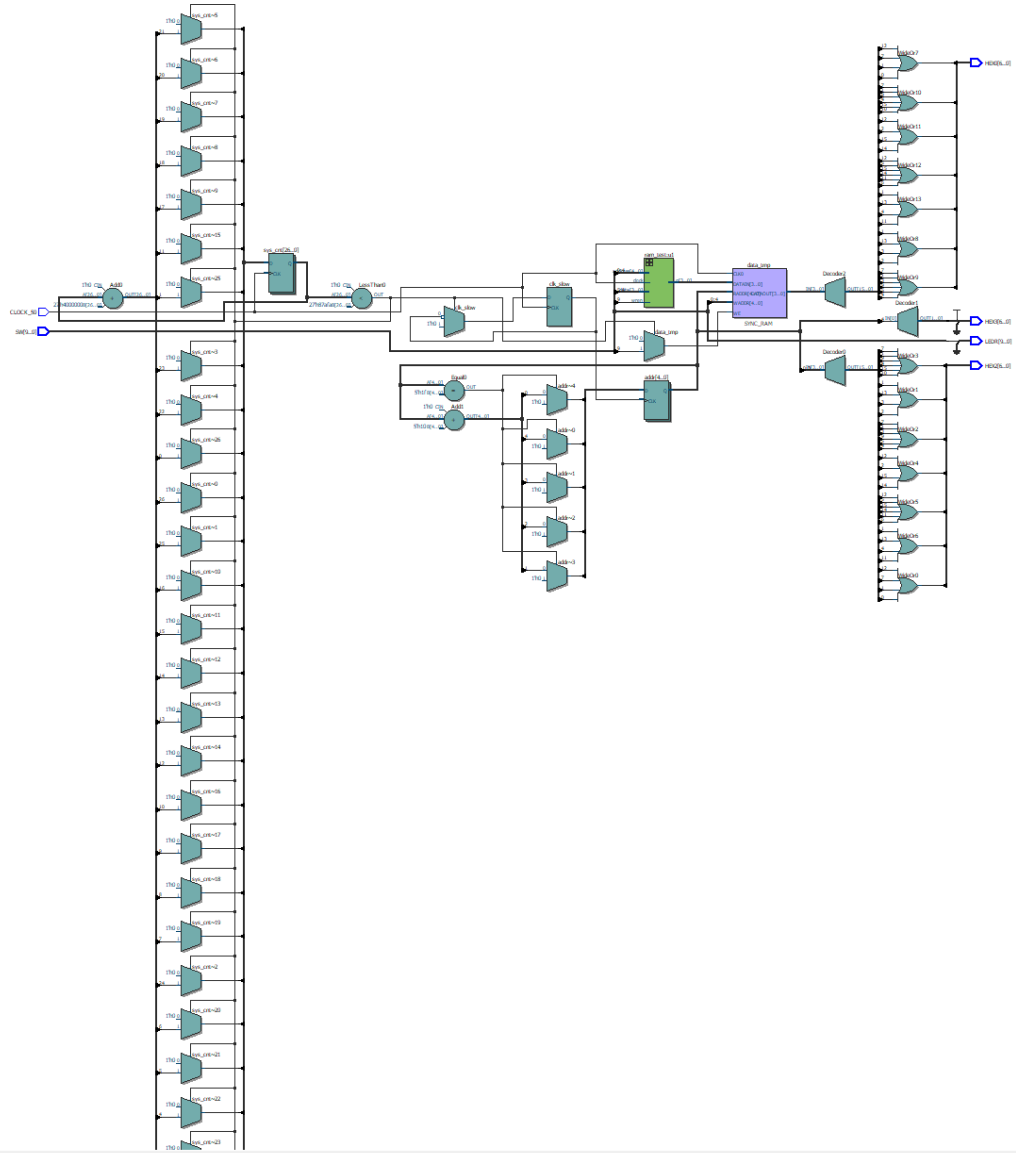
RAM

RAM:1



100% 00:00:09

問題與討論

問題:一開始撰寫CODE時，遇到該如何把地址與地址所讀取資料，以肉眼可見的速度一一讀取出。

討論 : 最後使用最笨的方法，以計數器數50M次後，在使用一個慢CLK數1秒，接下來讓地址與地址讀取到的數據1秒1秒跳。