

LAB04_312651057

吳鴻明

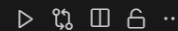
實驗目的

Finite-state-machine練習

實驗程式碼



FSM_bg.v M X



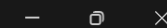
FSM_bg.v

```
1 module FSM(SW,KEY,HEX0);
2     input [3:0]KEY;
3     input [2:0]SW;
4     output reg [6:0]HEX0;
5
6     reg [3:0] result_ff,result;
7     reg [1:0] input_ff;
8
9
10    always@(negedge KEY[0] or negedge SW[0]) begin
11        if(!SW[0]) begin
12            result_ff <= 4'b0000;
13        end
14        else begin
15            if(SW[2:1] == 2'b00) begin
16                result_ff <= result_ff;
17            end
18            else if(SW[2:1] == 2'b01) begin
19                if(result_ff < 9)begin
20                    result_ff <= result_ff + 1;
21                end
22                else begin
23                    result_ff <= 4'b0000;
24                end
25            end
26            else if(SW[2:1] == 2'b10) begin
27                if(result_ff == 8 )begin
28                    result_ff <= 4'b0000;
29                end
30                else if(result_ff == 9) begin
31                    result_ff <= 4'b0001;
32                end
33                else begin
34                    result_ff <= result_ff + 2;
35                end
36            end
37            else if(SW[2:1] == 2'b11) begin
38                if(result_ff == 0)begin
39                    result_ff <= 4'd9;
40                end
41                else begin
42                    result_ff <= result_ff - 1;
43                end
44            end
45        end
46    end
47
48
```

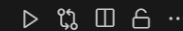




LAB04



FSM_bg.v M X



FSM_bg.v

```
1  module FSM(SW,KEY,HEX0);
10  always@(negedge KEY[0] or negedge SW[0]) begin
45      end
46
47
48
49      always@(*)begin
50          result = result_ff;
51          case(result)
52              4'b0000: HEX0 = 7'b1000000;
53              4'b0001: HEX0 = 7'b1111001;
54              4'b0010: HEX0 = 7'b0100100;
55              4'b0011: HEX0 = 7'b0110000;
56              4'b0100: HEX0 = 7'b0011001;
57              4'b0101: HEX0 = 7'b0010010;
58              4'b0110: HEX0 = 7'b0000011;
59              4'b0111: HEX0 = 7'b1011000;
60              4'b1000: HEX0 = 7'b0000000;
61              4'b1001: HEX0 = 7'b0011000;
62              4'b1010: HEX0 = 7'b0001000;
63              4'b1011: HEX0 = 7'b0000011;
64              4'b1100: HEX0 = 7'b1000110;
65              4'b1101: HEX0 = 7'b0100001;
66              4'b1110: HEX0 = 7'b0000110;
67              4'b1111: HEX0 = 7'b0001110;
68              default: HEX0 = 7'b1000000;
69          endcase
70      end
71
72
73
74  endmodule
```



問題與討論

問題:在實作中，遇到state如何設計。

討論:後來想想直接用簡單的case去做就好了