

LAB09_312651057

吳鴻明

實驗目的

將ARM上的DDR3與FPGA透過Avalon MM，溝通並存入與讀出DATA，不可使用FPGA上的邏輯去作出一個記憶體。

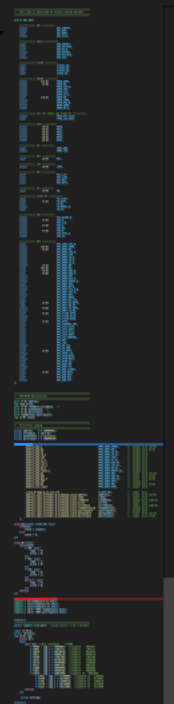
實驗程式碼

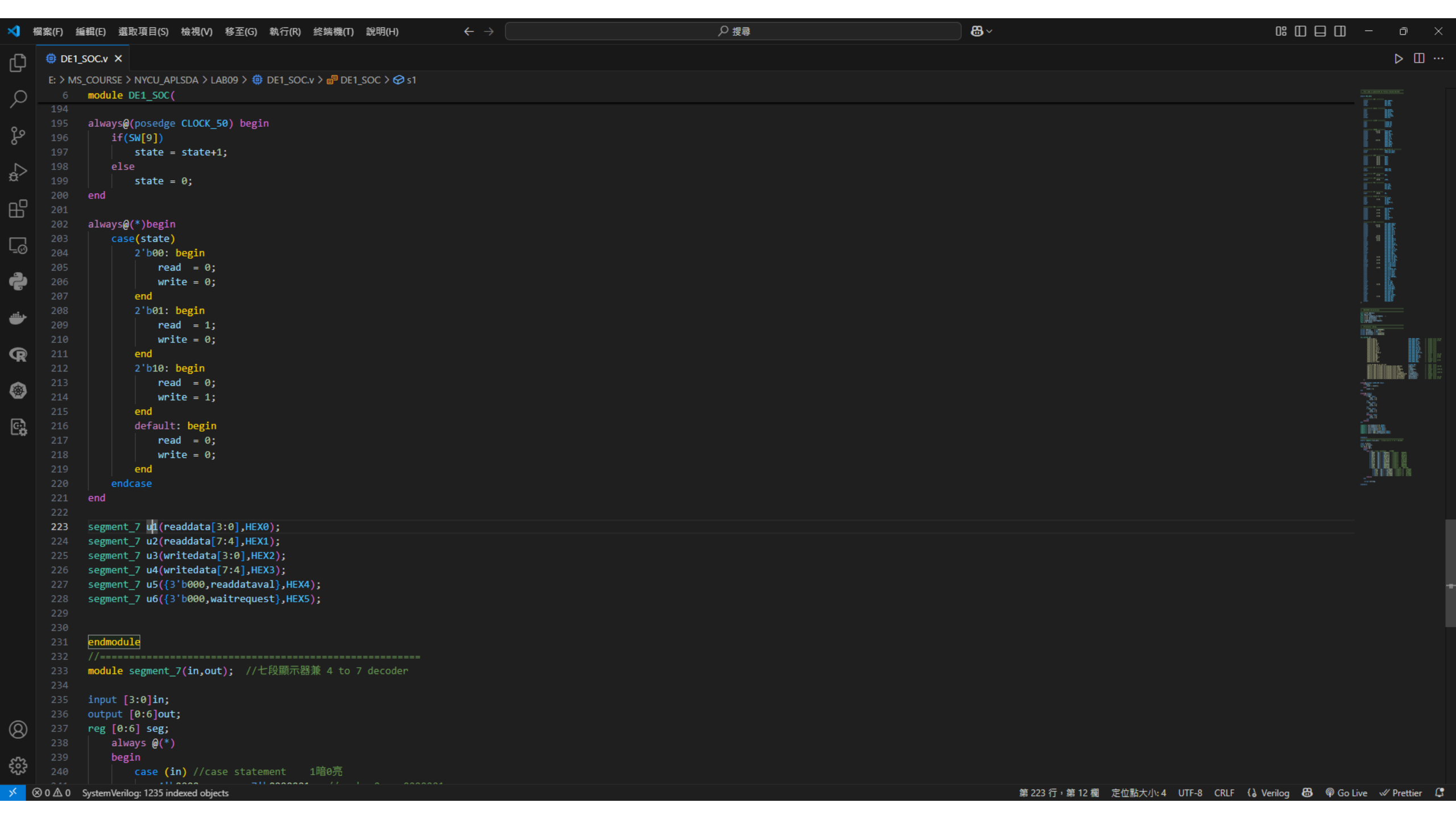


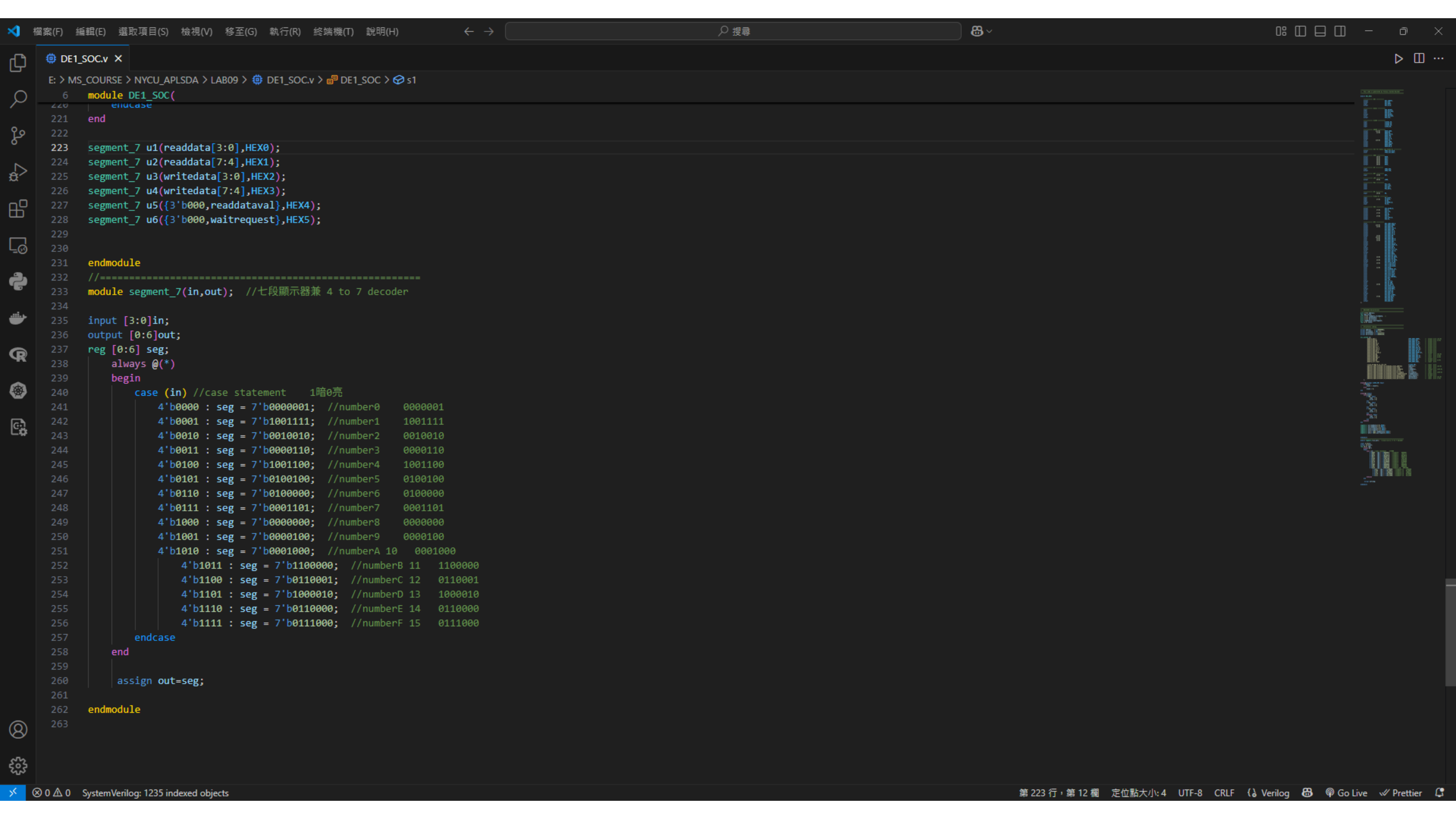
DE1_SOC.v 1 x

E: > MS_COURSE > NYCU_APLSDA > LAB09 > DE1_SOC.v > DE1_SOC

```
6 module DE1_SOC(  
147 // REG/WIRE declarations  
148 //=====   
149 wire [7:0] address;  
150 reg read,write;  
151 wire [7:0] readdata,writedata; //   
152 wire [7:0] byteenable; //   
153 wire [7:0] burstcount; //   
154 wire readdataval,waitrequest;  
155 reg [1:0] state;  
156   
157 //=====   
158 // Structural coding   
159 //=====   
160 assign address = 8'b00000001;  
161 assign writedata = SW[7:0];  
162 assign byteenable = 8'b11111111;  
163 assign burstcount = 8'b00000100;  
164   
165 soc_system s1(  
166     .memory_mem_a (HPS_DDR3_ADDR), // output wire [14:0] .memory.mem_a  
167     .memory_mem_ba (HPS_DDR3_BA), // output wire [2:0] .mem_ba  
168     .memory_mem_ck (HPS_DDR3_CK_P), // output wire .mem_ck  
169     .memory_mem_ck_n (HPS_DDR3_CK_N), // output wire .mem_ck_n  
170     .memory_mem_cke (HPS_DDR3_CKE), // output wire .mem_cke  
171     .memory_mem_cs_n (HPS_DDR3_CS_N), // output wire .mem_cs_n  
172     .memory_mem_ras_n (HPS_DDR3_RAS_N), // output wire .mem_ras_n  
173     .memory_mem_cas_n (HPS_DDR3_CAS_N), // output wire .mem_cas_n  
174     .memory_mem_we_n (HPS_DDR3_WE_N), // output wire .mem_we_n  
175     .memory_mem_reset_n (HPS_DDR3_RESET_N), // output wire .mem_reset_n  
176     .memory_mem_dq (HPS_DDR3_DQ), // inout wire [31:0] .mem_dq  
177     .memory_mem_dqs (HPS_DDR3_DQS_P), // inout wire [3:0] .mem_dqs  
178     .memory_mem_dqs_n (HPS_DDR3_DQS_N), // inout wire [3:0] .mem_dqs_n  
179     .memory_mem_odt (HPS_DDR3_ODT), // output wire .mem_odt  
180     .memory_mem_dm (HPS_DDR3_DM), // output wire [3:0] .mem_dm  
181     .memory_oct_rzqin (HPS_DDR3_RZQ), // input wire .oct_rzqin  
182   
183     .clock_bridge_0_in_clk_clk (CLOCK_50), // input wire .clock_bridge_0_in_clk.clk  
184     .address_span_extender_0_windowed_slave_address (address), // input wire [15:0] .address_span_extender_0_windowed_slave.address  
185     .address_span_extender_0_windowed_slave_read (read), // input wire .read  
186     .address_span_extender_0_windowed_slave_readdata (readdata), // output wire [255:0] .readdata  
187     .address_span_extender_0_windowed_slave_write (write), // input wire .write  
188     .address_span_extender_0_windowed_slave_writedata (writedata), // input wire [255:0] .writedata  
189     .address_span_extender_0_windowed_slave_readdatavalid (readdataval), // output wire .readdatavalid  
190     .address_span_extender_0_windowed_slave_waitrequest (waitrequest), // output wire .waitrequest  
191     .address_span_extender_0_windowed_slave_byteenable (byteenable), // input wire [31:0] .byteenable  
192     .address_span_extender_0_windowed_slave_burstcount (burstcount) // input wire [7:0] .burstcount  
193 );
```







實驗結果照片

DE1-Soc 開發板
編號: 64

000801

Download DE1-Soc CD from
<http://de1-soc.terasic.com>

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Cyclone V
soc

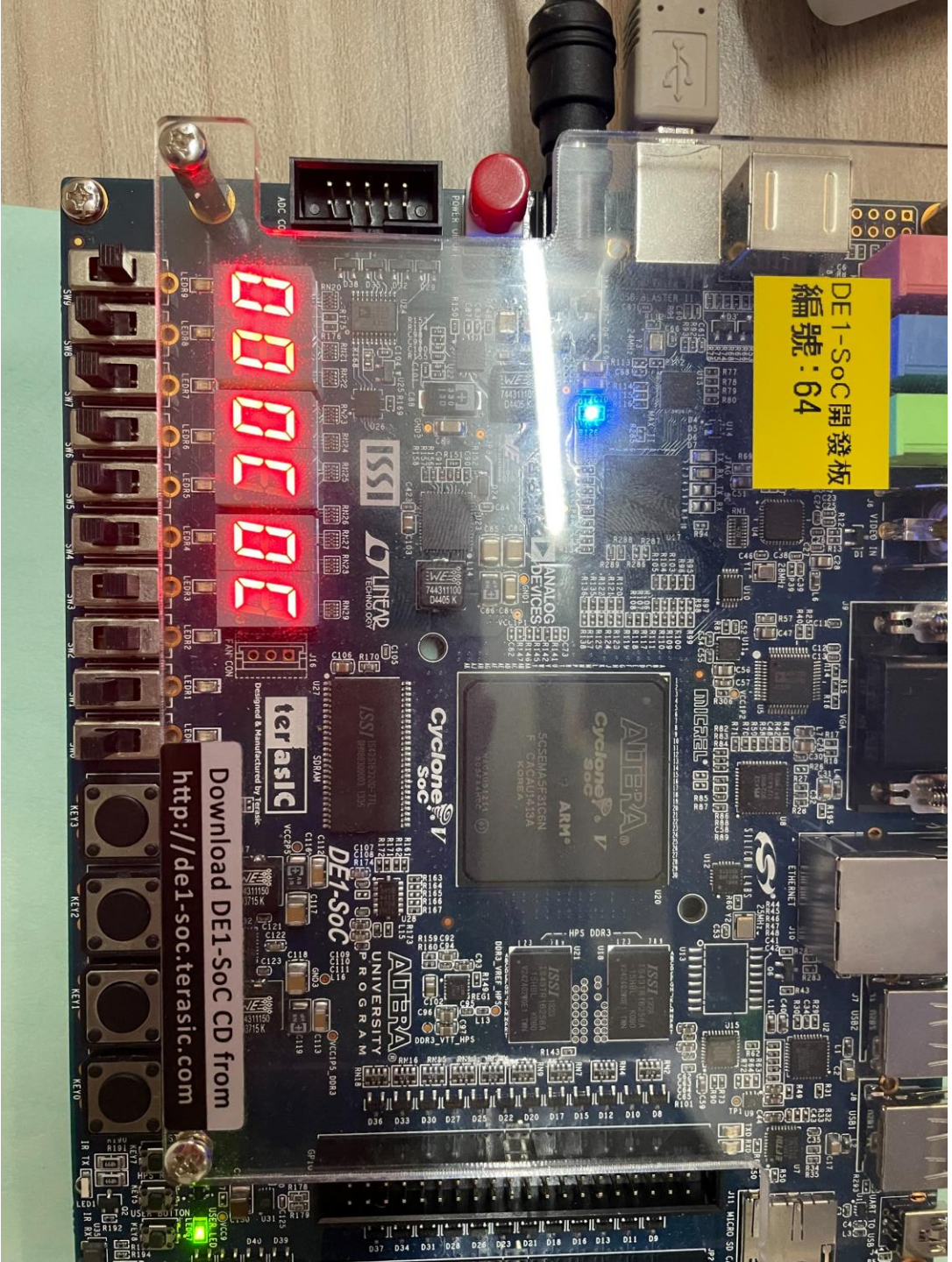
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DE1-Soc
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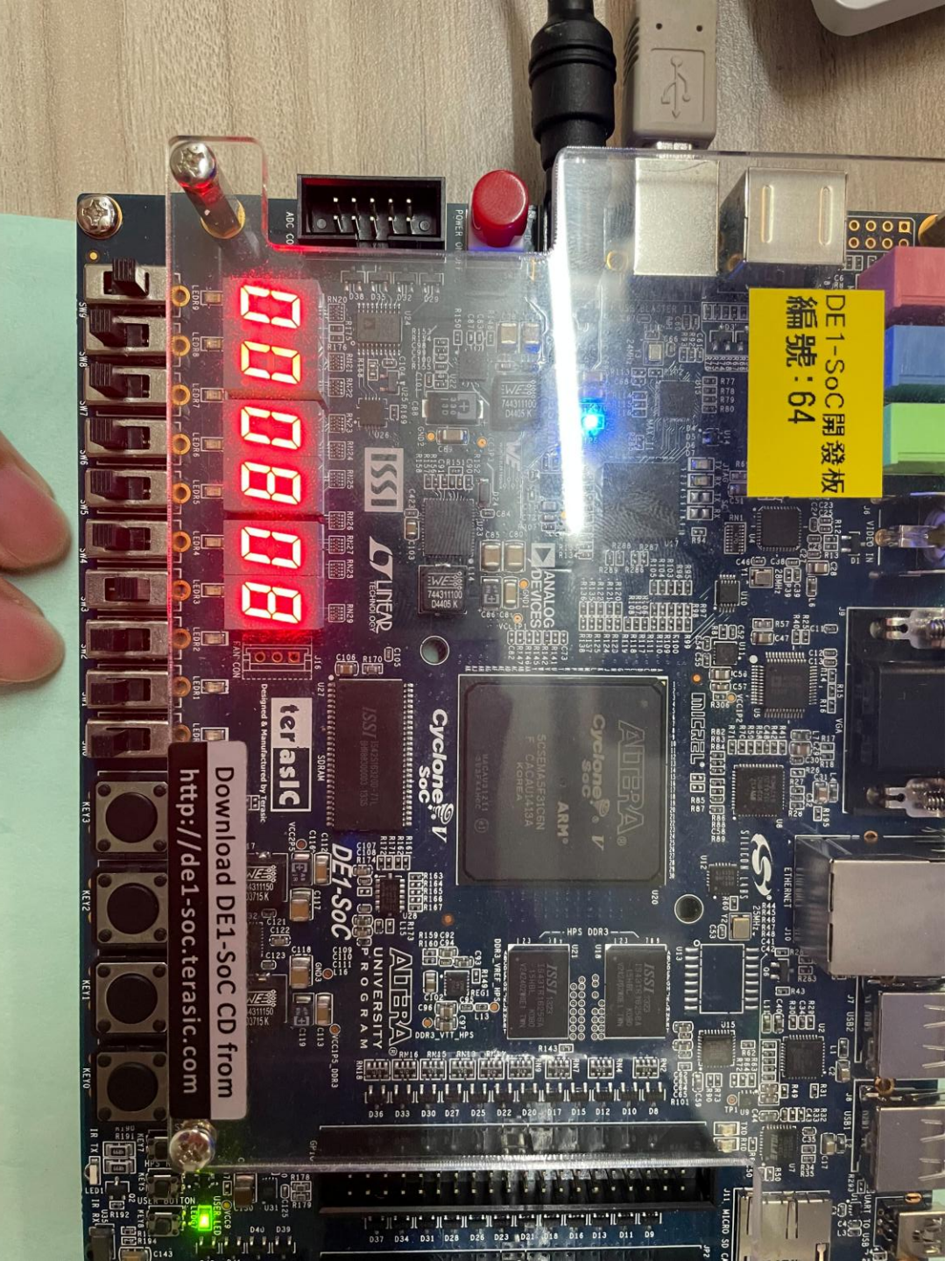
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問題與討論

問題：在寫Avalon MM時一直遇到問題，也問了助教以及同學。

討論：經過激烈討論後發覺，是自己沒有寫完整通訊協議，所以導致跑不出來。