109-2 VLSI Testing PA3 Report

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1 What I've done in this PA

In this PA, I have:

- trace the source code
- fill up the holes in *tdfsim.cpp*
- check the correctness of fault activation and V1 simulation
- run *golden_tdfsim* to validate my answers
- run several cases with *golden_tdfsim* to fill up the table below.

1.1 Problems I tackled

I faced a problem that shows "something is fishy(get_faulty_net)". It seems that I have generated faults in NOT and BUF gates, and it causes my result to be slightly different from the result of *golden_tdfsim*.

1.2 How I generated the tdf fault list

The program walks through all the wires and adds STR and STF on each wire. For the fanout branches, the program adds extra tdfs on each fanout stem.

2 The Table

circuit number	number of gates	number of total TDFs	number of detected faults	number of undetected faults	transition delay fault coverage
C17	6	34	23	11	67.64%
C432	245	1110	3	1107	0.27%
C499	554	2390	1552	838	64.94%
C880	545	2104	792	1312	37.64%
C1355	554	2726	593	2133	21.75%
C2670	1785	6520	4668	1852	71.60%
C3540	2082	7910	1142	6768	14.44%
C6288	4800	17376	16532	1844	95.14%
C7552	5679	19456	17421	2035	89.54%