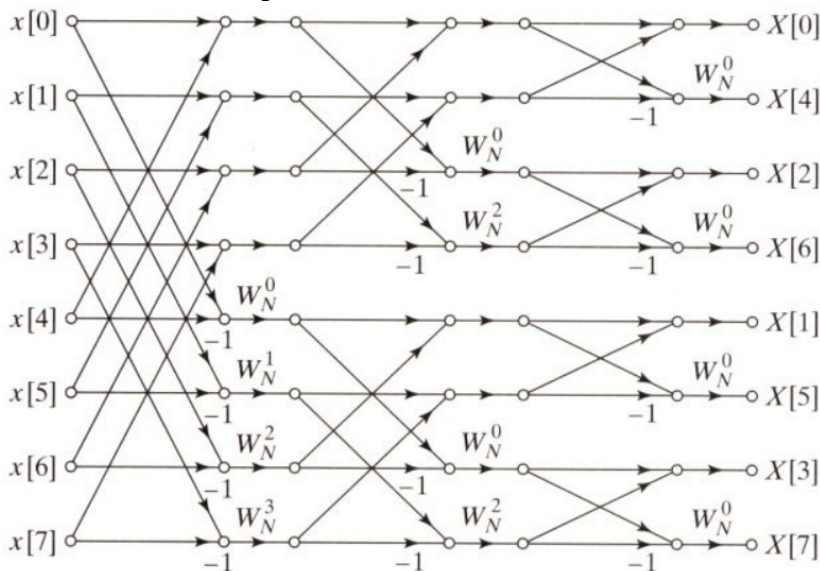


Lab C Report – DFT

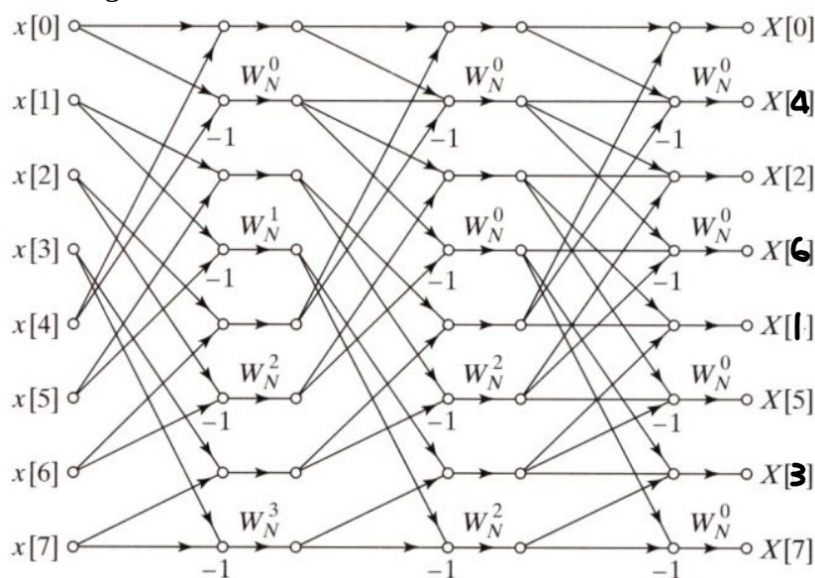
Introduction to the Algorithm and Overall System

The problem is to perform digital Fourier transformation (DFT) to a 1024-size vector, so we implement it by fast Fourier transformation (FFT).

We use the basic Radix-2 FFT. Since the usual FFT has different connecting structure in each stage, which is difficult to perform ARRAY_PARTITION to accelerate the process.^[1]



We adopt the connecting structure shown in the following figure, which has the same structure in each stage:^[1]



(Note: in Wikipedia the result has no bit reversal, but in our experiment and derivation the result must be bit reversal.)

By this algorithm we can first split the array into two blocks, and in each block we may use cyclic ARRAY_PARTITION to accelerate the process. This allow us to choose partition factor with more freedom.

At the final stage we need to do bit reversal process, and we combine it with output stage.

The value of cosine, sine and bit reversal are constant and is stored in look-up table to accelerate the process.

Details for Code and Pragma

The main program is a ten-stage FFT, and we use axis as input and output interfaces. To meet the requirement memory bandwidth, the array in each state input (output) is split into two arrays (as block partition) and each of them uses cyclic ARRAY_PARTITION pragma.

```
void dft(DTYPE real_sample[1024], DTYPE imag_sample[1024], DTYPE real_op[1024], DTYPE imag_op[1024])
{
    //Write your code here
    #pragma HLS INTERFACE mode=axis port=real_sample
    #pragma HLS INTERFACE mode=axis port=imag_sample
    #pragma HLS INTERFACE mode=axis port=real_op
    #pragma HLS INTERFACE mode=axis port=imag_op

    DTYPE R1u[SIZE/2], R2u[SIZE/2], I1u[SIZE/2], I2u[SIZE/2];
    DTYPE R1d[SIZE/2], R2d[SIZE/2], I1d[SIZE/2], I2d[SIZE/2];
    #pragma HLS ARRAY_PARTITION variable=R1u,R2u,I1u,I2u,R1d,R2d,I1d,I2d type=cyclic factor=8

    transfer_data_in(real_sample, imag_sample, R1u, R1d, I1u, I1d);
    fft_stage(R1u, R1d, I1u, I1d, 1, R2u, R2d, I2u, I2d);
    fft_stage(R2u, R2d, I2u, I2d, 2, R1u, R1d, I1u, I1d);
    fft_stage(R1u, R1d, I1u, I1d, 3, R2u, R2d, I2u, I2d);
    fft_stage(R2u, R2d, I2u, I2d, 4, R1u, R1d, I1u, I1d);
    fft_stage(R1u, R1d, I1u, I1d, 5, R2u, R2d, I2u, I2d);
    fft_stage(R2u, R2d, I2u, I2d, 6, R1u, R1d, I1u, I1d);
    fft_stage(R1u, R1d, I1u, I1d, 7, R2u, R2d, I2u, I2d);
    fft_stage(R2u, R2d, I2u, I2d, 8, R1u, R1d, I1u, I1d);
    fft_stage(R1u, R1d, I1u, I1d, 9, R2u, R2d, I2u, I2d);
    fft_stage(R2u, R2d, I2u, I2d, 10, R1u, R1d, I1u, I1d);
    /*
    bit_reversal(R1u, R1d, I1u, I1d, R2u, R2d, I2u, I2d);
    transfer_data_out(R2u, R2d, I2u, I2d, real_op, imag_op);
    */
    bit_reversal_out(R1u, R1d, I1u, I1d, real_op, imag_op);
}
```

The code also shows that bit reversal and output process are combined into one stage.

This structure of FFT is not suitable for DATAFLOW, since all stages run sequentially and in each stage the memory read and write pattern is not sequential.

```
void fft_stage(DTYPE Ruin[SIZE/2], DTYPE Rdin[SIZE/2], DTYPE Iuin[SIZE/2], DTYPE Idin[SIZE/2],
               int stage, DTYPE Ruout[SIZE/2], DTYPE Rdout[SIZE/2], DTYPE Iuout[SIZE/2], DTYPE Idout[SIZE/2]){
    int SIZE4 = SIZE >> 2;
    int angle = 0;
    for(int i=0; i<SIZE/2; i++){
        #pragma HLS PIPELINE II=1
        #pragma HLS UNROLL factor=16
        if(i%2==0){
            Ruout[i] = Ruin[i>>1] + Rdin[i>>1];
            Iuout[i] = Iuin[i>>1] + Idin[i>>1];
        }
        else{

```

Computation in FFT is accelerated by UNROLL pragma.

```
const DTYPE W_real[]={1.0, 0.99998116, 0.9999247, 0.9998306, 0.9996988, 0.9995294,
0.999336, 0.999016, 0.998572, 0.998017, 0.997366, 0.996534, 0.995534, 0.994381, 0.993081, 0.991649, 0.990099, 0.988446, 0.986694, 0.984857, 0.982941, 0.980961, 0.978924, 0.976837, 0.974706, 0.972538, 0.970339, 0.968116, 0.965875, 0.963622, 0.961364, 0.959108, 0.956861, 0.95463, 0.952412, 0.950204, 0.947999, 0.945794, 0.943595, 0.941401, 0.93921, 0.937021, 0.934831, 0.932641, 0.930451, 0.928261, 0.926071, 0.923881, 0.921691, 0.919501, 0.917311, 0.915121, 0.912931, 0.910741, 0.908551, 0.906361, 0.904171, 0.901981, 0.899791, 0.897601, 0.895411, 0.893221, 0.891031, 0.888841, 0.886651, 0.884461, 0.882271, 0.880081, 0.877891, 0.875701, 0.873511, 0.871321, 0.869131, 0.866941, 0.864751, 0.862561, 0.860371, 0.858181, 0.855991, 0.853801, 0.851611, 0.849421, 0.847231, 0.845041, 0.842851, 0.840661, 0.838471, 0.836281, 0.834091, 0.831901, 0.829711, 0.827521, 0.825331, 0.823141, 0.820951, 0.818761, 0.816571, 0.814381, 0.812191, 0.810001, 0.807811, 0.805621, 0.803431, 0.801241, 0.799051, 0.796861, 0.794671, 0.792481, 0.790291, 0.788101, 0.785911, 0.783721, 0.781531, 0.779341, 0.777151, 0.774961, 0.772771, 0.770581, 0.768391, 0.766201, 0.764011, 0.761821, 0.759631, 0.757441, 0.755251, 0.753061, 0.750871, 0.748681, 0.746491, 0.744301, 0.742111, 0.739921, 0.737731, 0.735541, 0.733351, 0.731161, 0.728971, 0.726781, 0.724591, 0.722401, 0.720211, 0.718021, 0.715831, 0.713641, 0.711451, 0.709261, 0.707071, 0.704881, 0.702691, 0.700501, 0.698311, 0.696121, 0.693931, 0.691741, 0.689551, 0.687361, 0.685171, 0.682981, 0.680791, 0.678601, 0.676411, 0.674221, 0.672031, 0.669841, 0.667651, 0.665461, 0.663271, 0.661081, 0.658891, 0.656701, 0.654511, 0.652321, 0.650131, 0.647941, 0.645751, 0.643561, 0.641371, 0.639181, 0.636991, 0.634801, 0.632611, 0.630421, 0.628231, 0.626041, 0.623851, 0.621661, 0.619471, 0.617281, 0.615091, 0.612901, 0.610711, 0.608521, 0.606331, 0.604141, 0.601951, 0.599761, 0.597571, 0.595381, 0.593191, 0.591001, 0.588811, 0.586621, 0.584431, 0.582241, 0.580051, 0.577861, 0.575671, 0.573481, 0.571291, 0.569101, 0.566911, 0.564721, 0.562531, 0.560341, 0.558151, 0.555961, 0.553771, 0.551581, 0.549391, 0.547201, 0.545011, 0.542821, 0.540631, 0.538441, 0.536251, 0.534061, 0.531871, 0.529681, 0.527491, 0.525301, 0.523111, 0.520921, 0.518731, 0.516541, 0.514351, 0.512161, 0.509971, 0.507781, 0.505591, 0.503401, 0.501211, 0.499021, 0.496831, 0.494641, 0.492451, 0.490261, 0.488071, 0.485881, 0.483691, 0.481501, 0.479311, 0.477121, 0.474931, 0.472741, 0.470551, 0.468361, 0.466171, 0.463981, 0.461791, 0.459601, 0.457411, 0.455221, 0.453031, 0.450841, 0.448651, 0.446461, 0.444271, 0.442081, 0.439891, 0.437701, 0.435511, 0.433321, 0.431131, 0.428941, 0.426751, 0.424561, 0.422371, 0.420181, 0.417991, 0.415801, 0.413611, 0.411421, 0.409231, 0.407041, 0.404851, 0.402661, 0.400471, 0.398281, 0.396091, 0.393901, 0.391711, 0.389521, 0.387331, 0.385141, 0.382951, 0.380761, 0.378571, 0.376381, 0.374191, 0.372001, 0.369811, 0.367621, 0.365431, 0.363241, 0.361051, 0.358861, 0.356671, 0.354481, 0.352291, 0.350101, 0.347911, 0.345721, 0.343531, 0.341341, 0.339151, 0.336961, 0.334771, 0.332581, 0.330391, 0.328201, 0.326011, 0.323821, 0.321631, 0.319441, 0.317251, 0.315061, 0.312871, 0.310681, 0.308491, 0.306301, 0.304111, 0.301921, 0.299731, 0.297541, 0.295351, 0.293161, 0.290971, 0.288781, 0.286591, 0.284401, 0.282211, 0.280021, 0.277831, 0.275641, 0.273451, 0.271261, 0.269071, 0.266881, 0.264691, 0.262501, 0.260311, 0.258121, 0.255931, 0.253741, 0.251551, 0.249361, 0.247171, 0.244981, 0.242791, 0.240601, 0.238411, 0.236221, 0.234031, 0.231841, 0.229651, 0.227461, 0.225271, 0.223081, 0.220891, 0.218701, 0.216511, 0.214321, 0.212131, 0.209941, 0.207751, 0.205561, 0.203371, 0.201181, 0.198991, 0.196801, 0.194611, 0.192421, 0.190231, 0.188041, 0.185851, 0.183661, 0.181471, 0.179281, 0.177091, 0.174901, 0.172711, 0.170521, 0.168331, 0.166141, 0.163951, 0.161761, 0.159571, 0.157381, 0.155191, 0.153001, 0.150811, 0.148621, 0.146431, 0.144241, 0.142051, 0.139861, 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```

Score

We calculate the score under different constraint and synthesis parameters:

1. Limited to resource used in FPGA, target clock time=10ns:

Csynthesis

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	7.256 ns	2.70 ns

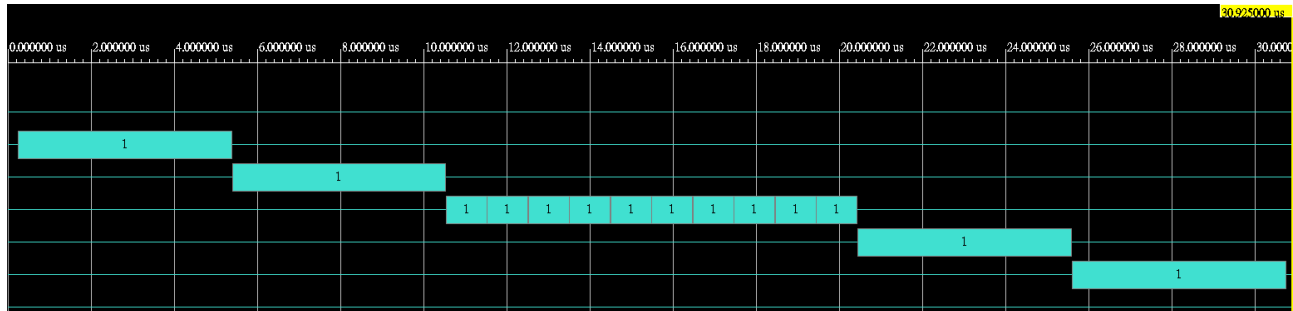
Performance & Resource Estimates

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM(%)	DSP(%)	FF(%)	LUT(%)	URAM(%)
dft					3099	3.099E4	-	3100		no	56	94	23	85	0
dft_pipeline_VITIS_LOOP_36_1				-	514	5.140E3	-	514	-	no	0	0	~0	~0	0
dft_pipeline_VITIS_LOOP_41_2				-	514	5.140E3	-	514	-	no	0	0	~0	~0	0
fft_stage				-	101	1.010E3	-	101	-	no	10	94	23	72	0
dft_pipeline_VITIS_LOOP_65_1				-	515	5.150E3	-	515	-	no	0	0	~0	~0	0
dft_pipeline_VITIS_LOOP_77_2				-	515	5.150E3	-	515	-	no	0	0	~0	~0	0

Cosimulation

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
• dft				3059	3059	3059
▶ dft_Pipeline_VITIS_LOOP_36_1				512	512	512
▶ dft_Pipeline_VITIS_LOOP_41_2				512	512	512
▶ fft_stage	99	99	99	97	97	97
▶ dft_Pipeline_VITIS_LOOP_65_1				513	513	513
▶ dft_Pipeline_VITIS_LOOP_77_2				513	513	513

Waveform



Score: $(1 \div (7.256 \times 10^{-9})) \div (309250 \div 10) = 4456.49$

2. Limited to resource used in FPGA, target clock time=7ns:

Csynthesis

Timing Estimate

Target	Estimated	Uncertainty	
7.00 ns	5.024 ns	1.89 ns	

Performance & Resource Estimates

Modules

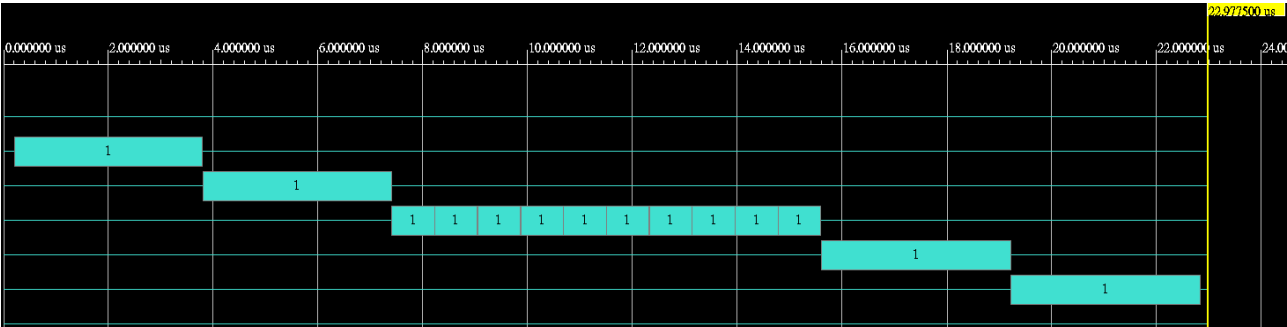
Loops

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM(%)	DSP(%)	FF(%)	LUT(%)	URAM(%)
dft					3283	2.298E4	-	3284	-	no	56	94	32	89	0
dft_Pipeline_VITIS_LOOP_36_1				-	514	3.598E3	-	514	-	no	0	0	~0	~0	0
dft_Pipeline_VITIS_LOOP_41_2				-	514	3.598E3	-	514	-	no	0	0	~0	~0	0
fft_stage				-	119	833.000	-	119	-	no	10	94	30	76	0
dft_Pipeline_VITIS_LOOP_65_1				-	517	3.619E3	-	517	-	no	0	0	1	~0	0
dft_Pipeline_VITIS_LOOP_77_2				-	517	3.619E3	-	517	-	no	0	0	1	~0	0

Cosimulation

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
➤ dft				3245	3245	3245
➤ dft_Pipeline_VITIS_LOOP_36_1				512	512	512
➤ dft_Pipeline_VITIS_LOOP_41_2				512	512	512
➤ fft_stage	117	117	117	115	115	115
➤ dft_Pipeline_VITIS_LOOP_65_1				515	515	515
➤ dft_Pipeline_VITIS_LOOP_77_2				515	515	515

Waveform



Score: $(1 \div (5.024 \times 10^{-9})) \div (229775 \div 7) = 6063.81$

3. Unlimited to resource used in FPGA, target clock time=10ns, unroll factor=128:

Csynthesis

Timing Estimate

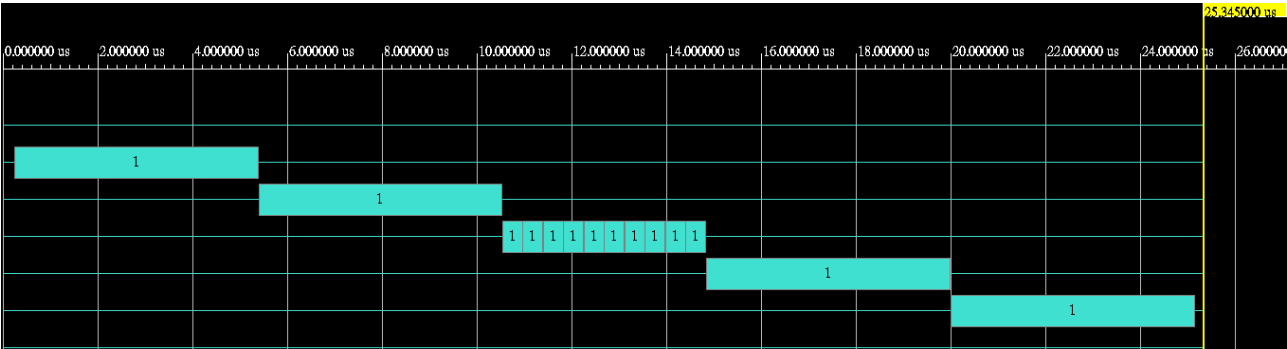
Target	Estimated	Uncertainty
10.00 ns	7.256 ns	2.70 ns

Performance & Resource Estimates

Cosimulation

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
dft				2501	2501	2501
dft_Pipeline_VITIS_LOOP_36_1				512	512	512
dft_Pipeline_VITIS_LOOP_41_2				512	512	512
fft_stage	43	43	43	41	41	41
dft_Pipeline_VITIS_LOOP_65_1				513	513	513
dft_Pipeline_VITIS_LOOP_77_2				513	513	513

Waveform



Score: $(1 \div (7.256 \times 10^{-9})) \div (253450 \div 10) = 5437.64$

4. Unlimited to resource used in FPGA, target clock time=7ns, unroll factor=128:

Csynthesis

Timing Estimate

Target	Estimated	Uncertainty	
7.00 ns	4.353 ns	1.89 ns	

Performance & Resource Estimates

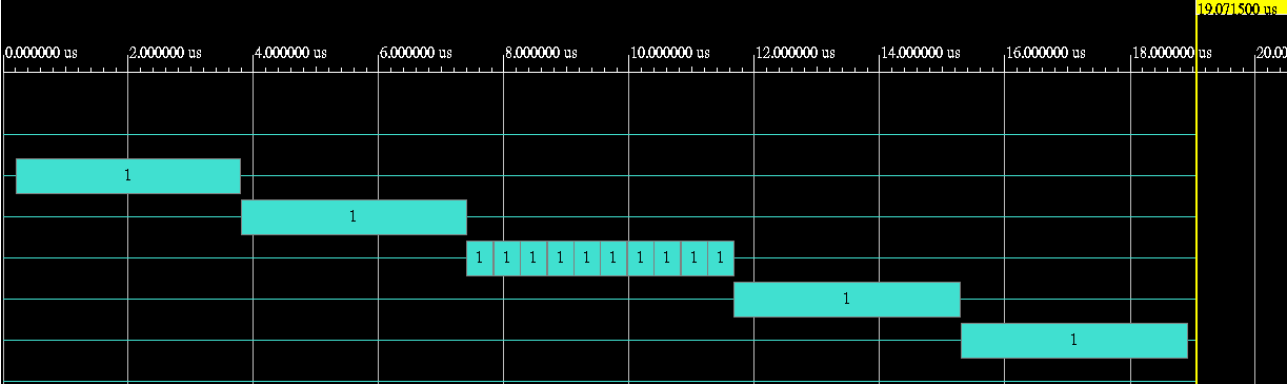
Modules & Loops

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM(%)	DSP(%)	FF(%)	LUT(%)	URAM(%)
dft				-	2723	1.906E4	-	2724	-	no	90	756	286	706	0
▶ dft_Pipeline_VITIS_LOOP_36_1				-	514	3.598E3	-	514	-	no	0	0	~0	~0	0
▶ dft_Pipeline_VITIS_LOOP_41_2				-	514	3.598E3	-	514	-	no	0	0	~0	~0	0
▶ fft_stage				-	63	441.000	-	63	-	no	90	756	239	611	0
▶ dft_Pipeline_VITIS_LOOP_65_1				-	517	3.619E3	-	517	-	no	0	0	7	2	0
▶ dft_Pipeline_VITIS_LOOP_77_2				-	517	3.619E3	-	517	-	no	0	0	7	2	0

Cosimulation

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
• dft				2687	2687	2687
▸ • dft_Pipeline_VITIS_LOOP_36_1				512	512	512
▸ • dft_Pipeline_VITIS_LOOP_41_2				512	512	512
▸ • fft_stage	61	61	61	59	59	59
▸ • dft_Pipeline_VITIS_LOOP_65_1				515	515	515
▸ • dft_Pipeline_VITIS_LOOP_77_2				515	515	515

Waveform



Score: $(1 \div (4.353 \times 10^{-9})) \div (190715 \div 7) = 8431.88$

Final Result (Score)

Resource	Limited		Unlimited	
Target Clock	10ns	7ns	10ns	7ns
Score	4456.49	6063.81	5437.64	8431.88

Reference

[1] <https://zh.wikipedia.org/zh-tw/%E5%BA%93%E5%88%A9%E5%BC%8D%E5%9B%BE%E5%9F%BA%E5%BF%AB%E9%80%9F%E5%82%85%E9%87%8C%E5%8F%B6%E5%8F%98%E6%8D%A2%E7%AE%97%E6%B3%95%E5%96%AE%E4%B8%80%E5%9F%BA%E5%BA%95>