Lab3 Report

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1 Modules Explanation

1. **branch_predictor.v :**
   branch_predictor module reads input value "is_branch", "result", "addr_1" and "addr_2" to decide the register "state" and output value "predict_o", "reserved_addr". Register "state" is initialized to 2b'11 in testbench, it changes its value according to "result" when "is_branch" = 1. Then predict_o and "reserved_addr" are assigned according to the value of state. Note that "predict_o" is used to predict taken/untaken, and "reserved_addr" is used to reserved the address to restored when the prediction is wrong.

2. **ALU_Control.v :**
   The difference in ALU_Control module between lab2 and lab3 is that in lab2, there is no output alu_control signal indicates that instruction is "beq", and "beq" is seen as "sub". However in lab3, sub's alu_control signal = 4'b0110, while beq's alu_control signal = 4'b1110.

3. **ALU.v :**
   The difference in ALU module between lab2 and lab3 is that lab3 has the output "zero", this output is updated when input "alu_control" indicates that instruction is "beq". In lab2, there is no output "zero" nor the "alu_control" of "beq".

4. **Flush_Control.v :**
   The difference in Flush_Control module between lab2 and lab3 is that in lab2, it only decides one flush control, while in lab3 it decides two flush controls on IF_ID stage and ID_EX stage. It reads input "IFID_branch", "IDEX_branch", which indicates that IF_ID/ID_EX stage is branch, and input "predict", "result", which represent the value predictor predict/resolved outcome, to decide output "IFID_flush" and "IDEX_flush".

2 Difficulties Encountered and Solutions in This Lab

In this lab I didn't encounter difficult challenge. Only some minor problems are stated below :

1. I wonder why don't predict at IF stage instead of ID stage, but this had been answered.

2. I forgot to store the address not taken during prediction in order to restore it when I found that the prediction was wrong.

3 Development Environment

OS : Windows, compiler : iverilog