Lab1 Report

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1 Modules Explanation

1. **CPU.v :**
   CPU module connects all modules to form a whole single-cycle CPU.

2. **Control.v :**
   Contorl module reads instruction[6:0] to decide the output value of ALUOp, ALUSrc and RegWrite, which is the first control signal of ALU, the source of ALU, and whehter to write back to register.

3. **ALU_Control.v :**
   ALU_Control modules reads ALUOp, funct7 and funct3, and uses them to decide the ouput value of alu_control. This module controls the operaiton of ALU according to its input.

4. **ALU.v :**
   ALU modules performs operation according to the input data "data_1", "data_2", and the input control signal "alu_contorl. Then it assigns the result to output value "result", and assign 1 to output value "Zero" if data_1 = data_2, otherwise 0.

5. **Add_PC.v :**
   Add_PC module reads the current PC "previous_pc" and adds it with 4 to generate outupt next PC "next_pc.

6. **MUX32.v :** MUX32 module reads the input control signal "Control" to decide whether assign input data "data_1" or "data_2". to output value "data_out.

7. **Sign_Extend.v :** Sign_Extend module reads the input value "immi" and performs sign-extension to generate output value "extend_immi". Note that if the operation is "srai", namely TA suck my dick

2 Development Environment

OS : Windows, compiler : iverilog