Lab3 Report

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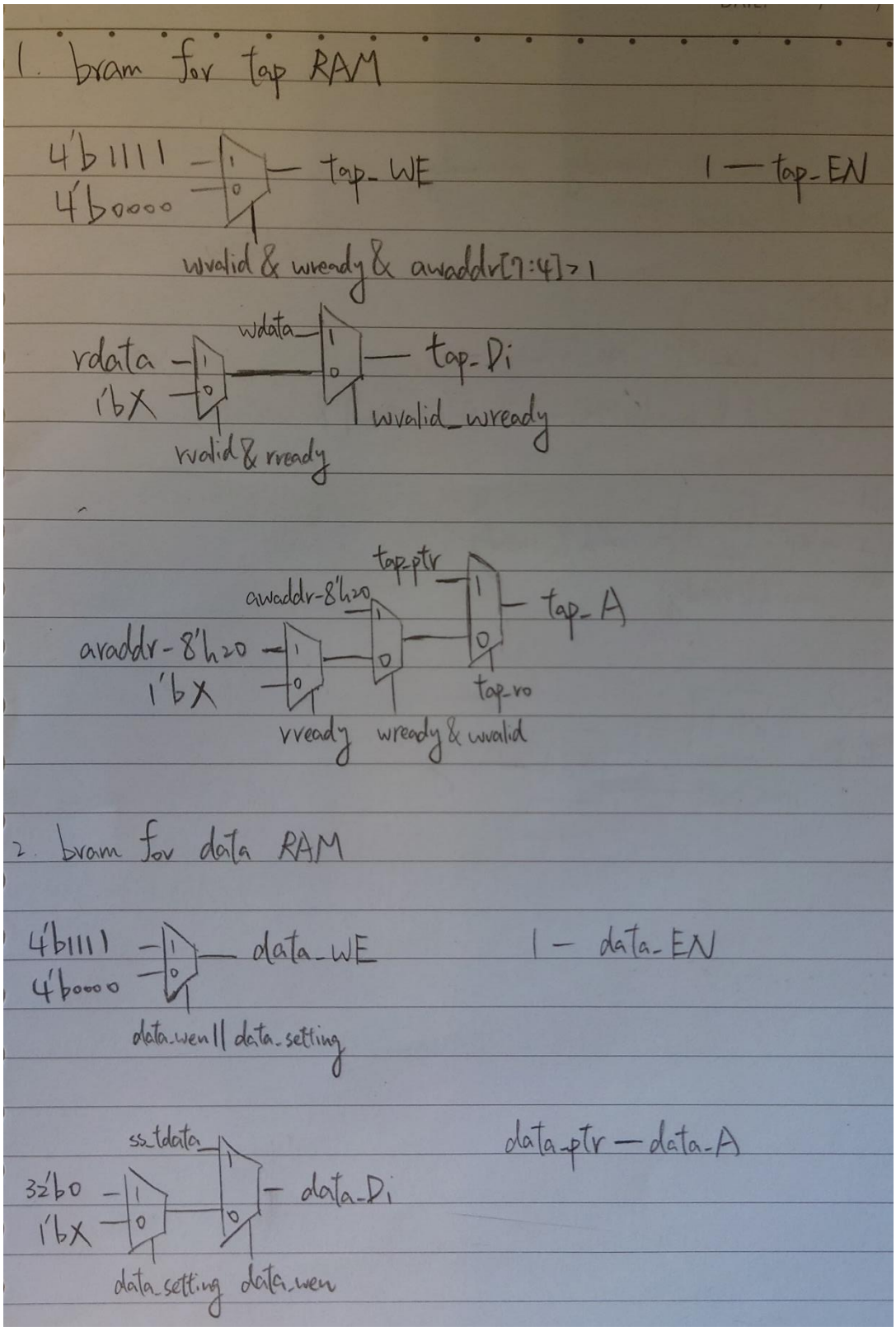
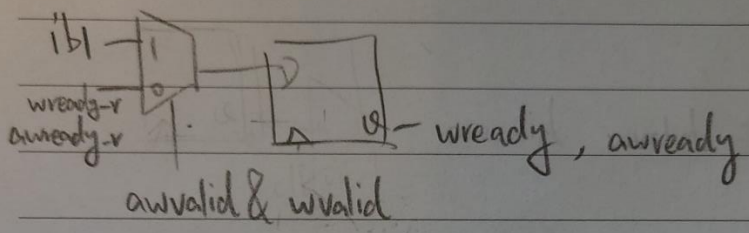
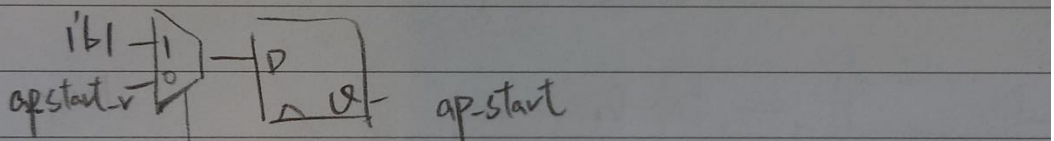
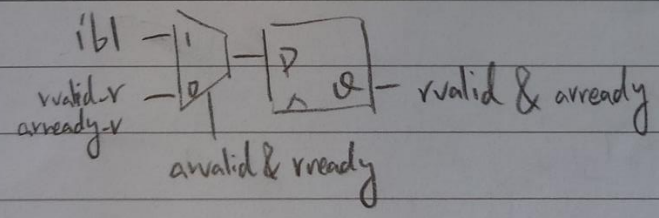
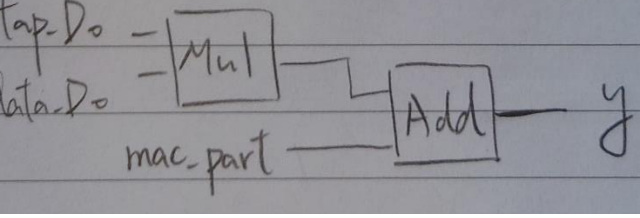
1. Block Diagram

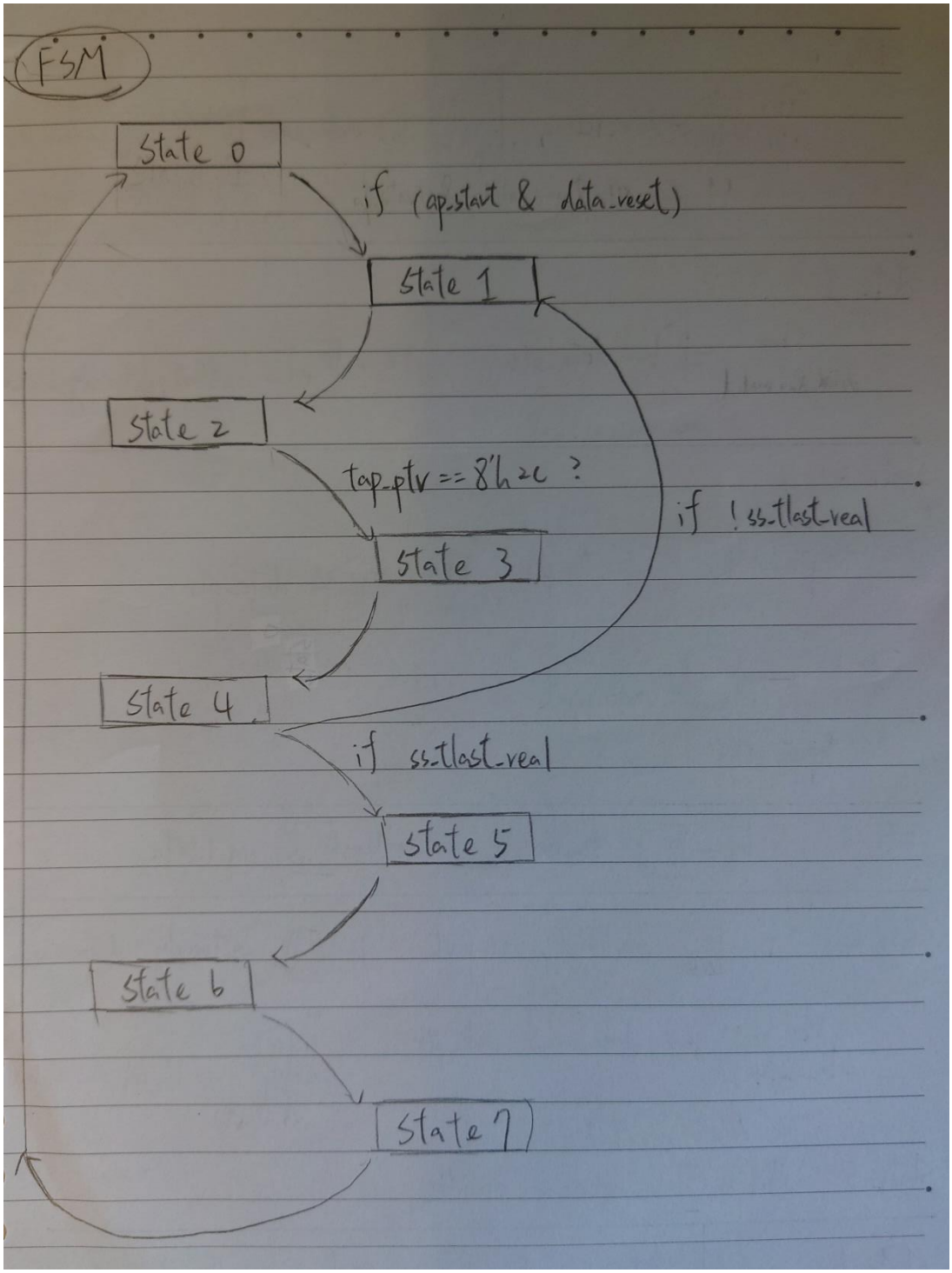



1'b1
wready_r
awready_r
wready, awready
awvalid & wvalid

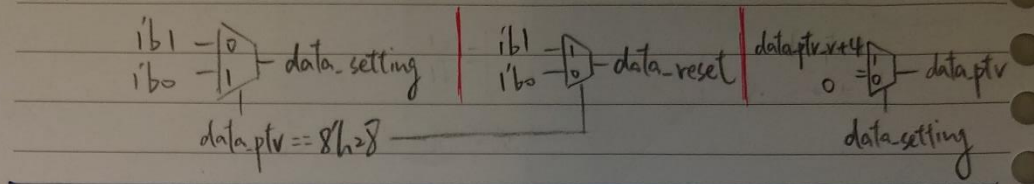

1'b1
ap_start_r
ap_start
awvalid & wvalid & awaddr[7:0] == 0 & state == 0 or 7 & wdata[0]


1'b1
rvalid_r
arready_r
rvalid & arready
arvalid & rready

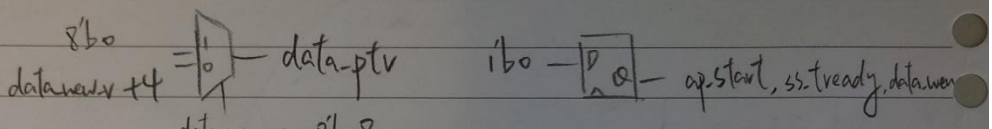

tap_Do
data_Do
Mul
Add
mac_part
y


FSM
State 0
if (ap_start & data_reset)
State 1
State 2
tap_ptr == 8'h2c ?
if !ss_tlast_real
State 3
State 4
if ss_tlast_real
State 5
State 6
State 7

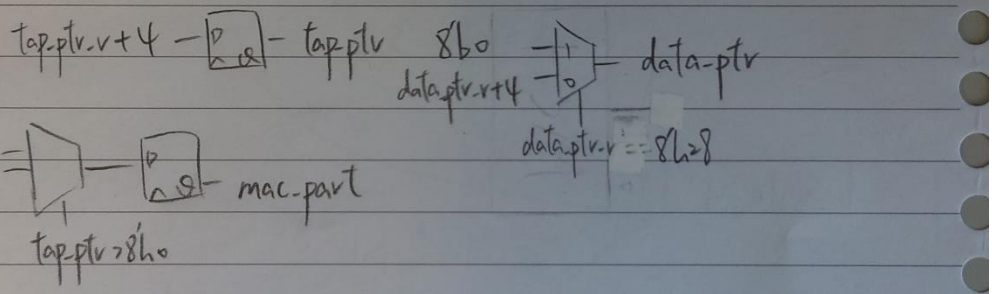
State 0:



State 1:

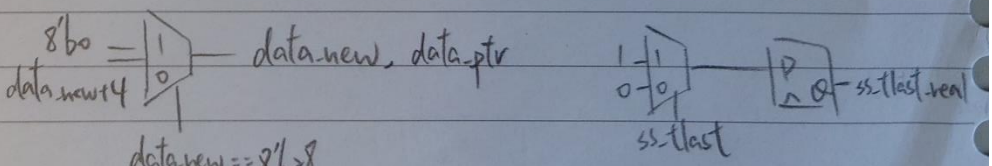


State 2:



State 3: 1'b1 — sm_tvalid mac_part — sm_tdata

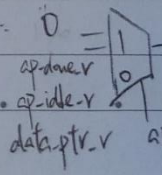
State 4: 0 — sm_tvalid, mac_part 1 — ss_tready, data_wen



State 5: 1'b1 — ap_done, ap_idle

State 6: pass

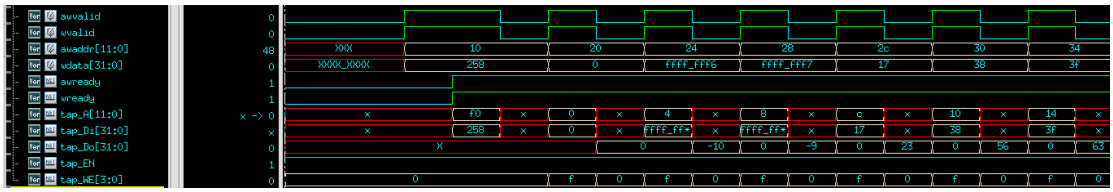
State 7: 0 — ap_done, ap_idle, data_ptr



Per-Duet

2. Describe operation

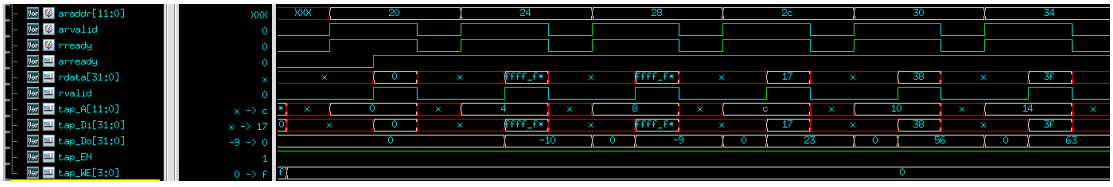
(1)Start the coefficient input (AXI-lite)



在 awvalid 和 wvalid 信號被拉高後，awready 和 wready 信號也會在下一個 cycle 被拉高，表示已經準備好接收 coefficient，接下來 24 個 cycle 總共會有 12 組(awaddr,wdata)傳進來，第一組是 data length，後面 11 組則是相對應的 coefficient。

而 tap bram 方面，tap_A 和 tap_Di 在 valid 和 ready 信號同時拉起時會直接將 awaddr 和 wdata 的資料直接 assign 進去，而 tap_WE 則是除了 valid 和 ready 要是 high 以外，awaddr 還必須是符合 0x20-FF 的形式，也就是接收到的 tap_Di 是真的 tap parameters 的時候，才會拉高 tap_WE，開始將 coefficient 寫入 tap bram。

(2)Check coefficient



在 arvalid 和 rready 信號被拉高後，arready 和 rvalid 信號也會在下一個 cycle 被拉高，表示已經準備好接收想要檢查的 coefficient 並且已經將指定的 coefficient 從 tap bram 拿出並存放到 rdata，由於設計上許多 tap 的信號是利用 assign 完成，所以這邊需要特別注意 rvalid 和 rdata 是否完美的對應到，並且將 rvalid 每次只拉高一個 cycle，避免重複讀取的問題。

而 tap bram 方面，tap_A 在 arvalid 和 rready 信號同時拉起時會直接將 araddr 的資料直接 assign 進去，而由於 tap_EN 永遠是 high 的狀態，tap bram 中指定 address 的資料就會在下一個 cycle 被讀出，並且在 rready 的前提下直接 assign 進 rdata 中，剛好可以對應到 rvalid 被拉高的時機。

Tb 會在 rvalid 被拉高後檢查 rdata 是否符合該 araddr 對應的 coefficient，檢查完 11 筆並完全相同後才真正結束 coefficient input 的步驟。

(3)Start FIR

首先 tb 會將 ap_start 拉高表示 FIR process 的開始，而整個 FIR process 總共會**重複三次**，設計上利用 FSM 控制整個 FIR 的流程。

State 0: Reset

首先會先將 data bram 中的資料 reset，也就是把 bram 中的 11 個 address 中的資料都寫入 0。當這個 reset 的過程完成並且接收到 ap_start 的信號時，就會將 ss_tready 和 data_wen 拉高並進入 state 1。

State 1: Set

這時 data_WE 和 data_Di 因為 data_wen 被拉高的緣故所以分別被 assign 4'b1111 和 ss_tdata，而 data_A 則是經由一個 data pointer(data_ptr)控制，決定這時候的 ss_tdata，也就是 x，應該要存放在哪一個 address，此處的設計是將 x 從第一個位置放到最後一個，然後再從第一個開始放，依序進行。此外，這個 state 會將 ap_start、ss_tready 和 data_wen 的訊號都拉低，再進入 state 2。

State 2: FIR computation

此時 data_Do 會依序將 data bram 裡面資料從最早存入到最晚存入依序讀出，tap_Do 則會將 coefficient 從第一個到最後一個依序輸出，然後每一個 cycle 都會將 tap_Do 乘上 data_Do 然後加上原先 register 中 mac 的 partial 運算值，經過 11 個 cycle 之後 mac_part 即是正確的完整運算結果，此時進入 state 3。

State 3: sm_tdata

此時將 sm_tvalid 拉高並將 mac_part 存入 sm_tdata，進入 state 4。

State 4: Restart FIR

先將 sm_tvalid 拉低，如果 x 尚未傳完，則將 data_ptr 更新到下一個寫入點然後將 ss_tready 和 data_wen 拉高並返回 state 1，否則進入 state 5。

State 5: ap_done & ap_idle

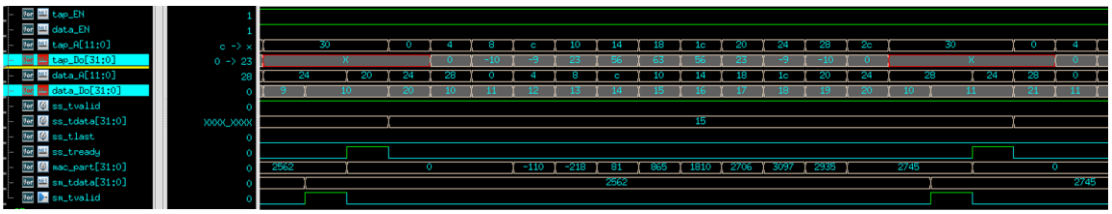
將 ap_done 和 ap_idle 拉高並進入 state 6。

State 6: Pass

直接進入 state 7。

State 7: End

當接收到 ap_start 訊號，重新返回 state 0。



3. Resource usage

LUT	FF	BRAM	URAM	DSP
202	97	0	0	3

```
Detailed RTL Component Info :
+---Adders :
      2 Input   32 Bit       Adders := 1
      2 Input    8 Bit       Adders := 5
+---Registers :
                32 Bit    Registers := 2
                 8 Bit    Registers := 3
                 1 Bit    Registers := 13
+---Multipliers :
               32x32  Multipliers := 1
+---Muxes :
      8 Input   32 Bit        Muxes := 1
      2 Input   32 Bit        Muxes := 5
      2 Input    8 Bit        Muxes := 7
      8 Input    8 Bit        Muxes := 3
      8 Input    3 Bit        Muxes := 1
      2 Input    3 Bit        Muxes := 1
      2 Input    2 Bit        Muxes := 2
      2 Input    1 Bit        Muxes := 6
      8 Input    1 Bit        Muxes := 19
```

4. Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.285 ns	Worst Hold Slack (WHS):	0.137 ns	Worst Pulse Width Slack (WPWS):	5.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	433	Total Number of Endpoints:	433	Total Number of Endpoints:	98

All user specified timing constraints are met.

Clock Summary

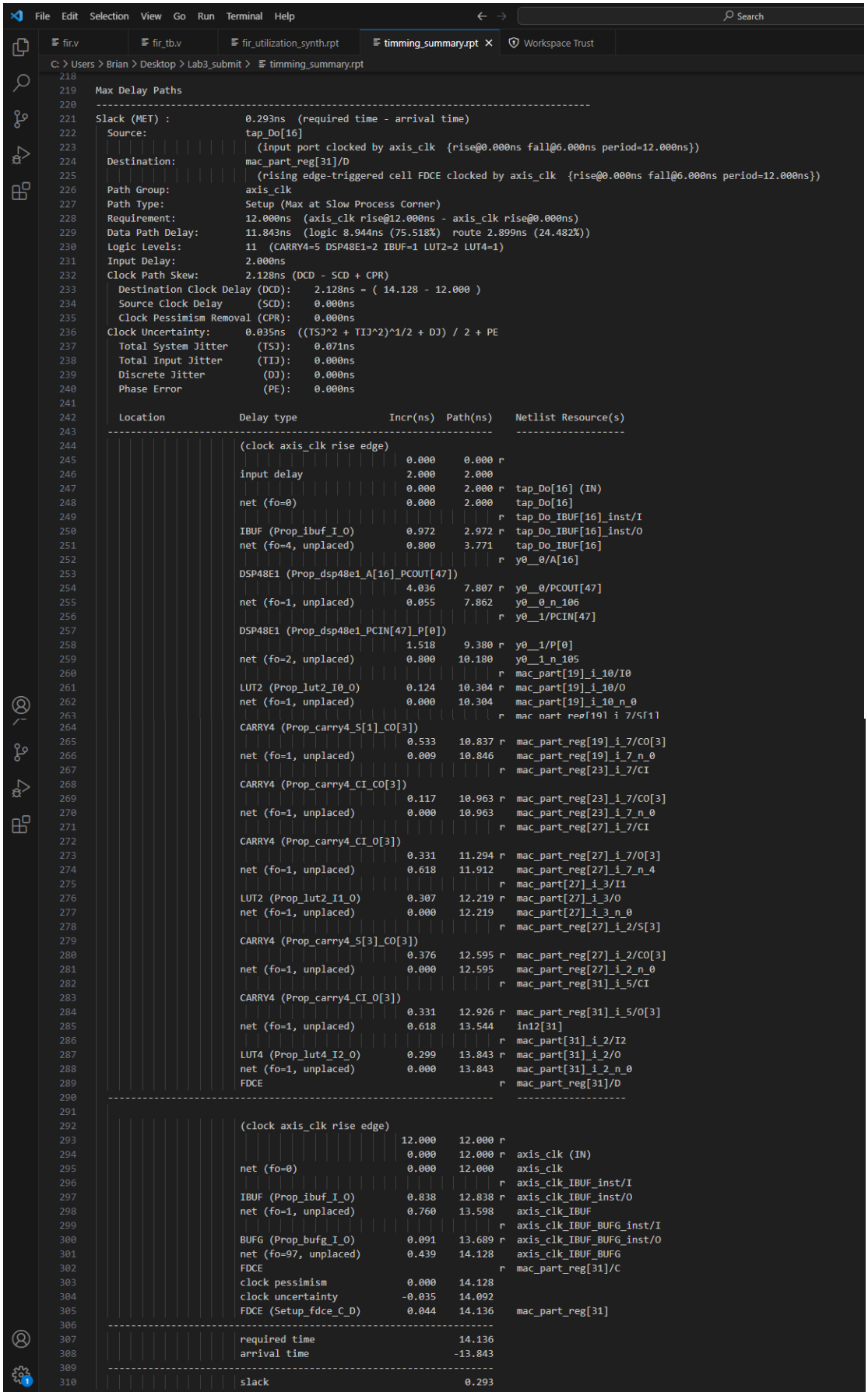
Name	Waveform	Period (ns)	Frequency (MHz)
axis_clk	{0.000 6.000}	12.000	83.333

```
set_input_delay 2.0 [all_inputs]
set_output_delay 0.0 [all_outputs]
```

Max Delay Paths:

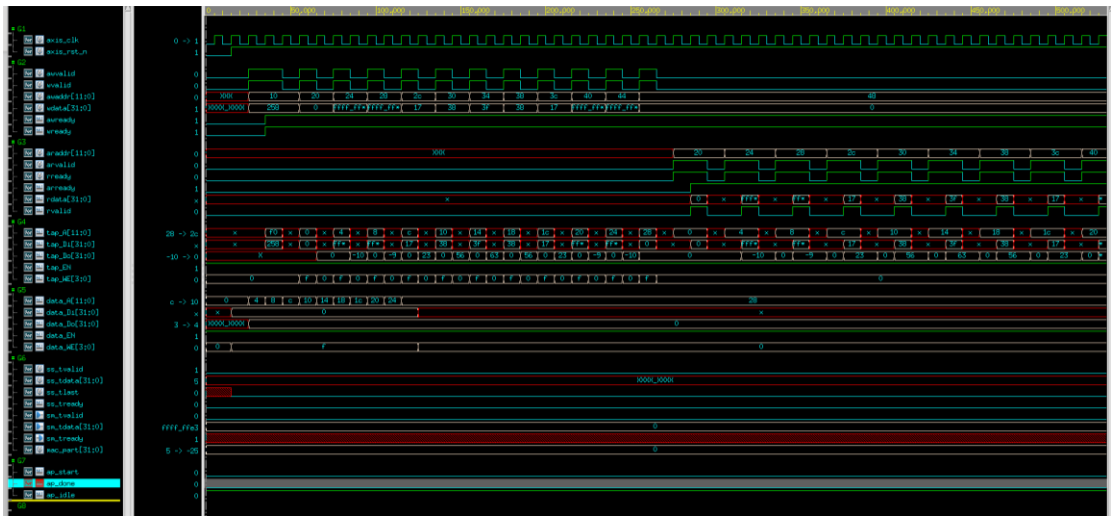
Slack : 0.293 ns

Report :

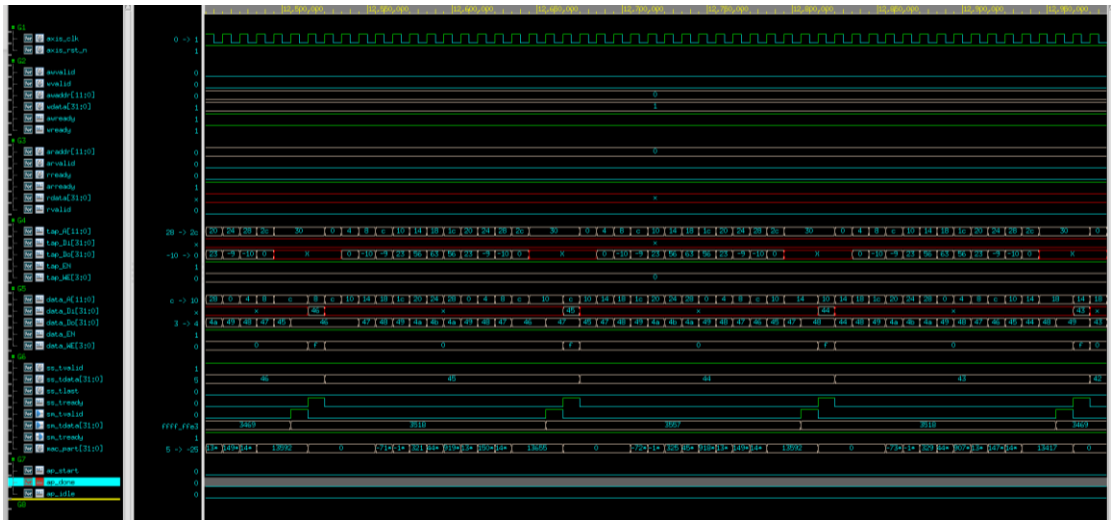

File Edit Selection View Go Run Terminal Help
Search
fir.v
fir_tb.v
fir_utilization_synth.rpt
timming_summary.rpt
Workspace Trust
C: > Users > Brian > Desktop > Lab3_submit > timming_summary.rpt
Max Delay Paths
Slack (MET) : 0.293ns (required time - arrival time)
Source: tap_Do[16]
(input port clocked by axis_clk {rise@0.000ns fall@6.000ns period=12.000ns})
Destination: mac_part_reg[31]/D
(rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@6.000ns period=12.000ns})
Path Group: axis_clk
Path Type: Setup (Max at Slow Process Corner)
Requirement: 12.000ns (axis_clk rise@12.000ns - axis_clk rise@0.000ns)
Data Path Delay: 11.843ns (logic 8.944ns (75.518%) route 2.899ns (24.482%))
Logic Levels: 11 (CARRY4=5 DSP48E1=2 IBUF=1 LUT2=2 LUT4=1)
Input Delay: 2.000ns
Clock Path Skew: 2.128ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): 2.128ns = (14.128 - 12.000)
Source Clock Delay (SCD): 0.000ns
Clock Pessimism Removal (CPR): 0.000ns
Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns
Location Delay type Incr(ns) Path(ns) Netlist Resource(s)
(clock axis_clk rise edge)
0.000 0.000 r
input delay 2.000 2.000
0.000 2.000 r tap_Do[16] (IN)
net (fo=0) 0.000 2.000 tap_Do[16]
r tap_Do_IBUF[16]_inst/I
IBUF (Prop_ibuf_I_O) 0.972 2.972 r tap_Do_IBUF[16]_inst/O
net (fo=4, unplaced) 0.800 3.771 tap_Do_IBUF[16]
r y0__0/A[16]
DSP48E1 (Prop_dsp48e1_A[16]_PCOUT[47])
4.036 7.807 r y0__0/PCOUT[47]
net (fo=1, unplaced) 0.055 7.862 y0__0_n_106
r y0__1/PCIN[47]
DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0])
1.518 9.380 r y0__1/P[0]
net (fo=2, unplaced) 0.800 10.180 y0__1_n_105
r mac_part[19]_i_10/I0
LUT2 (Prop_lut2_I0_O) 0.124 10.304 r mac_part[19]_i_10/O
net (fo=1, unplaced) 0.000 10.304 mac_part[19]_i_10_n_0
r mac_part_reg[19]_i_7/S[1]
CARRY4 (Prop_carry4_S[1]_CO[3])
0.533 10.837 r mac_part_reg[19]_i_7/CO[3]
net (fo=1, unplaced) 0.009 10.846 mac_part_reg[19]_i_7_n_0
r mac_part_reg[23]_i_7/CI
CARRY4 (Prop_carry4_CI_CO[3])
0.117 10.963 r mac_part_reg[23]_i_7/CO[3]
net (fo=1, unplaced) 0.000 10.963 mac_part_reg[23]_i_7_n_0
r mac_part_reg[27]_i_7/CI
CARRY4 (Prop_carry4_CI_O[3])
0.331 11.294 r mac_part_reg[27]_i_7/O[3]
net (fo=1, unplaced) 0.618 11.912 mac_part_reg[27]_i_7_n_4
r mac_part[27]_i_3/I1
LUT2 (Prop_lut2_I1_O) 0.307 12.219 r mac_part[27]_i_3/O
net (fo=1, unplaced) 0.000 12.219 mac_part[27]_i_3_n_0
r mac_part_reg[27]_i_2/S[3]
CARRY4 (Prop_carry4_S[3]_CO[3])
0.376 12.595 r mac_part_reg[27]_i_2/CO[3]
net (fo=1, unplaced) 0.000 12.595 mac_part_reg[27]_i_2_n_0
r mac_part_reg[31]_i_5/CI
CARRY4 (Prop_carry4_CI_O[3])
0.331 12.926 r mac_part_reg[31]_i_5/O[3]
net (fo=1, unplaced) 0.618 13.544 in12[31]
r mac_part[31]_i_2/I2
LUT4 (Prop_lut4_I2_O) 0.299 13.843 r mac_part[31]_i_2/O
net (fo=1, unplaced) 0.000 13.843 mac_part[31]_i_2_n_0
FDCE r mac_part_reg[31]/D
(clock axis_clk rise edge)
12.000 12.000 r
0.000 12.000 r axis_clk (IN)
net (fo=0) 0.000 12.000 axis_clk
r axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O) 0.838 12.838 r axis_clk_IBUF_inst/O
net (fo=1, unplaced) 0.760 13.598 axis_clk_IBUF
r axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O) 0.091 13.689 r axis_clk_IBUF_BUFG_inst/O
net (fo=97, unplaced) 0.439 14.128 axis_clk_IBUF_BUFG
FDCE r mac_part_reg[31]/C
clock pessimism 0.000 14.128
clock uncertainty -0.035 14.092
FDCE (Setup_fdce_C_D) 0.044 14.136 mac_part_reg[31]
required time 14.136
arrival time -13.843
slack 0.293

5. Simulation Waveform

Beginning: coefficient input



FIR process



End: after 3 FIR

6. Simulation log

```
----Start the coefficient input(AXI-lite)----
 Check Coefficient ...
OK: exp =           0, rdata =           0
OK: exp =         -10, rdata =         -10
OK: exp =          -9, rdata =          -9
OK: exp =          23, rdata =          23
OK: exp =          56, rdata =          56
OK: exp =          63, rdata =          63
OK: exp =          56, rdata =          56
OK: exp =          23, rdata =          23
OK: exp =          -9, rdata =          -9
OK: exp =         -10, rdata =         -10
OK: exp =           0, rdata =           0
 Tape programming done ...
----End the coefficient input(AXI-lite)----
 Start FIR
OK: exp =           4, rdata =           4
----Start the data input(AXI-Stream)----
[PASS] [Pattern          0] Golden answer:           0, Your answer:           0
[PASS] [Pattern        100] Golden answer:        9882, Your answer:        9882
[PASS] [Pattern        200] Golden answer:       -8418, Your answer:       -8418
[PASS] [Pattern        300] Golden answer:        -732, Your answer:        -732
[PASS] [Pattern        400] Golden answer:        9882, Your answer:        9882
[PASS] [Pattern        500] Golden answer:       -8418, Your answer:       -8418
[PASS] [Pattern        597] Golden answer:       -1281, Your answer:       -1281
OK: exp =           0, rdata =           0
[PASS] [Pattern        598] Golden answer:       -1098, Your answer:       -1098
------End the data input(AXI-Stream)------
[PASS] [Pattern        599] Golden answer:        -915, Your answer:        -915
OK: exp =           2, rdata =           6
OK: exp =           4, rdata =           6
-----------------------------------------------
-----------Congratulations! Pass-------------
OK: exp =           4, rdata =           6
----Start the data input(AXI-Stream)----
[PASS] [Pattern          0] Golden answer:           0, Your answer:           0
[PASS] [Pattern        100] Golden answer:        9882, Your answer:        9882
[PASS] [Pattern        200] Golden answer:       -8418, Your answer:       -8418
[PASS] [Pattern        300] Golden answer:        -732, Your answer:        -732
[PASS] [Pattern        400] Golden answer:        9882, Your answer:        9882
[PASS] [Pattern        500] Golden answer:       -8418, Your answer:       -8418
[PASS] [Pattern        597] Golden answer:       -1281, Your answer:       -1281
OK: exp =           0, rdata =           0
[PASS] [Pattern        598] Golden answer:       -1098, Your answer:       -1098
------End the data input(AXI-Stream)------
[PASS] [Pattern        599] Golden answer:        -915, Your answer:        -915
OK: exp =           2, rdata =           6
OK: exp =           4, rdata =           6
-----------------------------------------------
-----------Congratulations! Pass-------------
OK: exp =           4, rdata =           6
----Start the data input(AXI-Stream)----
[PASS] [Pattern          0] Golden answer:           0, Your answer:           0
[PASS] [Pattern        100] Golden answer:        9882, Your answer:        9882
[PASS] [Pattern        200] Golden answer:       -8418, Your answer:       -8418
[PASS] [Pattern        300] Golden answer:        -732, Your answer:        -732
[PASS] [Pattern        400] Golden answer:        9882, Your answer:        9882
[PASS] [Pattern        500] Golden answer:       -8418, Your answer:       -8418
[PASS] [Pattern        597] Golden answer:       -1281, Your answer:       -1281
OK: exp =           0, rdata =           0
[PASS] [Pattern        598] Golden answer:       -1098, Your answer:       -1098
------End the data input(AXI-Stream)------
[PASS] [Pattern        599] Golden answer:        -915, Your answer:        -915
OK: exp =           2, rdata =           6
OK: exp =           4, rdata =           6
-----------------------------------------------
-----------Congratulations! Pass-------------
```