ITSc 3181 - Problem Set #5

- 5.1.1: 2 32-bit integers can be stored in a 16-byte cache block.
- 5.1.2: Variables = I, J, B[I][0]
- 5.1.3: Variables = A[I][J]
- 5.2.1:

Word Address	Binary Address	Tag	Index	Hit/miss
0x03	0000 0011	0	3	m
0xb4	1011 0100	b	4	m
0x2b	0010 1011	2	b	m
0x02	0000 0010	0	2	m
0xbf	1011 1111	b	f	m
0x58	0101 1000	5	8	m
0xbe	1011 1110	b	e	m
0x0e	0000 1110	0	e	m
0xb5	1011 0101	b	5	m
0x2c	0010 1100	2	c	m
0xba	1011 1010	b	a	m
0xfd	1111 1101	f	d	m

- 5.2.2:

Word Address	Binary Address	Tag	Index	offset	Hit/miss
0x03	0000 0011	0	1	1	m
0x64	0110 0100	6	2	0	m
0x26	0010 0110	2	5	1	m
0x02	0000 0010	0	1	0	H
0x6F	0110 1111	6	7	1	m
0x58	0101 1000	5	4	0	m
0x6e	0110 1110	6	6	0	H
0x0e	0000 1110	0	7	0	m
0x65	0110 0101	6	2	1	H
0x2c	0010 1100	2	6	0	m
0x6a	0110 1010	6	5	0	m
0xFd	1111 1101	F	6	1	m

- 5.3.1: 1 word = 8 bytes, 1 block = 2 words, 1 block = 16 bytes
The cache contains $2^{15} \cdot 8$ bits of data plus
$2^{11} \cdot 49$ bits of tag plus 2^{11} valid bits
Cache block size = 364, 544 bits

- 5.3.2: 1 64-bit address divides into: a 3-bit word offset, a 4-bit block offset, a 9-bit index, & a 48 bit tag
The cache contains $2^{16} \cdot 8$ bits of data plus $2^9 \cdot 48$ bits of tag plus 2^9 valid bits = 549, 376 bits

- 5.3.3 : A larger cache blocke size requires an increased hit time & an increased miss penalty than the original cache. The fewer number of blocks causes a higher conflict miss rate than the original cache.

- 5.6.1 : Clock rate for P1 Processor = 1/0.66 = 1.515 GHz
  Clock rate for P2 Processor = 1/0.9 = 1.11 GHz

- 5.6.2 : P1 = 0.66 + (89·70) = 0.66 + 5.6 = 6.26 ns
  P2 = 0.9 + (69·70) = 0.90 + 4.2 = 5.1 ns

- 5.6.3 : P1 = 1 + [(70·89)/0.66] · 0.36 = 4.054
  P2 = 1 + [(70·69)/0.90] · 0.36 = 2.68

- 5.12.1 : VA = 43 bits, VA memory size = 2^{43},
  Page size = 2^{12}

  PTE = 2^{31}, PTE size = 2^2

  Physical memory needed = 2^{33}