|  |  |
| --- | --- |
| **Freescale Semiconductor** | Document |
| LDPAA AIOP SERVICE LAYER | Number: AIOPSLRN |
| Release Notes for LDPAA AIOP Service Layer Alpha v0.5.3.0 | Doc. Rev. 0.1 Jan 8, 2015 |

**LDPAA AIOP SERVICE LAYER ALPHA V0.5.3.0**

**Release Notes**

Contents

[1. Overview 2](#_Toc408497200)

[2. Compatibility List 3](#_Toc408497201)

[3. New Features 3](#_Toc408497202)

[4. Changes 4](#_Toc408497203)

[5. Quick Start with this release 4](#_Toc408497204)

[6. Contact Information 4](#_Toc408497205)

[7. Bug Fixes 5](#_Toc408497206)

[8. Workarounds for HW Bugs 5](#_Toc408497207)

[9. Known Limitations/ Issues 5](#_Toc408497208)

[9.1 General Limitations 5](#_Toc408497209)

[9.2 Error Support Limitation 6](#_Toc408497210)

[9.3 Known problems 7](#_Toc408497211)

[9.4 Tools known issues 7](#_Toc408497212)

1. Overview

This document describes the main updates included in the LDPAA AIOP Service Layer Alpha v0.5.3.0 as compared with v0.5.2.0

Applications should use the APIs in: aiopsl/src/include/

All other APIs are internal to the Service Layer and should not be called by applications.

The API may be changed in future releases.

The API may be updated in future releases to align with the latest HW specs.

This release can be retrieved from GIT:

GIT repository: ssh://gerrit/ldpaa/aiopsl/

GIT tag: **ldpaa-aiop-sl-v0.5.3.0**

Please see the aiopsl/docs/AIOPCoreLib\_ChangeLog.txt and aiopsl/docs/AIOP\_ARENA\_ChangeLog.txt files for a detailed list of changes.

Please subscribe to the AIOPSREL mailing list to receive future release notifications.

1. Compatibility List

This release is bit accurate with respect to the following docs/tools.

As such, it is suitable for running on RTL/Emulator/Simulator.

|  |  |
| --- | --- |
| **Tool/Doc** | **Version** |
| AIOP\_Archdef | 0.8.0 |
| FD\_section | 0.62.3 |
| CTLU\_AIOP\_bg | 0.7.4 |
| TMan | 1.0 |
| Parser\_Block\_Guide | 3.090 |
| AIOP\_Instruction\_Additions | 1.1 |
| Compiler | Build 293 |
| CW for DPAA | 10.0.14 |
| Simulator | m0128 |
| MC Firmware | 0.5.3 |
| PowerISA | 2.06 |
| AIOP\_z490\_CPU\_Specification | Rev1.2 |
|  |  |

1. New Features

The following new features have been added since version 0.5.2.0:

* GPP-AIOP Communication
  + GPP-API shared buffer pools. (ENGR00338056)
  + Command Interface session close. (ENGR00341799)
  + Command Interface user callback function provided upon command send. (ENGR00341805)
  + AIOP Isolation Context query.
  + GPP Isolation Context query. (ENGR00343801)
* Memory Management
  + User-confi**g**urable Slab buffer sizes and quantities. (ENGR00341806, ENGR00340987, ENGR00341820)
  + Support more than 1000 slab pools. (ENGR00341802)
  + Support committed/max allocation scheme. (ENGR00341821)
  + Allocation from System DDR. (ENGR00341798)
* Network Interfaces
  + Storage Profile attributes query. (ENGR00344464)
  + Connected NI query. (ENGR00341214)
* Code Placement
  + File-level code placement macros (ENGR00344073)
* Error Handling
  + Fatal Error Handler prints information prepared by Service Routines. (ENGR00341990)
* Support Service routines errors according to section 9.2
* Support Functional Module errors according to section 9.2
* New HM commands:
  + l4\_set\_tcp\_src() - replace TCP source port
  + l4\_set\_tcp\_dst() - replace TCP destination port
  + l4\_set\_udp\_src() - replace UDP source port
  + l4\_set\_udp\_dst() - replace UDP destination port
* IPR:
  + Timeout functionality.
  + IPR statistics.
  + Support malformed fragments: overlap and duplicate.
  + Support for errors: max reassembled frame size, min fragment size.
  + ECN compliance
* Workarounds for HW Bugs as detailed in section 8

1. Changes

The following are changes from version v0.5.2.0:

* The layout file has been updated.
* BMan buffer pools are no longer filled up by ARENA. This must be done by applications during early initialization.
* SL initialization includes buffer registration needed for IPR and IPsec functional modules. 750 buffers are initialized for each of these modules. In the future a dedicated API for setting number of buffers for IPR and IPSec will be added.
* Memory attributes of GPP-AIOP shared memory must be configured by the GPP to match AIOP.
* The deprecated memory management functions have been removed.
* The Command Interface API has been updated.
* The Slab API has been updated. (ENGR00341803)
* For Command Interface and Shared Buffer Pool flibs integration and testing on GPP, please follow instructions in aiopsl\tests\cmdif\README.txt.

Please see the aiopsl/docs/AIOPCoreLib\_ChangeLog.txt and aiopsl/docs/AIOP\_ARENA\_ChangeLog.txt files for a detailed list of changes.

1. Quick Start with this release

Please see the README.txt file at aiopsl\build\aiop\_ sim\apps\app\_process\_packet\src\ for running instructions.

1. Contact Information

* Mail List: **AIOPSREL**
* Bug Reporting [Clear Quest](http://cq.freescale.net/cqweb/) BINs: **LS-AIOP-LOW-LEVEL** and **LS-ARENA**

1. Bug Fixes

The following are bugs fixed in this release since version v0.5.2.0

* Command Interface
  + AIOP CMDIF client should change the WS to have AIOP icontext before calling async callback (ENGR00344241)
  + Function inst\_alloc() error in cmdif\_srv.c file (ENGR00343203)
  + AIOP-GPP and MC-GPP dpci setup does not support high/low priorities. (ENGR00342149)
* Parser
  + The checksum of an IPV6 UDP frame is reported error by AIOP parser (ENGR00341594)
* IPR:
  + IPv6 fails due to incorrect checksum. (ENGR00341098)
  + L4 checksum validation for IPv4 frames with padding different than 0. (ENGR00342190)
* GRO:
  + Max size limit counter is not incremented. (ENGR00339198)
* IPsec:
  + CCM Encryption is not supported. (ENGR341153)

1. Workarounds for HW Bugs

The following SW workarounds have been added in this release.

* FDMA
  + FDMA Replace Working Frame Segment returns unexpected representation (TKT237377)
* IPF/GSO
  + FDMA split sequence return incorrect data (TKT240996)
* TABLE
  + Table delete never completes (TKT226361).
* TMAN
  + HW bug in delete TMI (TKT008205)
  + HW issue in TMI create command (TKT226418)

1. Known Limitations/ Issues

## General Limitations

* The fsl\_os\_print() function is limited to strings smaller than 80 characters when called at runtime.
* The number of tasks per core should not be set to a value greater than 4 since some AIOP SL functions have not yet been optimized for minimal stack usage.
* The Parser does not support the Invalid HXS error code (shown in the Parser Block Guide version 3.090).
* Packets without L2 Ethernet header are not supported due to a hardware bug (TKT237150).
* The SEGMENT\_OFFSET field in the Presentation Context must be set to 0. This means that a frame must be presented from its first byte.
* The maximum key size allowed is 80 bytes due to a hardware bug (TKT231187).
* Presentation size should not exceed 256 bytes due to a CTLU HW bug (TKT228731).
* Parser: PARSER\_HW\_STATUS\_INVALID\_SOFT\_PARSE\_INSTRUCTION error is not covered since there is no way to download code to the parser memory.

## Error Support Limitation

* FDMA errors are not supported.
* HM errors are not supported.
* Keygen:
  + Only FECIDs 0 to 23 are verified.
* TMAN:
  + TMAN\_TMI\_BUS\_ERR is not verified.
  + tman\_create\_timer function EBUSY error cannot be verified by the simulator.
  + TMAN\_TMI\_PURGED Fatal error cannot be verified by the simulator.
* CDMA
  + The following CDMA errors were not verified due to a simulator issue:
    - CDMA\_REFCOUNT\_INVALID\_OPERATION\_ERR (ENGR00344456)
  + The following CDMA errors cannot be verified by the simulator:
    - CDMA\_INTERNAL\_MEMORY\_ECC\_ERR
    - CDMA\_SYSTEM\_MEMORY\_READ\_ERR
    - CDMA\_SYSTEM\_MEMORY\_WRITE\_ERR
    - CDMA\_INTERNAL\_ERR
  + The following CDMA errors cannot be verified:
    - CDMA\_MUTEX\_LOCK\_FAILED
    - CDMA\_INVALID\_DMA\_COMMAND\_ARGS\_ERR
    - CDMA\_REFCOUNT\_INCREMENT\_ERR
* The following OSM errors cannot be verified:
  + Relinquish concurrent
  + Enter scope exhausted
  + Duplicate scope identifier detected
* IPR
  + Errors returned by SR are not supported.

## Known problems

* IPsec:
  + IPSec FLIB RTA does not support correct endianess (ENGR338051).  
    IPSec works on simulator with flag caam.ENGR00330235\_fix=false
  + Transport mode does not support IPv6. (ENGR342116)
  + Copy DSCP from inner header to outer header is not supported. (ENGR341311)
  + GCM16 is not supported (ENGR341892)

## Tools known issues

The below are known simulator and other tools issues which cause limitations in the Service Layer.

* Keygen:
  + KCR is not able to extract ARP header related fields properly (ENGR341315)
  + The ARP\_OP fec is not able to extract ARP header related fields properly (ENGR344244)
  + The KSE bit should be set while the generated key size is larger than 124 bytes (ENGR344457)
  + The MPLSL\_2 fec is not able to extract MPLS header related fields properly (ENGR344479).
  + The IPID\_1 fec is not able to extract IP Identification field properly (ENGR344576)
  + The IPv6FL\_1 fec is not able to extract IPv6 Flow Label field properly (ENGR344674)
* IPF and GSO:
  + Original frame's buffer doesn't acquire correct after split command (ENGR344334).
* STE
  + AXI Outbound Read Transfer Error cannot be verified due to simulator issue (ENGR329755)
  + Outbound Write Transfer Error cannot be verified due to simulator issue (ENGR329755)
* TMAN
  + Return status error for timer created command after tmi is deleted without ccp (ENGR00341715)
* IPsec:
  + Incorrect handling of IP Header in IPSec protocol descriptor Block (ENGR330235)
  + CAAM/SEC: transport mode decapsulation output frame IP header length field and payload data error (ENGR340827)
  + CAAM/SEC: reuse buffer mode decryption error (ENGR342843)
  + CAAM/SEC: CCM algorithm decapsulation output is illegal frame (ENGR342871)
  + CAAM/SEC: SEC use a wrong IP header length to get N field offset (ENGR343388)
  + Decapsulation ICV check failure (ENGR344126)
  + CAAM/SEC: padding length error then get a wrong byte count (ENGR344062)
  + CAAM/SEC: padding length error then get a wrong byte count (ENGR344253)
  + GCM12 decapsulation padding check error (GCM12 decapsulation padding check error)
  + seq number update error (ENGR344281)
  + CAAM/SEC:SEC output bytecount is zero (ENGR344347)
  + descriptor corrupted (ENGR343926)

***How to Reach Us:***

**Home Page:**

www.freescale.com

**email:**

support@freescale.com

**USA/Europe or Locations Not Listed:**

Freescale Semiconductor

Technical Information Center, CH370

1300 N. Alma School Road

Chandler, Arizona 85224

(800) 521-6274

480-768-2130

support@freescale.com

**Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH

Technical Information Center

Schatzbogen 7

81829 Muenchen, Germany

+44 1296 380 456 (English)

+46 8 52200080 (English)

+49 89 92103 559 (German)

+33 1 69 35 48 48 (French)

support@freescale.com

**Japan:**

Freescale Semiconductor Japan Ltd.

Headquarters

ARCO Tower 15F

1-8-1, Shimo-Meguro, Meguro-ku

Tokyo 153-0064, Japan

0120 191014

+81 2666 8080

support.japan@freescale.com

**Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.

Technical Information Center

2 Dai King Street

Tai Po Industrial Estate,

Tai Po, N.T., Hong Kong

+800 2666 8080

support.asia@freescale.com

**For Literature Requests Only:**

Freescale Semiconductor

Literature Distribution Center

P.O. Box 5405

Denver, Colorado 80217

(800) 441-2447

303-675-2140

Fax: 303-675-2150

LDCForFreescaleSemiconductor

@hibbertgroup.com

Information in this document is provided solely to enable system and software

implementers to use Freescale Semiconductor products. There are no express or

implied copyright licenses granted hereunder to design or fabricate any integrated

circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to

any products herein. Freescale Semiconductor makes no warranty, representation or

guarantee regarding the suitability of its products for any particular purpose, nor does

Freescale Semiconductor assume any liability arising out of the application or use of

any product or circuit, and specifically disclaims any and all liability, including without

limitation consequential or incidental damages. “Typical” parameters which may be

provided in Freescale Semiconductor data sheets and/or specifications can and do

vary in different applications and actual performance may vary over time. All operating

parameters, including “Typicals” must be validated for each customer application by

customer’s technical experts. Freescale Semiconductor does not convey any license

under its patent rights nor the rights of others. Freescale Semiconductor products are

not designed, intended, or authorized for use as components in systems intended for

surgical implant into the body, or other applications intended to support or sustain life,

or for any other application in which the failure of the Freescale Semiconductor product

could create a situation where personal injury or death may occur. Should Buyer

purchase or use Freescale Semiconductor products for any such unintended or

unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor

and its officers, employees, subsidiaries, affiliates, and distributors harmless against all

claims, costs, damages, and expenses, and reasonable attorney fees arising out of,

directly or indirectly, any claim of personal injury or death associated with such

unintended or unauthorized use, even if such claim alleges that Freescale

Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

The described product contains a PowerPC processor core. The PowerPC name is a

trademark of IBM Corp. and used under license. All other product or service names are

the property of their respective owners.

© Freescale Semiconductor, Inc., 2005-2014.