|  |  |
| --- | --- |
| **Freescale Semiconductor** | Document |
| LDPAA AIOP SERVICE LAYER | Number: AIOPSLRN |
| Release Notes for LDPAA AIOP Service Layer v1088\_ENG\_0.1 | Doc. Rev. 0.1 Jul 30, 2015 |

**LDPAA AIOP SERVICE LAYER for LS1088 ENG v0.1**

**Release Notes**

Contents

[1. Overview 2](#_Toc425941844)

[2. Compatibility List 3](#_Toc425941845)

[3. New Features 3](#_Toc425941846)

[4. Changes 3](#_Toc425941847)

[5. Quick Start with this Release 4](#_Toc425941848)

[6. Contact Information 4](#_Toc425941849)

[7. Bug Fixes 4](#_Toc425941850)

[8. Workarounds for HW Bugs 4](#_Toc425941851)

[9. Known Limitations/ Issues 5](#_Toc425941852)

[9.1 General Limitations 5](#_Toc425941853)

[9.2 Known problems 5](#_Toc425941854)

[9.2.1 Supported IPsec Encryption Algorithms 5](#_Toc425941855)

[9.2.2 Supported IPsec Authentication Algorithms 6](#_Toc425941856)

[9.3 Tools known issues 6](#_Toc425941857)

1. Overview

This document targets LS1088 and describes the main updates included in the LDPAA AIOP Service Layer v1088\_ENG\_0.1 as compared with v0.7.1.0

Applications should use the APIs in CW libraries under: aiops\include\ of the LS1088a rev1 Code Warrior .project located under aiopsl\build\ls1088a\rev1\aiopsl.

All other APIs are internal to the Service Layer and should not be called by applications.

The API may be changed in future releases.

This release can be retrieved from GIT:

GIT repository: <http://sw-stash.freescale.net/scm/dpaa2/aiopsl.git>

GIT tag: **aiop\_release\_1088\_ENG\_0.1**

Please see the aiopsl/docs/AIOPCoreLib\_ChangeLog.txt and aiopsl/docs/AIOP\_ARENA\_ChangeLog.txt files for a detailed list of changes.

Please subscribe to the AIOPSREL mailing list to receive future release notifications.

1. Compatibility List

This release is compatible with the following SW, Tools:

|  |  |
| --- | --- |
| **SW/Tool** | **Version** |
| CW for DPAA | CW\_NetApps\_v2015.08 |
| Simulator | LS\_SIM\_f0137\_150723 |
| MC Firmware | 1088\_ENG\_0.1 |
|  |  |

1. New Features

The following new features have been added since version v0.7.1.0:

* AIOP SL has been ported to run on the LS1088 simulator.
* Keygen
  + Added FECID 0x25 (KEYGEN\_KCR\_ICMP\_TYPE\_FECID) and FECID 0x26 (KEYGEN\_KCR\_ICMP\_CODE\_FECID) which were not supported in REV1 due to TKT241788.
* Parser
  + Added VXLAN support
  + Parse result additions:
    - nxt\_hdr\_before\_ipv6\_frag\_ext
    - ip\_n\_pid\_offset
* Statistics Engine
  + Add STE registers macros (TKT224651).
* TMAN
  + Added tman\_query\_tmi() (TKT226418).
  + Added tman\_modify\_timer() (TKT226418).
  + Added return value for tman\_recharge\_timer() (TKT258245).
* Memory Manager
  + Dependency on DP-DDR has been removed. (ENGR00342657)
  + Added API for checking whether a memory exists - fsl\_mem\_exists().

1. Changes

The following are changes from version v0.7.1.0 which are not backward compatible:

* Table:
  + Removed internal memory location and DP-DDR memory locations for tables. (Not available for 1088)
* RCU Sync:
  + RCU Sync functionality has been removed for LS1088.
* Network Interfaces
  + The following deprecated APIs have been removed: dpni\_drv\_get\_connected\_dpni\_id(), dpni\_drv\_get\_connected\_aiop\_ni\_id() (ENGR00362002)

The following are additional changes from version v0.7.1.0:

* IPR, IPF, I GRO & GSO:
  + Remove following requirement:

"As part of a workaround to ticket TKT260685 in REV1 this function requires one of the four nested scope levels."

Please see the aiopsl/docs/AIOPCoreLib\_ChangeLog.txt and aiopsl/docs/AIOP\_ARENA\_ChangeLog.txt files for a detailed list of changes.

1. Quick Start with this Release

Please see the README.txt file at aiopsl\apps\app\_process\_packet\ for running instructions.

1. Contact Information

* Mail List: **AIOPSREL**
* Bug Reporting [Clear Quest](http://cq.freescale.net/cqweb/) BINs: **LS-AIOP-LOW-LEVEL** and **LS-ARENA**

1. Bug Fixes

The following are bugs fixed in this release since version v0.7.1.0:

* TMAN:
  + Remove shared memory array for TKT226418 (max number of timers).
  + Add exception error cases (TKT226701).
* Command Interface:
  + inst\_alloc can't allocate all instances (ENGR00361727)

1. Workarounds for HW Bugs

The following workarounds were removed in this release:

* IPF, GRO, GSO:
  + Removed workaround for TKT240996 (FDMA split)
* FDMA:
  + Remove workaround for TKT237377 (preserve segment boundaries on replace commands)
  + Remove workaround for TKT260685 (FDMA locks up under high load and certain operating conditions)
* Frame Operations:
  + Remove workaround for TKT254401 (creating a new frame)
* Table:
  + Remove workaround for TKT226361 (mflu delete table issue)
* TMAN:
  + Remove workaround for TKT226418 (tman\_delete\_tmi).
  + Remove workaround for TKT254640 (tman\_create\_tmi).
* Core:
  + SW workaround for wrong e200 PVR register content (ENGR00346193)

No additional SW workarounds have been added in this release.

1. Known Limitations/ Issues

## General Limitations

* This release was only tested with IPF/IPR Demo.
* The Event Manager and Dynamic DPNI/DPCI Configuration features have been unit-tested only. Integration tests involving GPP SW were not performed yet.
* The fsl\_os\_print() function is limited to strings smaller than 80 characters when called at runtime.
* The SEGMENT\_OFFSET field in the Presentation Context must be set to 0. This means that a frame must be presented from its first byte.

## Known problems

* IPR:
  + ENGR362035 : upon malformed fragment handling, wrong address buffer may be returned to BMAN.
  + ENGR00363687 : wrong handling of IPv6 atomic fragments
* IPsec is not supported due to simulator ticket ENGR363782

## Tools known issues

The below are known simulator and other tools issues which cause limitations in the Service Layer.

* Keygen
  + ENGR362236 VF filed issue in multi PS FECIDs
* WRIOP:
  + ENGR00363659 - WRIOP simulator does not support SGE of type frame\_format = 2
* IPsec
  + SEC seems to be not functional for LS1088 device (ENGR363782 )
  + CAAM/SEC: The AES-NULL-WITH-GMAC algorithm is not supported in transport mode (ENGR00361214)
  + CAAM/SEC: For AES-NULL-WITH-GMAC algorithm, the kilobytes counter is not consistent with board (ENGR00361340)
  + CAAM/SEC: The simulator get the wrong outer header length causes the decapsulation failed (ENGR00361341)
  + CAAM/SEC: The simulator goes into an infinite loop when enable the buffer reuse mode (ENGR00360053)

***How to Reach Us:***

**Home Page:**

www.freescale.com

**email:**

support@freescale.com

**USA/Europe or Locations Not Listed:**

Freescale Semiconductor

Technical Information Center, CH370

1300 N. Alma School Road

Chandler, Arizona 85224

(800) 521-6274

480-768-2130

support@freescale.com

**Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH

Technical Information Center

Schatzbogen 7

81829 Muenchen, Germany

+44 1296 380 456 (English)

+46 8 52200080 (English)

+49 89 92103 559 (German)

+33 1 69 35 48 48 (French)

support@freescale.com

**Japan:**

Freescale Semiconductor Japan Ltd.

Headquarters

ARCO Tower 15F

1-8-1, Shimo-Meguro, Meguro-ku

Tokyo 153-0064, Japan

0120 191014

+81 2666 8080

support.japan@freescale.com

**Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.

Technical Information Center

2 Dai King Street

Tai Po Industrial Estate,

Tai Po, N.T., Hong Kong

+800 2666 8080

support.asia@freescale.com

**For Literature Requests Only:**

Freescale Semiconductor

Literature Distribution Center

P.O. Box 5405

Denver, Colorado 80217

(800) 441-2447

303-675-2140

Fax: 303-675-2150

LDCForFreescaleSemiconductor

@hibbertgroup.com

Information in this document is provided solely to enable system and software

implementers to use Freescale Semiconductor products. There are no express or

implied copyright licenses granted hereunder to design or fabricate any integrated

circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to

any products herein. Freescale Semiconductor makes no warranty, representation or

guarantee regarding the suitability of its products for any particular purpose, nor does

Freescale Semiconductor assume any liability arising out of the application or use of

any product or circuit, and specifically disclaims any and all liability, including without

limitation consequential or incidental damages. “Typical” parameters which may be

provided in Freescale Semiconductor data sheets and/or specifications can and do

vary in different applications and actual performance may vary over time. All operating

parameters, including “Typicals” must be validated for each customer application by

customer’s technical experts. Freescale Semiconductor does not convey any license

under its patent rights nor the rights of others. Freescale Semiconductor products are

not designed, intended, or authorized for use as components in systems intended for

surgical implant into the body, or other applications intended to support or sustain life,

or for any other application in which the failure of the Freescale Semiconductor product

could create a situation where personal injury or death may occur. Should Buyer

purchase or use Freescale Semiconductor products for any such unintended or

unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor

and its officers, employees, subsidiaries, affiliates, and distributors harmless against all

claims, costs, damages, and expenses, and reasonable attorney fees arising out of,

directly or indirectly, any claim of personal injury or death associated with such

unintended or unauthorized use, even if such claim alleges that Freescale

Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

The described product contains a PowerPC processor core. The PowerPC name is a

trademark of IBM Corp. and used under license. All other product or service names are

the property of their respective owners.

© Freescale Semiconductor, Inc., 2005-2014.