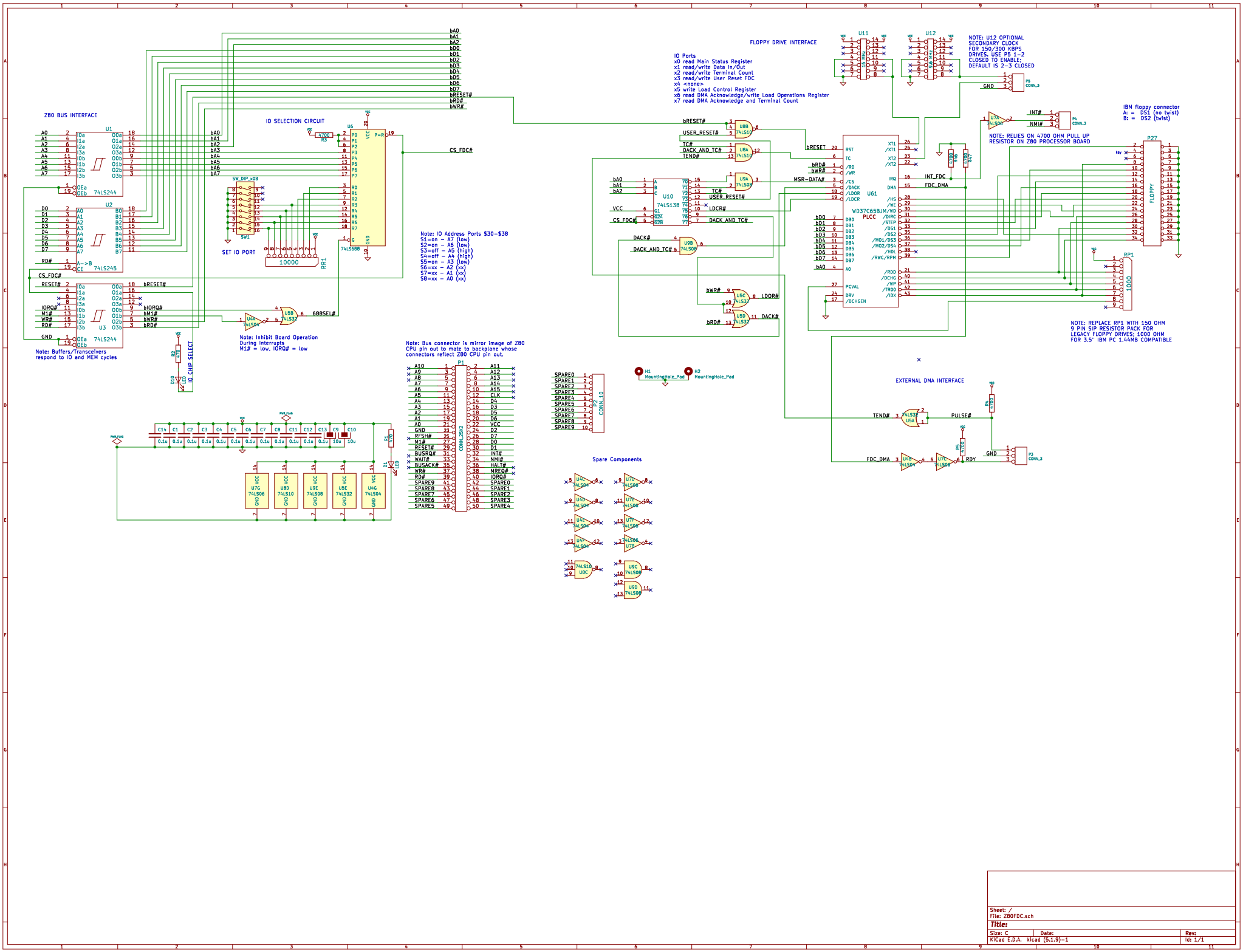
Z80 BUS INTERFACE
IO SELECTION CIRCUIT
SET IO PORT
Note: IO Address Ports $30-$38
S1=on - A7 (low)
S2=on - A6 (low)
S3=off - A5 (high)
S4=off - A4 (high)
S5=on - A3 (low)
S6=xx - A2 (xx)
S7=xx - A1 (xx)
S8=xx - A0 (xx)
Note: Buffers/Transceivers respond to IO and MEM cycles
Note: Inhibit Board Operation During Interrupts M1# = low, IORQ# = low
IO CHIP SELECT
Note: Bus connector is mirror image of Z80 CPU pin out to mate to backplane whose connectors reflect Z80 CPU pin out.
Spare Components
FLOPPY DRIVE INTERFACE
IO Ports
x0 read Main Status Register
x1 read/write Data In/Out
x2 read/write Terminal Count
x3 read/write User Reset FDC
x4 <none>
x5 write Load Control Register
x6 read DMA Acknowledge/write Load Operations Register
x7 read DMA Acknowledge and Terminal Count
NOTE: U12 OPTIONAL SECONDARY CLOCK FOR 150/300 KBPS DRIVES. USE P5 1-2 CLOSED TO ENABLE: DEFAULT IS 2-3 CLOSED
IBM floppy connector
A: = DS1 (no twist)
B: = DS2 (twist)
NOTE: RELIES ON 4700 OHM PULL UP RESISTOR ON Z80 PROCESSOR BOARD
NOTE: REPLACE RP1 WITH 150 OHM 9 PIN SIP RESISTOR PACK FOR LEGACY FLOPPY DRIVES: 1000 OHM FOR 3.5" IBM PC 1.44MB COMPATIBLE
EXTERNAL DMA INTERFACE
WD37C65BJM/WD PLCC
Sheet: /
File: Z80FDC.sch
Title:
Size: C
Date:
Rev:
KiCad E.D.A. kicad (5.1.9)-1
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