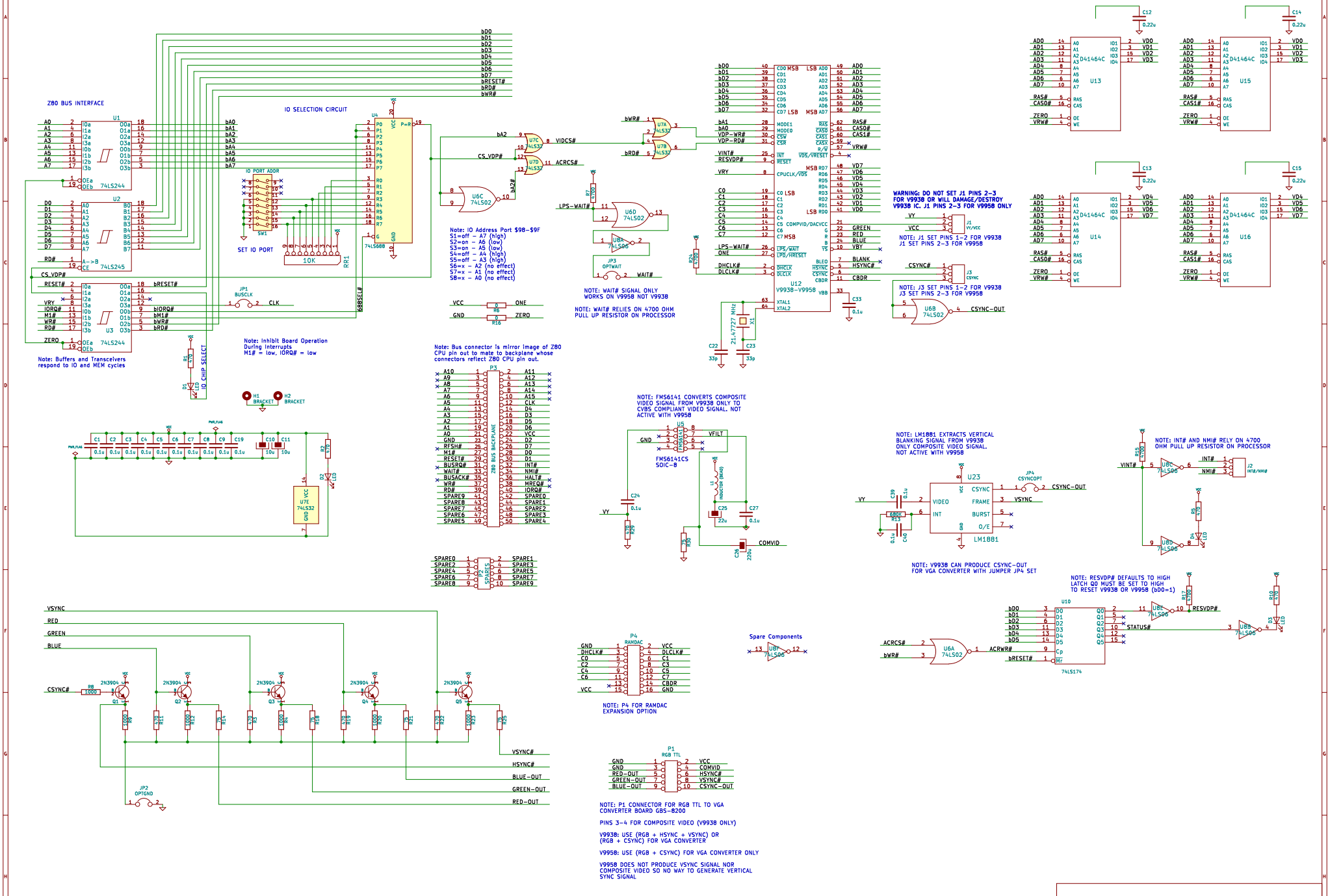
Z80 BUS INTERFACE
IO SELECTION CIRCUIT
IO PORT ADDR
SET IO PORT
Note: IO Address Port $98-$9F
S1=off - A7 (high)
S2=on - A6 (low)
S3=on - A5 (low)
S4=off - A4 (high)
S5=off - A3 (high)
S6=x - A2 (no effect)
S7=x - A1 (no effect)
S8=x - A0 (no effect)
Note: Buffers and Transceivers respond to IO and MEM cycles
Note: Inhibit Board Operation During Interrupts
M1# = low, IORQ# = low
IO CHIP SELECT
Note: Bus connector is mirror image of Z80 CPU pin out to mate to backplane whose connectors reflect Z80 CPU pin out.
Z80 BUS BACKPLANE
NOTE: WAIT# SIGNAL ONLY WORKS ON V9958 NOT V9938
NOTE: WAIT# RELIES ON 4700 OHM PULL UP RESISTOR ON PROCESSOR
WARNING: DO NOT SET J1 PINS 2-3 FOR V9938 OR WILL DAMAGE/DESTROY V9938 IC. J1 PINS 2-3 FOR V9958 ONLY
NOTE: J1 SET PINS 1-2 FOR V9938
J1 SET PINS 2-3 FOR V9958
NOTE: J3 SET PINS 1-2 FOR V9938
J3 SET PINS 2-3 FOR V9958
NOTE: FMS6141 CONVERTS COMPOSITE VIDEO SIGNAL FROM V9938 ONLY TO CVBS COMPLIANT VIDEO SIGNAL. NOT ACTIVE WITH V9958
FMS6141CS
SOIC-8
NOTE: LM1881 EXTRACTS VERTICAL BLANKING SIGNAL FROM V9938 ONLY COMPOSITE VIDEO SIGNAL. NOT ACTIVE WITH V9958
LM1881
NOTE: V9938 CAN PRODUCE CSYNC-OUT FOR VGA CONVERTER WITH JUMPER JP4 SET
NOTE: INT# AND NMI# RELY ON 4700 OHM PULL UP RESISTOR ON PROCESSOR
NOTE: RESVDP# DEFAULTS TO HIGH LATCH Q0 MUST BE SET TO HIGH TO RESET V9938 OR V9958 (bD0=1)
74LS174
NOTE: P4 FOR RAMDAC EXPANSION OPTION
Spare Components
NOTE: P1 CONNECTOR FOR RGB TTL TO VGA CONVERTER BOARD GBS-8200
PINS 3-4 FOR COMPOSITE VIDEO (V9938 ONLY)
V9938: USE (RGB + HSYNC + VSYNC) OR (RGB + CSYNC) FOR VGA CONVERTER
V9958: USE (RGB + CSYNC) FOR VGA CONVERTER ONLY
V9958 DOES NOT PRODUCE VSYNC SIGNAL NOR COMPOSITE VIDEO SO NO WAY TO GENERATE VERTICAL SYNC SIGNAL
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File: Z80VDP1A.sch
Title:
Size: C
Date:
Rev:
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