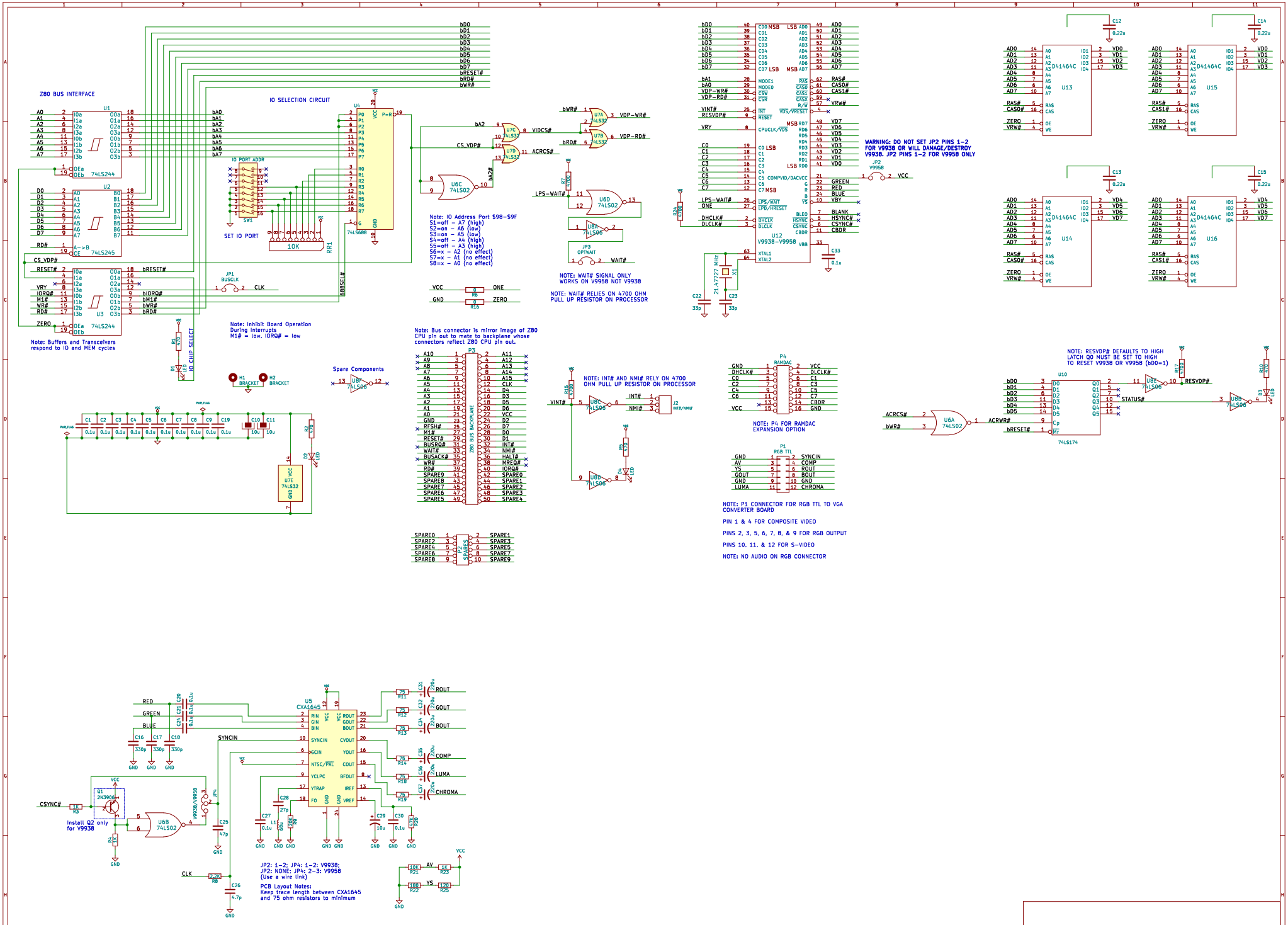
Z80 BUS INTERFACE
IO SELECTION CIRCUIT
IO PORT ADDR
SET IO PORT
Note: IO Address Port $98-$9F
S1=off - A7 (high)
S2=on - A6 (low)
S3=on - A5 (low)
S4=off - A4 (high)
S5=off - A3 (high)
S6=x - A2 (no effect)
S7=x - A1 (no effect)
S8=x - A0 (no effect)
Note: Buffers and Transceivers respond to IO and MEM cycles
Note: Inhibit Board Operation During Interrupts
M1# = low, IORQ# = low
Note: Bus connector is mirror image of Z80 CPU pin out to mate to backplane whose connectors reflect Z80 CPU pin out.
Spare Components
NOTE: WAIT# SIGNAL ONLY WORKS ON V9958 NOT V9938
NOTE: WAIT# RELIES ON 4700 OHM PULL UP RESISTOR ON PROCESSOR
WARNING: DO NOT SET JP2 PINS 1-2 FOR V9938 OR WILL DAMAGE/DESTROY V9938. JP2 PINS 1-2 FOR V9958 ONLY
NOTE: INT# AND NMI# RELY ON 4700 OHM PULL UP RESISTOR ON PROCESSOR
NOTE: RESVDP# DEFAULTS TO HIGH LATCH Q0 MUST BE SET TO HIGH TO RESET V9938 OR V9958 (bD0=1)
NOTE: P4 FOR RAMDAC EXPANSION OPTION
NOTE: P1 CONNECTOR FOR RGB TTL TO VGA CONVERTER BOARD
PIN 1 & 4 FOR COMPOSITE VIDEO
PINS 2, 3, 5, 6, 7, 8, & 9 FOR RGB OUTPUT
PINS 10, 11, & 12 FOR S-VIDEO
NOTE: NO AUDIO ON RGB CONNECTOR
Install Q2 only for V9938
JP2: 1-2: V9938;
JP2: NONE; JP4: 2-3: V9958
(Use a wire link)
PCB Layout Notes:
Keep trace length between CXA1645 and 75 ohm resistors to minimum
Sheet: /
File: Z80VDP1B.sch
Title:
Size: C
Date:
Rev:
KiCad E.D.A. kicad (5.1.10)-1
Id: 1/1