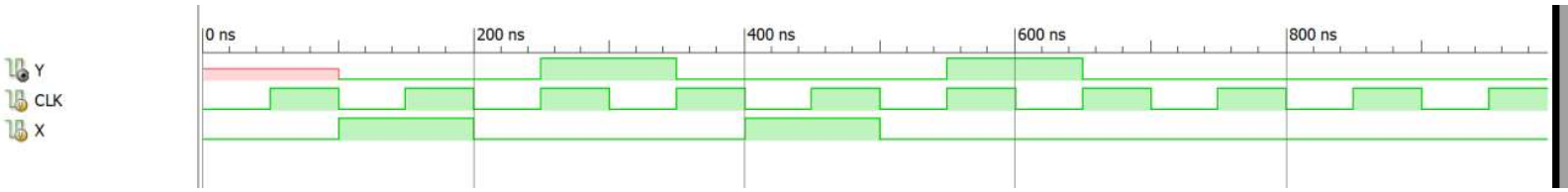
It is not working on posedge



Testbench:

```
module DFFTest;

	// Inputs
	reg CLK;
	reg X;

	// Outputs
	wire Y;

	// Instantiate the Unit Under Test (UUT)
	sequence_detector uut (
		.Y(Y),
		.CLK(CLK),
		.X(X)
	);

	initial begin
		// Initialize Inputs
		X = 0;
		CLK = 0;
		#100;
		X = 1;
		#100;
```

```
                X = 0;
                #100;
                X = 0;
                #100;
                X = 1;
                #100;
                X = 0;
                #100;
                X = 0;
                #100;
        end
  always #50 CLK = !CLK;
endmodule
```

Code

```
module D_FlipFLop( Q, D, CLK);
        output reg Q;
        input D, CLK;
        always @(posedge CLK)
                Q = D;
endmodule
module sequence_detector(Y,CLK,X);
        input CLK;
        input X;
        output Y;
        wire W1,W2,W3;
        D_FlipFLop first (.Q(W1),.D(X),.CLK(CLK));
        assign W2 = W1 && ~X;
        D_FlipFLop second(.Q(W3),.D(W2),.CLK(CLK));
        assign Y= ~W1 && ~X && W3;
endmodule
```