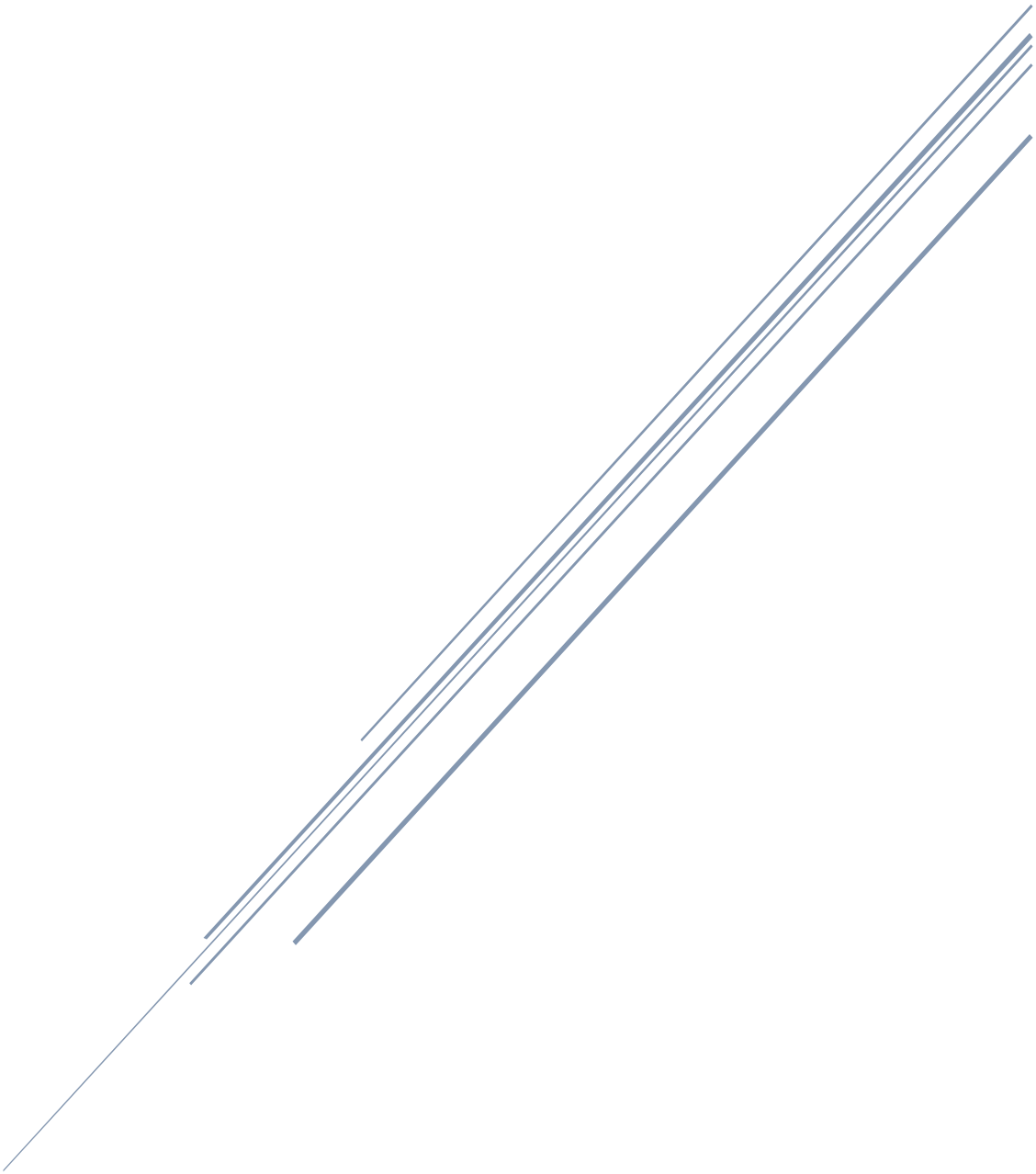
VERILOG ASSIGNMENT 3

21604552 – Emre Hancı



Hacettepe University - Department of Computer Engineering

BBM233 Logic Design Lab.

-Verilog Codes

```
module Afunc(input A,B,C,D, output a);
        assign a = (B && !D) || (!A && !B &&!C &&D);
endmodule
module Bfunc(input A,B,C,D, output b);
        assign b = (B && !C && D) || (B && C && !D);
endmodule
module Cfunc(input A,B,C,D, output c);
        assign c = (!B && C && !D);
endmodule
module Dfunc(input A,B,C,D, output d);
        assign d = (!B && !C && D) || (B && !C && !D) || (B && C && D);
endmodule
module Efunc(input A,B,C,D, output e);
        assign e = (D) || (B && !C);
endmodule
module Ffunc(input A,B,C,D, output f);
        assign f =(C && D) || (!B && C) || (!A && !B && D);
endmodule
module Gfunc(input A,B,C,D, output g);
        assign g = (!A && !B && !C) || (B && C && D);
endmodule
module Lab3Exp(input A,B,C,D, output a,b,c,d,e,f,g);
        Afunc AA(A,B,C,D,a);
        Bfunc BB(A,B,C,D,b);
        Cfunc CC(A,B,C,D,c);
        Dfunc DD(A,B,C,D,d);
        Efunc EE(A,B,C,D,e);
        Ffunc FF(A,B,C,D,f);
        Gfunc GG(A,B,C,D,g);
Endmodule
```

-Testbench

```
module TestBench;

	// Inputs
	reg A;
	reg B;
	reg C;
	reg D;

	// Outputs
	wire a;
	wire b;
	wire c;
	wire d;
	wire e;
	wire f;
	wire g;

	// Instantiate the Unit Under Test (UUT)
	Lab3Exp uut (
		.A(A),
		.B(B),
		.C(C),
		.D(D),
		.a(a),
		.b(b),
		.c(c),
		.d(d),
		.e(e),
		.f(f),
		.g(g)
```

```
	);

	initial begin

		// Initialize Inputs
		A = 0; B = 0; C = 0; D = 0;#100
		A = 0; B = 0; C = 0; D = 1;#100
		A = 0; B = 0; C = 1; D = 0;#100
		A = 0; B = 0; C = 1; D = 1;#100
		A = 0; B = 1; C = 0; D = 0;#100
		A = 0; B = 1; C = 0; D = 1;#100
		A = 0; B = 1; C = 1; D = 0;#100
		A = 0; B = 1; C = 1; D = 1;#100
		A = 1; B = 0; C = 0; D = 0;#100
		A = 1; B = 0; C = 0; D = 1;#100
		A = 1; B = 0; C = 0; D = 1;#100
		// Wait 100 ns for global reset to finish
		#100;

		// Add stimulus here

	end

endmodule
```

-Waveform