Hacettepe University
Faculty of Engineering
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BBM233 – First Verilog Assignment

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-Verilog Code

```
module Assignment1(F,A,B,C);
   input A,B,C;
   output F;
   wire and1, and2;
   and(and1,A,B);
   and(and2,B,C);
   or(F,and1,and2);

endmodule
```

-Testbench

```
module FirstAssignmentTestbench;

	// Inputs
	reg A;
	reg B;
	reg C;

	// Outputs
	wire F;

	// Instantiate the Unit Under Test (UUT)
	Assignment1 uut (
		.A(A),
		.B(B),
		.C(C),
		.F(F)
	);

	initial begin
		// Initialize Inputs
		A = 0;
		B = 0;
		C = 0;

		// Wait 100 ns for global reset to finish
		#100;
		// Add stimulus here

		A = 0;
		B = 0;
		C = 1;

		// Wait 100 ns for global reset to finish
		#100;
		A = 0;
		B = 1;
		C = 0;

		// Wait 100 ns for global reset to finish
		#100;

		A = 0;
		B = 1;
		C = 1;

		// Wait 100 ns for global reset to finish
		#100;

		A = 1;
		B = 0;
		C = 0;
```

```
        #100;

        A = 1;
        B = 0;
        C = 1;

        // Wait 100 ns for global reset to finish
        #100;

        A = 1;
        B = 1;
        C = 0;

        // Wait 100 ns for global reset to finish
        #100;

        A = 1;
        B = 1;
        C = 1;

        // Wait 100 ns for global reset to finish
        #100;

    end

endmodule
```

-Waveform